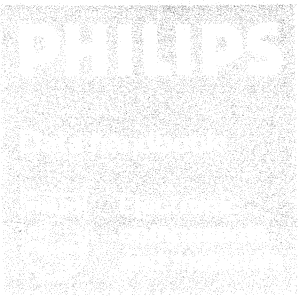

Semiconductors and integrated circuits

Part 6 March 1972

Digital Integrated Circuits

DTL, HNIL, TTL, CML, MOS

SEMICONDUCTORS AND INTEGRATED CIRCUITS

Part 6 **March 1972**

DATA HANDBOOK SYSTEM

To provide you with a comprehensive source of information on electronic components, subassemblies and materials, our Data Handbook System is made up of three series of handbooks, each comprising several parts.
The three series, identified by the colours noted, are:

ELECTRON TUBES (9 parts) BLUE

SEMICONDUCTORS AND INTEGRATED CIRCUITS (6 parts) RED

COMPONENTS AND MATERIALS (7 parts) GREEN

The several parts contain all pertinent data available at the time of publication, and each is revised and reissued annually; the contents of each series are summarized on the following pages.
We have made every effort to ensure that each series is as accurate, comprehensive and up-to-date as possible, and we hope you will find it to be a valuable source of reference. Where ratings or specifications quoted differ from those published in the preceding edition they will be pointed out by arrows. You will understand that we can not guarantee that all products listed in any one edition of the handbook will remain available, or that their specifications will not be changed, before the next edition is published. If you need confirmation that the published data about any of our products are the latest available, may we ask that you contact our representative. He is at your service and will be glad to answer your inquiries.

December 1971

ELECTRON TUBES (BLUE SERIES)

This series consists of the following parts, issued on the dates indicated.

Part 1 — **January 1972**

Transmitting tubes (Tetrodes, Pentodes)
Amplifier circuit assemblies

Part 2 — **February 1972**

Tubes for microwave equipment

Part 3 — **March 1972**

Special Quality tubes
Miscellaneous devices

Part 4 — **April 1971**

Receiving tubes

Part 5 — **May 1971**

Cathode-ray tubes
Photo tubes
Camera tubes
Associated accessories

Part 6 — **June 1971**

Photomultipliers tubes
Channel electron multipliers
Scintillators
Photoscintillators
Radiation counter tubes
Semiconductor radiation detectors
Neutron generator tubes
Photo diodes
Associated accessories

Part 7 — **July 1971**

Voltage stabilizing and reference tubes
Counter, selector, and indicator tubes
Trigger tubes
Switching diodes
Thyratrons
Ignitrons
Industrial rectifying tubes
High-voltage rectifying tubes

Part 8 — **August 1971**

T.V. Picture tubes

Part 9 — **December 1971**

Transmitting tubes (Triodes)
Tubes for R.F. heating (Triodes)
Associated accessories

March 1972

SEMICONDUCTORS AND INTEGRATED CIRCUITS (RED SERIES)

This series consists of the following parts, issued on the dates indicated.

Part 1 Diodes and Thyristors — **September 1971**

General
Signal diodes
Variable capacitance diodes
Voltage regulator diodes
Rectifier diodes
Thyristors, diacs, triacs
Rectifier stacks
Accessories
Heatsinks

Part 2 Low frequency; Deflection — **October 1971**

General
Low frequency transistors (low power)
Low frequency power transistors
Deflection transistors
Accessories

Part 3 High frequency; Switching — **November 1971**

General
High frequency transistors
Switching transistors
Accessories

Part 4 Special types — **December 1971**

General
Transmitting transistors
Microwave devices
Field effect transistors
Dual transistors
Microminiature devices for thick- and thin-film circuits
Photoconductive devices
Photodiodes
Phototransistors
Light emitting diodes
Infra-red sensitive devices
Accessories

Part 5 Linear Integrated Circuits — **February 1972**

General
Linear integrated circuits

Part 6 Digital integrated circuits — **March 1972**

General
DTL (FC family)
DTL/HNIL (FZ family)
TTL (FJ family)
TTL (GJ family)
CML (GH family)
MOS (FD family)

March 1972

COMPONENTS AND MATERIALS (GREEN SERIES)

This series consists of the following parts, issued on the dates indicated.

Part 1 Circuit Blocks, Input/Output Devices, Electro-mechanical Components *), Peripheral Devices — **October 1971**

Circuit blocks 40-Series
Counter modules 50-Series
Norbits 60-Series, 61-Series
Circuit blocks 90-Series
Input/output devices
Electro-mechanical components *)
Peripheral devices

Part 2 Resistors, Capacitors — **December 1971**

Fixed resistors
Variable resistors
Non-linear resistors
Ceramic capacitors
Paper capacitors and film capacitors
Electrolytic capacitors
Variable capacitors

Part 3 Radio, Audio, Television — **February 1972**

FM tuners
Coil assemblies
Piezoelectric ceramic resonators and filters
Loudspeakers
Audio and mains transformers
Television tuners, aerial input assemblies
Components for black and white television
Components for colour television
Deflection assemblies for camera tubes

Part 4 Magnetic Materials, Piezoelectric Ceramics — **April 1971**

Ferrites for radio, audio and television
Small coils, assemblies and assembling parts
Ferroxcube potcores and square cores
Ferroxcube transformer cores
Piezoxide
Permanent magnet materials

Part 5 Memory Products, Magnetic Heads, Quartz Crystals, Microwave Devices, Variable Transformers — **June 1971**

Ferrite memory cores
Matrix planes, matrix stacks
Complete memories
Magnetic heads
Quartz crystal units, crystal filters
Isolators, circulators
Variable mains transformers

Part 6 Electric Motors and Accessories, Timing and Control Devices — **August 1971**

Stepper motors
Small synchronous motors
Asynchronous motors
Small d.c. motors
Tachogenerators and servomotors
Indicators for built-in test equipment

Part 7 Circuit Blocks — **September 1971**

Circuit blocks 100kHz Series
Circuit blocks 1-Series
Circuit blocks 10-Series
Circuit blocks for ferrite core memory drive

*) From October 1971 published in Part 1 instead of Part 5.

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General

PREFACE TO DATA OF INTEGRATED CIRCUITS

1. General

The published data comprise particulars needed by designers of equipment in which integrated circuits are to be incorporated, and criteria on which to base acceptance testing of such circuits. For ease of reference, the data on each circuit are grouped according to the several headings discussed below.
The limiting values quoted under the headings Characteristics and Package Outline may be taken as references for acceptance testing.
Values cited as typical are given for information only.
For an explanation of the type designation code, see the section Type Designation.
For an explanation of the letter symbols used in designating terminals and performance of integrated circuits, and the electrical and logic quantities pertaining to them, see the section Letter Symbols.

2. Quick Reference Data

The main properties of the integrated circuit summarized for quick reference

3. Ratings

Ratings are limits beyond which the serviceability of the integrated circuit may be impaired. The ratings given here are in accordance with the Absolute Maximum System as defined in publication no. 134 of the International Electrical Commission; for further details see item 2 of the section Rating Systems.
If a circuit is used under the conditions set forth in the sections Characteristics and Additional System Design Data, its operation within the ratings is ensured.

4. Circuit diagram

Circuit diagrams and logic symbols are given to illustrate the circuit function. The diagrams show only essential elements, parasitic elements due to the method of manufacture normally being omitted. The manufacturer reserves the right to make minor changes to improve manufacturability.

5. System Design Data and Additional System Design Data

System Design Data normally derived from the Characteristics and based on worst-case assumptions as to temperature, loading and supply voltage, are quoted for the guidance of equipment designers. Supplementary information derived from measurements on large production samples may be given under Additional System Design Data.

6. Application information

Under this heading, practical circuit connections and the resulting performance are described. Care has been taken to ensure the accuracy and completeness of the information given, but no liability therefor is assumed, nor is licence under any patent implied.

7. Characteristics

Characteristics are measurable properties of the integrated circuit described. Under a specific set of test conditions compliance with limit values given under this heading establishes the specified performance of the circuit; this can be used as a criterion for acceptance testing.
Values cited as typical are given for information only and are not subject to any form of guarantee.

8. Logic symbols (digital circuits)

Graphical logic symbols accord with MIL standard 806B.
Supplementary drawings correlate logic functions with pin locations as a help to laying out printed circuit boards.

9. Outline drawing and pin 1 identification

Dimensional drawings indicate the pin numbering of circuit packages.
Dual in-line packages have a notch at one end to identify pin 1.
Take care not to mistake adventitious moulding marks for the pin 1 identification.
Flat packs identify pin 1 by a small projection on the pin itself and/or by a dot on the body of the package.
Metal can encapsulations identify pin 1 by a tab on the rim of the can.

PRO ELECTRON TYPE DESIGNATION CODE

The type number consists of three letters followed by three figures (sometimes followed by a version letter*)
For the purpose of type designation integrated circuits are divided in four groups:
- Digital family circuits
- Digital solitary circuits
- Analogue (including linear) circuits
- Mixed digital/analogue circuits

DIGITAL FAMILY TYPES

First two letters: family
Third letter: circuit function
First two figures: serial number
Third figure: operating ambient temperature range

DIGITAL SOLITARY TYPES

First letter: "S"
Second letter: extension of serial number
Third letter: circuit function
First two figures: serial number
Third figure: operating ambient temperature range

ANALOGUE (LINEAR) TYPES

First letter: "T"
Second and third letter: extension of serial number
First two figures: serial number
Third figure: operating ambient temperature range

MIXED DIGITAL/ANALOGUE TYPES

First letter: "U"
Second and third letter: extension of serial number
First two figures: serial number
Third figure: operating ambient temperature range

*The version letter denotes a variant with respect to electrical performance and/or encapsulation

FUNCTION

H = Combinatorial circuit
J = Bistable or multistable sequential circuit
K = Monostable sequential circuit
L = Level converter
N = Bimetastable or multimetastable sequential circuit
Q = Read/write memory circuit
R = Read-only memory circuit
S = Sense amplifier
Y = Miscellaneous

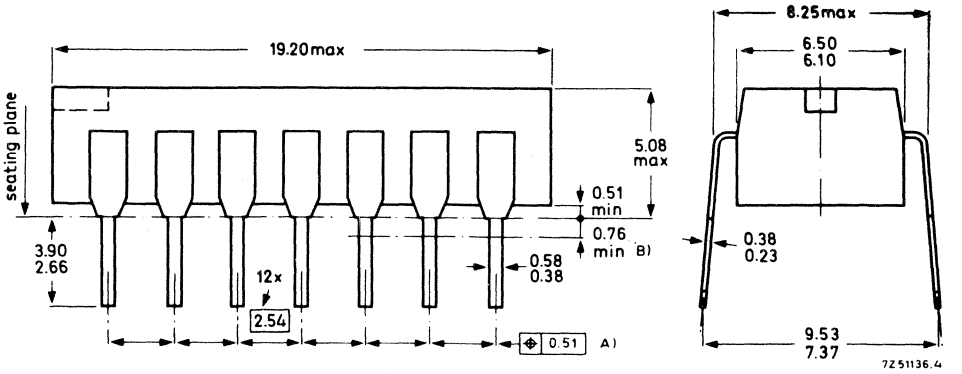
OPERATING AMBIENT TEMPERATURE RANGE

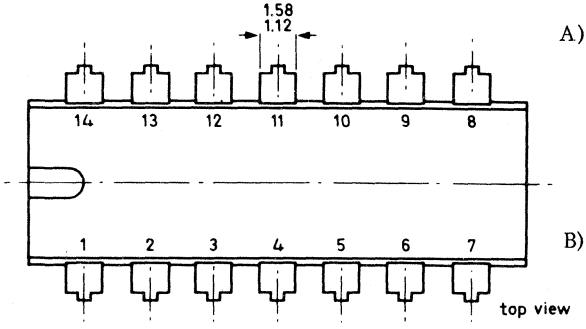
1 = 0 to + 70 °C or wider
2 = −55 to +125 °C or wider
3 = −10 to + 85 °C or wider
4 = +15 to + 55 °C or wider
5 = −25 to + 70 °C or wider
6 = −40 to + 85 °C or wider
0 = Open

PACKAGE OUTLINES

14 LEAD PLASTIC DUAL IN-LINE (type A)

Dimensions in mm





A) Centre-lines of all leads are within ± 0.254 mm of the nominal positions shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0.51 mm.

B) Lead spacing tolerances apply from seating plane to the line indicated.

SOLDERING

1. By hand

   Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300°C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

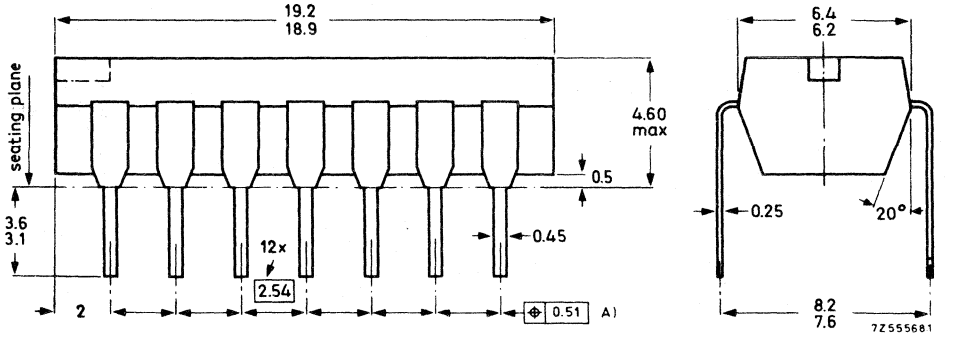
   260 °C is the maximum allowable temperature of the solder; it must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
   The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the allowable limit.

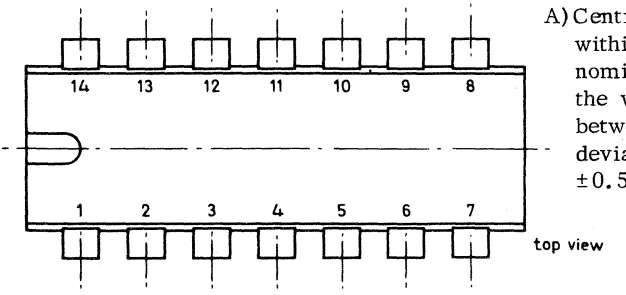
3. Repairing soldered joints

   The same precautions and limits apply as in (1) above.

14 LEAD PLASTIC DUAL IN-LINE (type B)

Dimensions in mm





A) Centre-lines of all leads are within ± 0.254 mm of the nominal positions shown: in the worst case, the spacing between any two leads may deviate from nominal by ±0.51 mm.

SOLDERING

1. By hand

   Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for more than 5 seconds.

2. By dip or wave

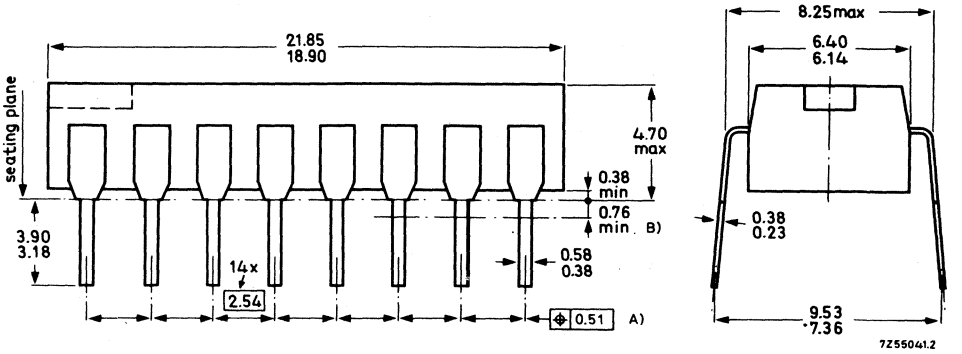
   260 °C is the maximum allowable temperature of the solder; it must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
   The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the allowable limit.

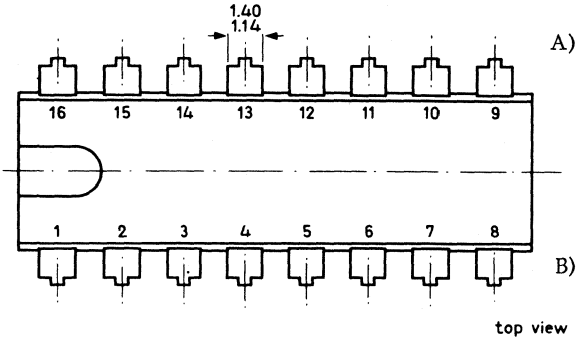
3. Repairing soldered joints

   The same precautions and limits apply as in (1) above.

16 LEAD PLASTIC DUAL IN-LINE (type A)

Dimensions in mm





A) Centre-lines of all leads are within ± 0.254 mm of the nominal positions shown; in the worst case, the spacing between any two leads may deviate from nominal by ± 0.51 mm.

B) Lead spacing tolerances apply from seating plane to the line indicated.

SOLDERING

1. By hand

   Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

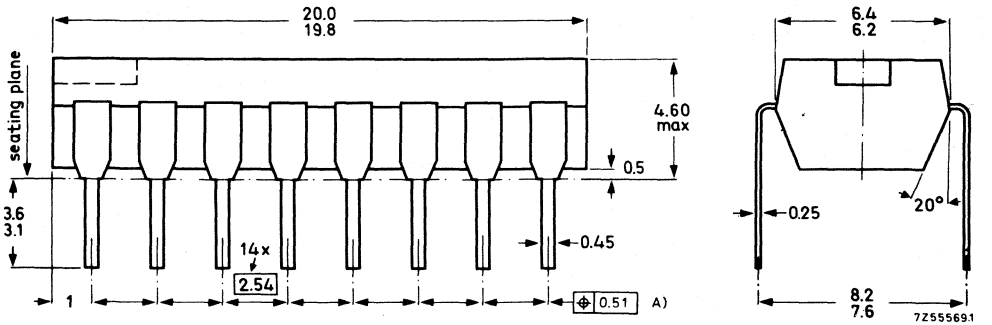
   260 °C is the maximum allowable temperature of the solder; it must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
   The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the allowable limit.

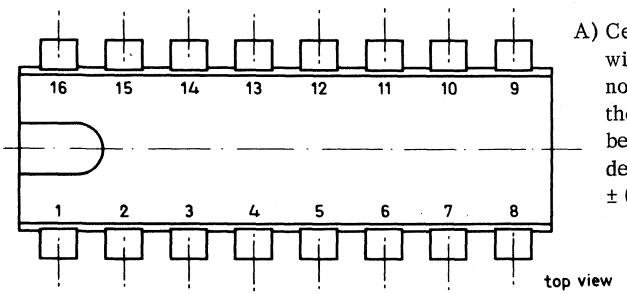
3. Repairing soldered joints

   The same precautions and limits apply as in (1) above.

16 LEAD PLASTIC DUAL IN-LINE (type B)

Dimensions in mm





A) Centre-lines of all leads are within ± 0.254 mm of the nominal positions shown; in the worst case, the spacing between any two leads may deviate from nominal by ± 0.51 mm.

SOLDERING

1. By hand

   Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

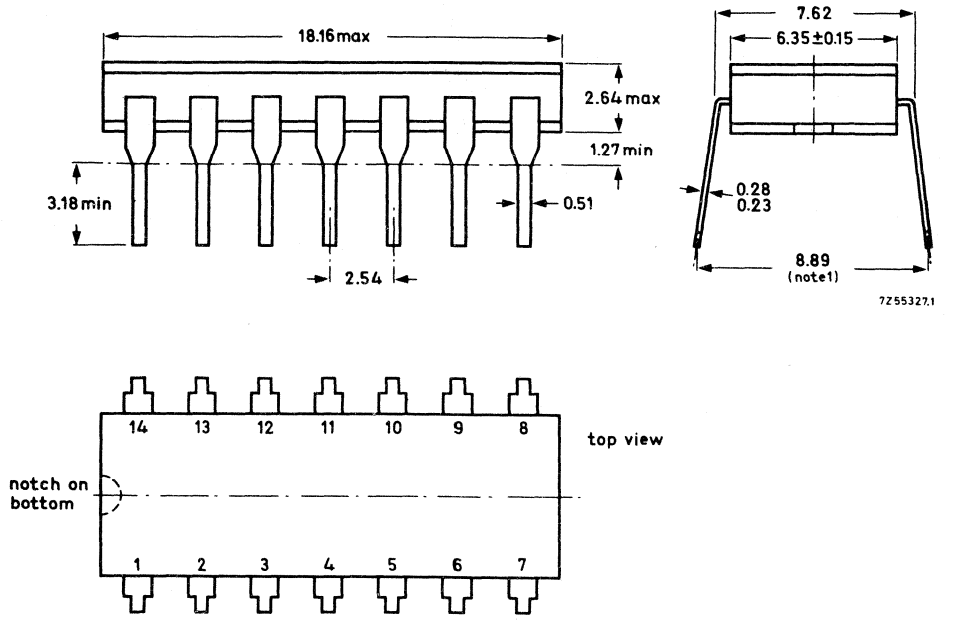
   260 °C is the maximum allowable temperature of the solder; it must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
   The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the allowable limit.

3. Repairing soldered joints

   The same precautions and limits apply as in (1) above.

14 LEAD METAL-CERAMIC DUAL IN-LINE

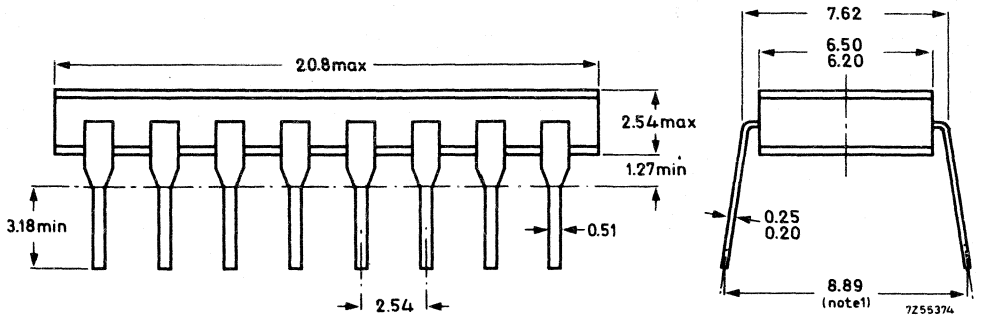
Dimensions in mm

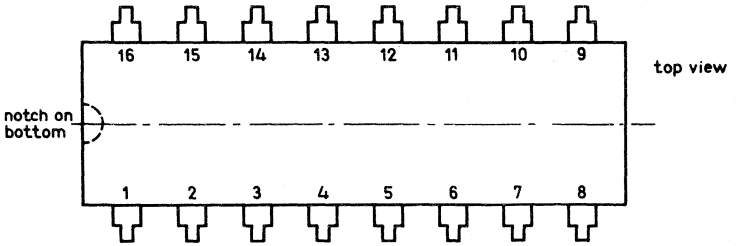


1. Leads on opposite sides are designed to fit in holes 7.62 mm apart. They are given positive misaligment so that they grip after insertion.
2. Pin 1 is normally marked by a dot.

16 LEAD METAL-CERAMIC DUAL IN-LINE

Dimensions in mm

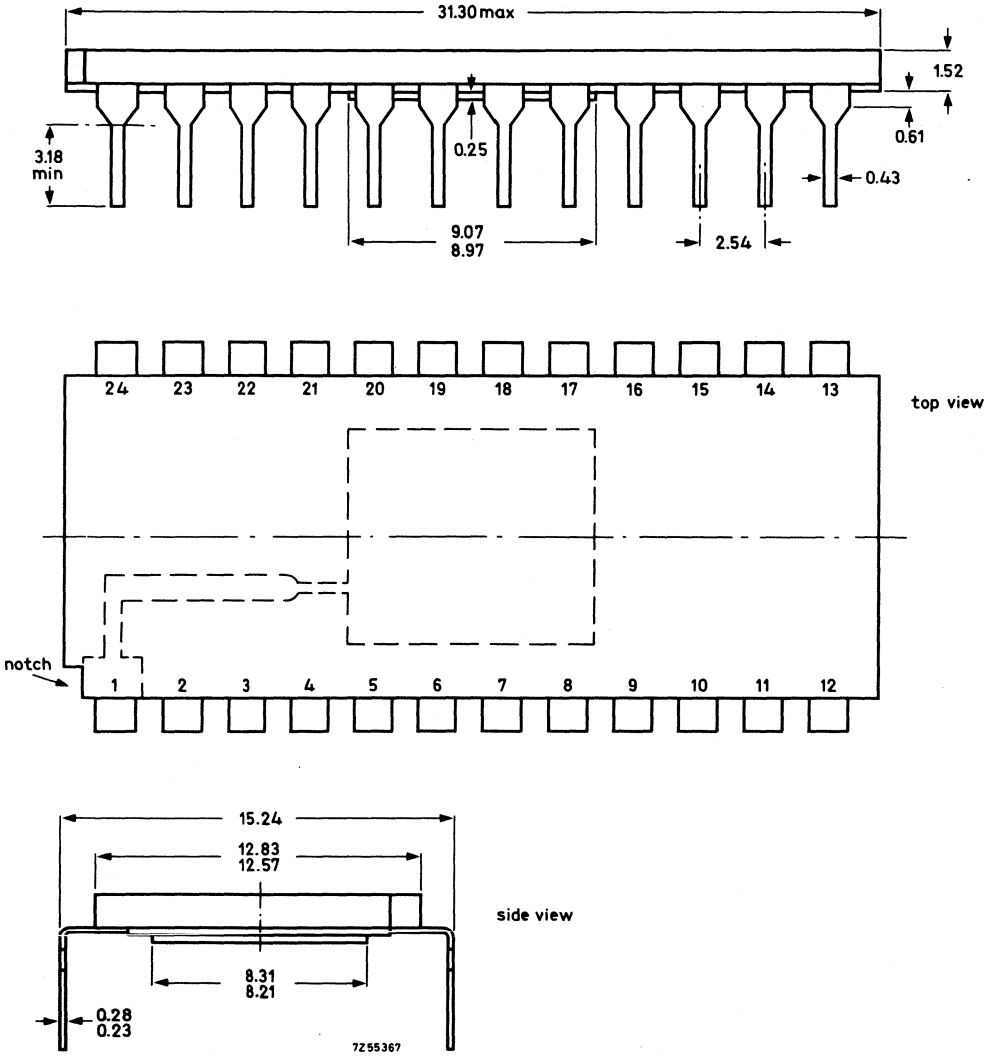




1. Leads on opposite sides are designed to fit in holes 7.62 mm apart. They are given positive misaligment so that they grip after insertion.
2. Pin 1 is normally marked by a dot.

24 LEAD METAL-CERAMIC DUAL IN-LINE

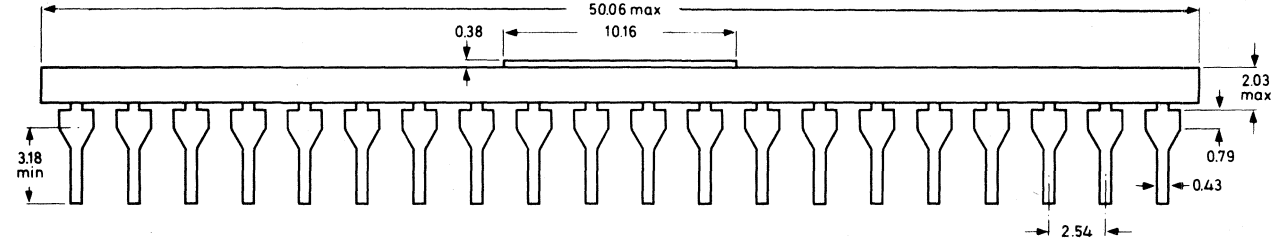
Dimensions in mm

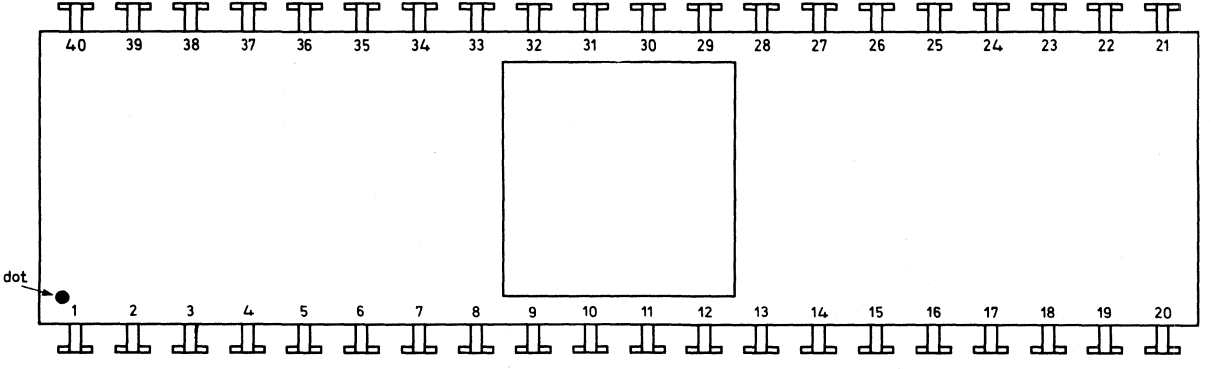


Notes

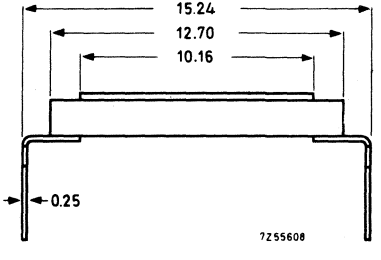
1. Leads on opposite sides are designed to fit in holes 15.24 mm apart.
2. Pin 1 is marked by a notch and connected to the metal lid on the bottom of the package.

40 LEAD METAL-CERAMIC DUAL IN-LINE





top view



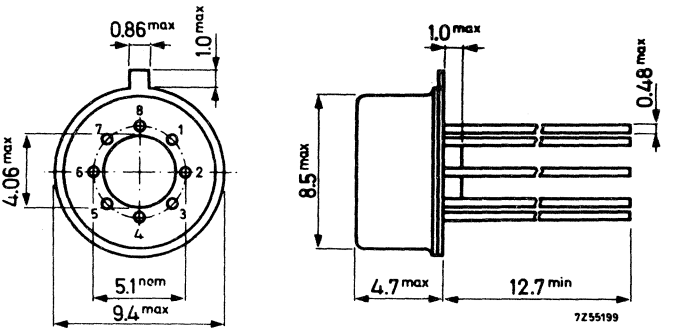
side view

Notes

1. Leads on opposite sides are designed to fit in holes 15.24 mm apart.
2. Pin 1 is marked by a dot.
3. Dimensions in mm.

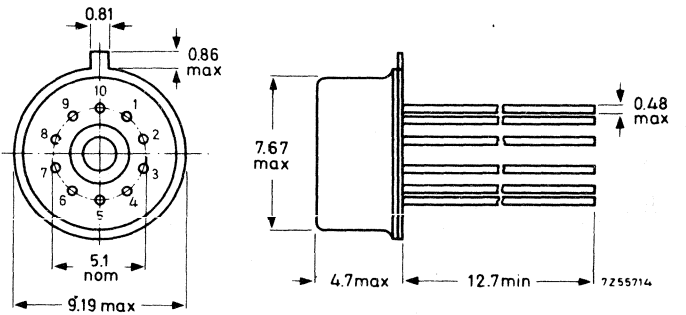
TO-99 METAL ENVELOPE

Dimensions in mm



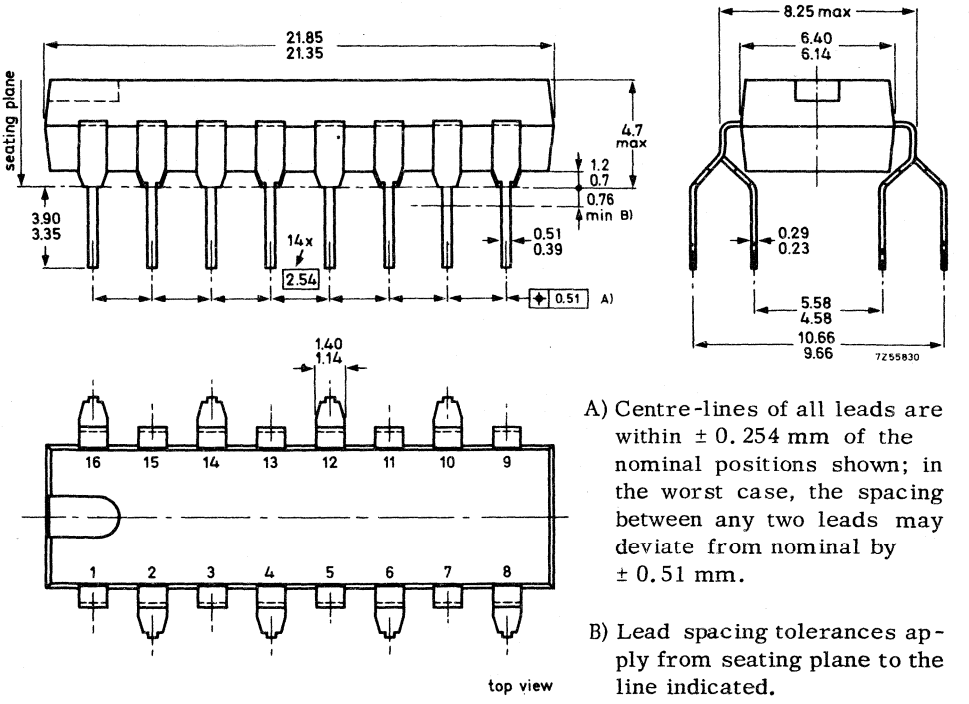
TO-100 METAL ENVELOPE

Dimensions in mm



16 LEAD PLASTIC QUADRUPLE IN-LINE

Dimensions in mm



A) Centre-lines of all leads are within ± 0.254 mm of the nominal positions shown; in the worst case, the spacing between any two leads may deviate from nominal by ± 0.51 mm.

B) Lead spacing tolerances apply from seating plane to the line indicated.

SOLDERING

1. By hand

   Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

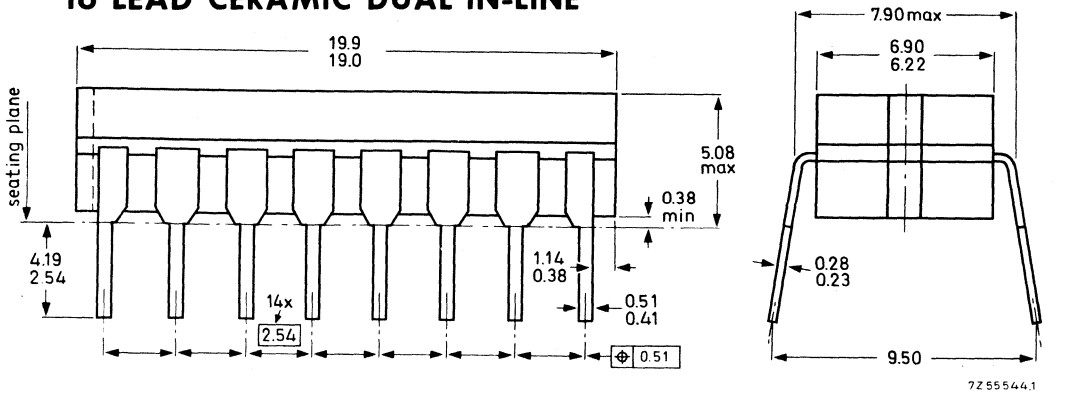
2. By dip or wave

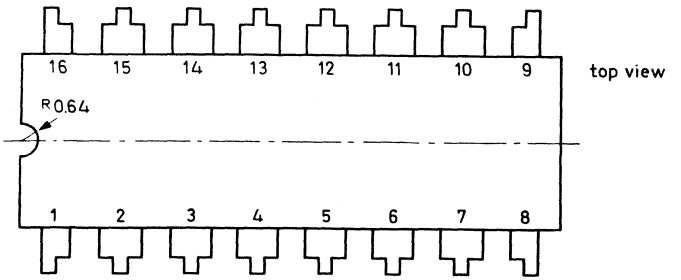
   260 °C is the maximum allowable temperature of the solder; it must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
   The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the allowable limit.

3. Repairing soldered joints

   The same precautions and limits apply as in (1) above.

16 LEAD CERAMIC DUAL IN-LINE



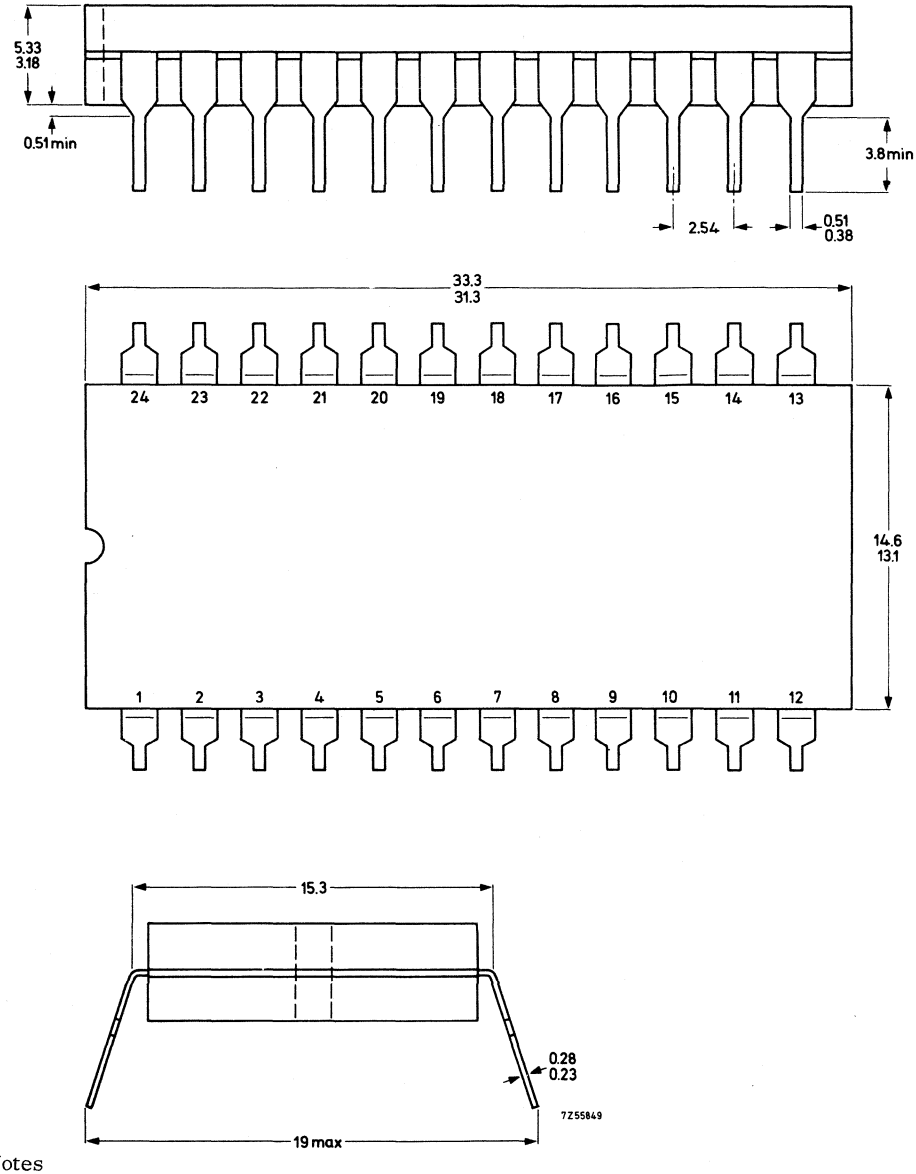


Notes

1. Leads are given positive misalignment so that they grip after insertion.
2. Leads are tin plated Kovar.

24 LEAD CERAMIC DUAL IN-LINE

Dimensions in mm



Notes

1. Leads on opposite sides are designed to fit in holes 15.24 mm apart. They are given positive misalignment so that they grip after insertion.
2. Leads are gold plated Kovar.

Measures to be taken when handling MOS devices

Though all our MOS integrated circuits incorporate protection against electrostatic discharges, they can nevertheless be damaged by accidental overvoltages. In storing and handling them, the following precautions should be observed.

1. Store and transport the circuits in carriers that either short-circuit all leads or insulate all leads from external contact.

2. Work on a conductive surface (e.g. a metal table top) when testing the circuits or transferring them from one carrier to another. Electrically connect the person doing the testing or handling to the conductive surface, as by a metal bracelet and a conductive cord or chain. Also connect all testing and handling equipment to the surface.

3. Mount MOS integrated circuits on printed circuit boards after all other components have been mounted. Take care that the circuits themselves, metal parts of the board, mounting tools, and the person doing the mounting are kept at the same electric potential (earth).
   If it is impossible to earth the printed circuit board, the person mounting the circuits should touch the board before bringing a MOS circuit into contact with it.
   The soldering iron or bath should also be kept at the same potential as the MOS circuit and the board.

4. Avoid building up electrostatic charges through movement of air over non-conductive material (plastics, ceramics). Acid sinks and test ovens call for special precautions in this regard.
   Beware of voltage surges due to:
   - switching electrical equipment on or off
   - relays
   - a.c. lines.

5. If possible, dress personnel in anti-static clothing (no wool, silk, or synthetic fibres).

N.B. Points 2 and 3 call for special attention to personnel safety.

GATE SYMBOLS

Symbols taken from MIL-STD-806B published 26-2-1962 together with the explanation given in the MIL-STD are framed (the number in brackets refers to the section of the MIL-STD from which the extract has been made).
Other symbols and explanations are unframed.

A. LOGIC SYMBOLS (5 partial)*)

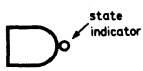
AND The symbol shown below represents the AND function (5.1).

OR The symbol shown below represents the OR function (5.2).

EXCLUSIVE-OR The symbol shown below represents the Exclusive-OR function (5.6).

STATE INDICATOR (Active) (5.3). The presence of the small circle symbol at the input(s) or output(s) of a function indicates:

(a) Input Condition. The electrical condition at the input terminal(s) which control the active state of the respective function.
(b) Output Condition. The electrical condition existing at the output terminal(s) of an activated function.



(5.3.1) A small circle(s) at the input(s) to any element (logical or non-logical) indicates that the relatively LOW (L) input signal activates the function. Conversely, the absence of a small circle indicates that the relatively HIGH (H) input signal activates the function.
(5.3.2) A small circle at the symbol output indicates that the output terminal of the activated function is relatively LOW (L), the absence indicates that the output terminal is relatively HIGH (H).
This small circle shall never be drawn by itself on a diagram.

On pages 4 and 5 the terms HIGH and LOW and the translation of logic notations "0" and "1" into HIGH and LOW will be elucidated.

*) See appendix for drawing dimensions.

EXAMPLES

AND (5.1.1)

A	B	X
L	L	L
H	L	L
L	H	L
H	H	H

The output is HIGH if and only if all inputs are HIGH.

(5.4)

A	B	X
L	L	H
H	L	H
L	H	H
H	H	L

The output is LOW if and only if all inputs are HIGH

OR (5.2.1)

A	B	X
L	L	L
H	L	H
L	H	H
H	H	H

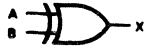
The output is HIGH if and only if any one or more of the inputs are HIGH.

(5.5)

A	B	X
L	L	H
H	L	L
L	H	L
H	H	L

The output is LOW if and only if any one or more of the inputs are HIGH.

EXCLUSIVE-OR (5.6.1)



A	B	X
L	L	L
H	L	H
L	H	H
H	H	L

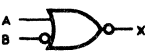
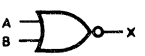
The output is HIGH if and only if any one input is HIGH and all other inputs are LOW.

A	B	X
L	L	H
H	L	L
L	H	L
H	H	H

The output is LOW if and only if any one input is HIGH and all other inputs are LOW.

Table I, (5.7) of MIL-STD-806B, shows two-input AND and OR gate symbols with all the possible combinations of terminals with or without state indicator. It will be noted that the AND-gate symbol in the 1st column has the same function table as the OR-gate symbol in the 2nd column.

Table I

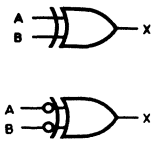
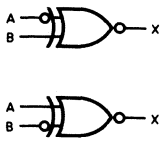
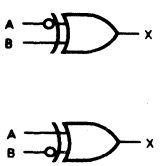
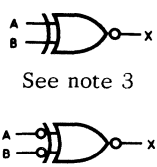
AND	OR	Function Table A B | X
		H H | H H L | L L H | L L L | L
		H H | L H L | L L H | H L L | L
		H H | L H L | H L H | L L L | L
 See note 1		H H | L H L | L L H | L L L | H
		H H | H H L | H L H | H L L | L
		H H | H H L | L L H | H L L | H
		H H | H H L | H L H | L L L | H
 See note 2		H H | L H L | H L H | H L L | H

Note 1. In literature often described as NOR.
Note 2. In literature often described as NAND.

Although the MIL-STD-806B does not use the expression NAND and NOR they are referred to becaused these terms are commonly used.

Although MIL-STD-806B shows the EXCLUSIVE-OR symbol only without state indicator, for the sake of completeness Table II shows it with all the possible combinations of terminals with or without state indicator. It will be noted from the table that one function table (3rd column) is applicable to four symbols.

Table II

Symbol	Symbol	Function Table
		A B | X H H | L H L | H L H | H L L | L
	 See note 3	A B | X H H | H H L | L L H | L L L | H

Note 3. In literature described as BINARY COMPARATOR

HIGH AND LOW

The terms relatively HIGH and relatively LOW are explained with reference to the following three examples

+5 volts = HIGH
+0.5 volts = LOW

+0.5 volts = HIGH
-5 volts = LOW

-5 volts = HIGH
-10 volts = LOW

It can be seen that the more positive voltage is termed relatively HIGH and the less positive is termed relatively LOW. These terms are abbreviated to HIGH (H) and LOW (L) respectively and are used throughout MIL-STD-806B.

LOGICAL "1" AND "0"

In deviation from MIL-STD-806B Appendix B, which for the sake of fully general systems applicability (page 17, fig.5) refrains from establishing any fixed relations between "active-nonactive" and "logical 0-1", we have in the following rules chosen to relate "active" to "1" and "non-active" to "0", as being most suitable when regarding each gate function separately.

"0" at the input always symbolizes the non-activating signal or, at the output, the signal from a non-activated gate;

"1" at the input always symbolizes the activating signal or, at the output, the signal from an activated gate. (The expression activated does not mean that current must flow at the respective terminal(s) but refers to the influence of inputs upon the output(s) of the respective gates.)

The translation from the logic notation into the electrical levels HIGH and LOW is explained with the aid of two examples, one without state indicators and one with. In each case a two-input AND gate truth table is drawn up, and a function table corresponding to the symbol is given so that a direct comparison can be made.

For inputs or outputs	without state indicator	with state indicator
	Logic 1 = HIGH (H)	Logic 1 = LOW (L)
	Logic 0 = LOW (L)	Logic 0 = HIGH (H)

EXAMPLE

Truth Table

Inputs A	Inputs B	Output X
0	0	0
1	0	0
0	1	0
1	1	1

Symbol

Function Table

Inputs A	Inputs B	Output X
L	L	L
H	L	L
L	H	L
H	H	H

Inputs A	Inputs B	Output X
0	0	0
1	0	0
0	1	0
1	1	1

Inputs A	Inputs B	Output X
H	L	H
L	L	H
H	H	H
L	H	L

B. DRAWING PRACTICE

Any of the symbols from Tables I and II may be used in diagrams, bearing in mind the following general rule.
Every signal line shall preferably have at each end
either a state indicator circle,
or no state indicator circle.
An example showing how compliance with this rule can be achieved is given in the following sketch.

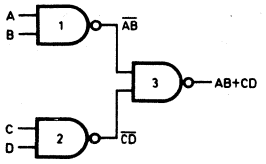


fig. 1

should be drawn as

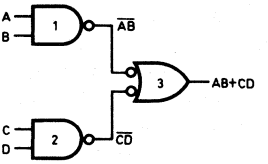


fig. 2

A further advantage of drawing the symbol of gate 3 as in fig. 2 is that it is more apparent that it behaves as an OR function than when drawn as in fig. 1 (cf. table I).

When state indicators are not used no more than four input lines should be drawn at the input side of the symbol (see fig. 3).

When state indicators are used no more than three input lines should be drawn at the input side (see fig. 4).
Following these rules will help to avoid unnecessary crowding of lines in the drawing.
When more input lines are needed the input side of the symbol can be extended in any of the ways indicated in fig. 5.

fig. 3

fig. 4

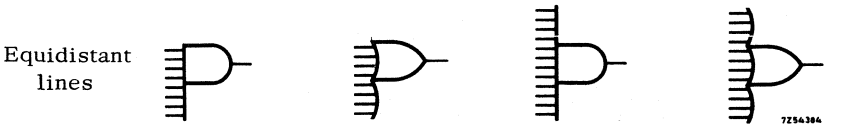


fig. 5

EXTENDED INPUTS

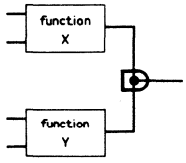
If the number of inputs to an expandable gate is extended by means of an expander circuit, the output line(s) of the expander is (are) connected to the specific expansion input(s) of the gate as drawn below.
The expander symbol shall be drawn to the same dimensions as the gate symbol; however, two filled arrows shall be drawn on each connection line, one arrow close to the expander symbol and another close to the gate symbol.

f = gate
E = expander

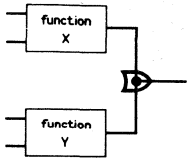
A signal line provided with arrows need not imply the usual logic levels. Generally it should not be connected to "normal" inputs or outputs of gates.

C. **OUTPUT COMBINATIONS** (6.3)

Where functions have the capability of being combined according to the AND (or OR) function, simply by having the outputs connected, that capability shall be shown by enveloping the branched connection with a smaller sized AND or OR symbol .



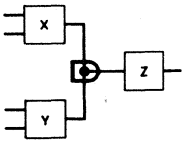
Dot "AND"



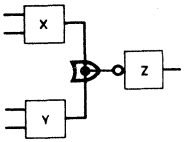
Dot "OR"

Note: These connections of outputs are often described in the literature as "WIRED-OR".

EXAMPLES



The function Z is activated on its input by a HIGH level (because a state indicator is not applied there) if and only if both outputs of functions X and Y are HIGH.
The branched connection shall therefore be enveloped by a small-sized AND symbol.

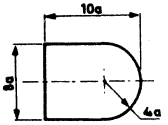


The function Z is activated on its input by a LOW level (because a state indicator is applied there) if and only if one or both outputs of the functions X and Y are LOW.
The branched connection shall therefore be enveloped by a small-sized OR symbol.
It should be noted that it would seem necessary to use state indicators on all terminals of the Dot "OR" symbol for correct interpretation of the circuit. However it is not usual to use state indicators on Dot symbols.

APPENDIX

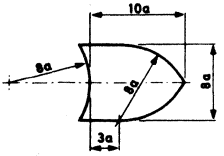
DRAWING DIMENSIONS

Ratio of dimensions of symbols may be derived from the drawings shown.

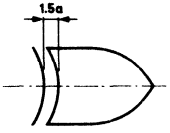


AND

Symbols enveloping a branched connection shall have half the dimensions of the fundamental symbols.



OR

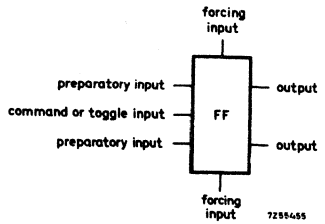


EXCLUSIVE-OR

STATE INDICATOR

FLIP-FLOP SYMBOLS

1. GENERAL SYMBOL



2. DEFINITIONS

Active or "1" state of an input signal.

That state (either a level or a transition from one level to the other) which causes, directly or indirectly, a change of the output state. Conversely, the inactive or "0" state of an input signal is that state which does not cause an output change.

Output state.

There may be one output terminal (Q) or two (Q_1 and Q_2). If there are two, the "output state" refers to the states of the signals at Q_1 and Q_2; since these are normally complementary, the state at Q_1 is usually considered to represent the output state.

Preparatory input terminal (e.g. J, K, D)

An input terminal to which application of an active signal does not directly cause a change of the output state but prepares the circuit for such a change.

Command input terminal (T)

An input terminal to which application of an active signal causes the output to assume the state corresponding to the preparatory inputs. It is also known as the "clock input terminal".

Toggle input terminal (T)

An input terminal at which an active transition from one level to the other directly causes a change of the output state.

Forcing input terminal (S_1 = "direct set", S_2 = "direct reset")

An input terminal at which application of an active signal directly causes the output to assume a specific state, irrespective of the states of other input terminals.

3. LOCATION OF TERMINALS AND USE OF POLARITY STATE INDICATOR, SHOWN BY EXAMPLES

Legend:

H = HIGH level

L = LOW level

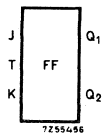
L→H = transition from LOW level to HIGH level

H→L = transition from HIGH level to LOW level

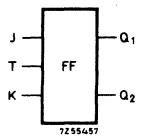
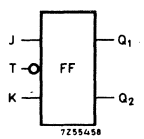
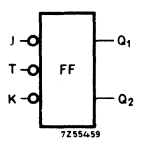
X = state (level or transition) has no influence

? = indeterminate, unless exact timing of relevant input signals (e.g. S_1 and S_2) is known.

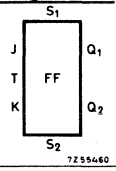
3.1. JK flip-flop without forcing inputs



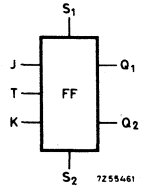
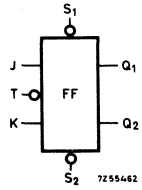
An active ("1") signal at J, together with an **inactive ("0") signal** at K and an active signal transition at T, causes the "1" state at Q_1 and the "0" state at Q_2.

Symbol	Function table			
	J	K	T	Q_1 Q_2
	H	L	L→H	H L
	L	H	L→H	L H
	H	H	L→H	reversed
	L	L	L→H	no change
	X	X	H→L	no change
	H	L	H→L	H L
	L	H	H→L	L H
	H	H	H→L	reversed
	L	L	H→L	no change
	X	X	L→H	no change
	L	H	H→L	H L
	H	L	H→L	L H
	L	L	H→L	reversed
	H	H	H→L	no change
	X	X	L→H	no change

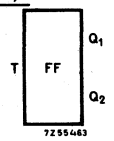
3.2. JK flip-flop with forcing inputs



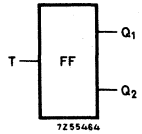
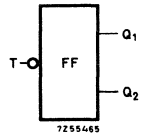
Irrespective of the states at J, K and T: an active ("1") signal at S_1, together with an inactive ("0") signal at S_2, causes Q_1 to assume the "1" and Q_2 the "0" state

Symbol	Function table						
	J	K	T	S_1	S_2	Q_1	Q_2
	X	X	X	H	L	H	L
	X	X	X	L	H	L	H
	X	X	X	H	H	?	?
	H	L	L→H	L	L	H	L
	L	H	L→H	L	L	L	H
	H	H	L→H	L	L	reversed	
	L	L	L→H	L	L	no change	
	X	X	H→L	L	L	no change	
	X	X	X	L	H	H	L
	X	X	X	H	L	L	H
	X	X	X	L	L	?	?
	H	L	H→L	H	H	H	L
	L	H	H→L	H	H	L	H
	H	H	H→L	H	H	reversed	
	L	L	H→L	H	H	no change	
	X	X	L→H	H	H	no change	

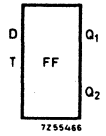
3.3. T flip-flop ("Toggle")



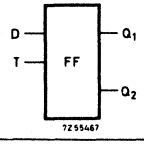
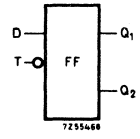
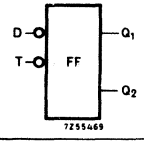
An active ("1") signal transition at T causes the complementary states at Q_1 and Q_2 to reverse.

Symbol	Function table	
	T	Q_1 Q_2
	L→H	reversed
	H→L	no change
	H→L	reversed
	L→H	no change

3.4. Edge-triggered D flip-flop

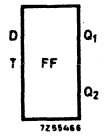


An active ("1") signal transition at T causes Q_1 to assume the same state as D. I.e., if D is in the "1" state during the active transition at T, Q_1 also assumes the "1" state: if D is "0", Q_1 also becomes "0". The output state will remain unchanged until the next active transition at T occurs.

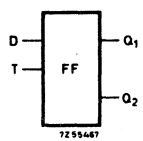
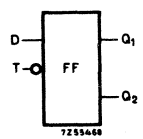
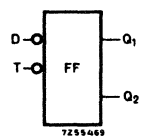
Symbol	Function table			
	D	T		Q_1 Q_2
		level	transition	
	H		L→H	H L
	L		L→H	L H
	X	X		no change
	X		H→L	no change
	H		H→L	H L
	L		H→L	L H
	X	X		no change
	X		L→H	no change
	L		H→L	H L
	H		H→L	L H
	X	X		no change
	X		L→H	no change

3.5. Level-operated ("gated") D flip-flop, or "Bistable latch".

(Graphical symbol equal to 3.4.)

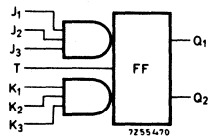


As long as the signal at T is at its active ("1") level, the signal at Q_1 follows the signal at D. When the signal at T changes to its inactive ("0") level, the signal at Q_1 latches (Subsequent changes in D cause no change in Q_1). Q_1 unlatches when the signal at T returns to its active level.

Symbol	Function table			
	D	T		Q_1 Q_2
		level	subsequent transition	
	H	H		H L
	H	H	H→L	H L
	L	H		L H
	L	H	H→L	L H
	X	L		no change
	H	L		H L
	H	L	L→H	H L
	L	L		L H
	L	L	L→H	L H
	X	H		no change
	L	L		H L
	L	L	L→H	H L
	H	L		L H
	H	L	L→H	L H
	X	H		no change

4. MULTIPLE INPUTS

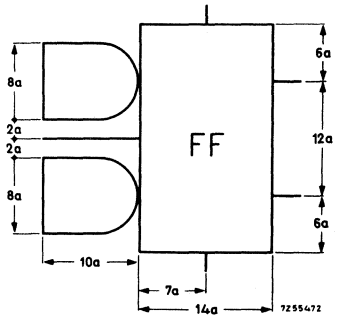
Where inputs are functionally combined by an input gate, the connecting line between the gate symbol and the flip-flop symbol may conveniently be omitted, as shown in the drawing.



5. TIME DELAY CIRCUIT

The following time delay symbol (MIL-STD-806 B, 5.15) is used in some logic flip-flop block diagrams:

6. DRAWING DIMENSIONS (to MIL-STD-806 B)



The ratio of dimensions is given in the drawing above.

For dimensions of gates and state-indicators see "Appendix", page 8.

RATING SYSTEMS

ACCORDING TO I.E.C. PUBLICATION 134

1. DEFINITIONS OF TERMS USED

1.1 Electronic device. An electronic tube or valve, transistor or other semiconductor device.
Note: This definition excludes inductors, capacitors, resistors and similar components.

1.2 Characteristic. A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

1.3 Bogey electronic device. An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

1.4 Rating. A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.
Note: Limiting conditions may be either maxima or minima.

1.5 Rating system. The set of principles upon which ratings are established and which determine their interpretation.
Note: The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

2. ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

p.t.o.

The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

3. DESIGN MAXIMUM RATING SYSTEM

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout life, no design maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

4. DESIGN CENTRE RATING SYSTEM

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

NOTE

It is common use to apply the Absolute Maximum System in semiconductor published data.

LETTER SYMBOLS
FOR DIGITAL INTEGRATED CIRCUITS

(Additional symbols for MOS circuits on page 4)

1. General

The voltages and currents are related to the terminals to which they are applied or at which they appear. Each terminal is indicated by a letter relating to the function of the device or the function of the pertinent signal.
In order to avoid confusion by any ambiguity in logical conventions, signal levels are indicated by H (= HIGH, for the more positive potential) and L (= LOW, for the less positive potential). Where circuit functions or logical equations are involved, the logical convention is mentioned specifically (for positive logic: H = 1, and for negative logic: H = 0).

2. Terminal designations

D = D input of D type latch flip-flops
E = expander input (if necessary, this letter may be followed by an index, e.g. E_1 or E_2 or by one of the input letters, such as EG = gate expander input)
G = gate input
J, K = J, K input of JK flip-flops
N = negative supply
P = positive supply
Q = output
S = direct SET input
T = trigger (or toggle) input
Ø = common supply return and voltage reference

3. Subscript sequence for voltages and currents

First subscript : terminal designation letter.
Second subscript: H (for HIGH) or L (for LOW), if applicable.
Third subscript : min or max, if applicable.
Examples: V_P, I_{QL}, V_{QHmin}, I_{PH} (in the latter case H denotes that the output level is HIGH).

4. Polarity of current and voltage

A current is defined as positive when its conventional direction of flow is into the device.
Unless otherwise specified, a voltage is measured with respect to the reference terminal (Ø). Its polarity is defined as positive when the potential is higher than that of the reference terminal.

5. Time designations

If required for reasons of unambiguity, the related terminals may be included in the designations given below (e.g. t_{fQ1}).

t_f = fall time (transition from HIGH to LOW, see Fig. 1)

t_H = signal HIGH duration (Fig. 1)

t_L = signal LOW duration (Fig. 1)

t_{pd} = average propagation delay time, defined as $\frac{t_{pdr} + t_{pdf}}{2}$

t_{pdf} = fall propagation delay time (output voltage falling, see Fig. 2)

t_{pdr} = rise propagation delay time (output voltage rising, see Fig. 2)

t_r = rise time (transition from LOW to HIGH, see Fig. 1)

t_{sc} = duration of short circuit (from relevant terminal to common return terminal)

V_{pd} = reference voltage level for propagation delay measurement

Fig. 1.

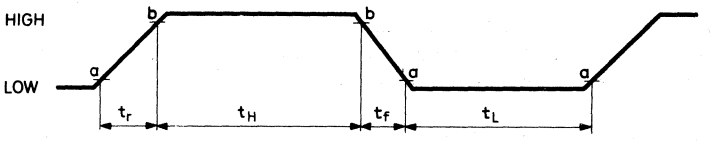
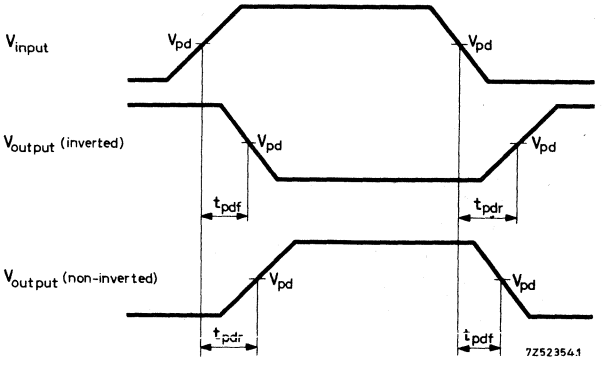


Fig. 2.



6. Other designations

i.c. = internally connected
Terminals with this indication should be left open. Otherwise correct working cannot be ensured; the device may even be damaged

n.c. = not connected internally
It is recommended not to use these terminals for any connection

I_P = supply current
The logic state of the device indicated by H or L is normally referred to the output level, unless otherwise specified

I_{Pmax} = supply current
Maximum d.c. value under defined conditions

M = d.c. noise margin

M_L = d.c. noise margin, signal level LOW
(defined as: $M_L = V_{GLmax} - V_{QLmax}$ under defined loading, temperature and supply voltage conditions)

M_H = d.c. noise margin, signal level HIGH
(calculated from: $M_H = V_{QHmin} - V_{GHmin}$ under defined loading, temperature and supply voltage conditions)

N_a = available d.c. fan-out (defined as: $N_a = \frac{I_{QLmax}}{-I_{GLmax}}$ under defined temperature and supply voltage conditions)

P_H; P_L = power consumption, defined as the product of the supply current(s) and of the corresponding supply voltage(s). The logical state of the device, indicated by a letter index H or L, is normally referred to the output level, unless otherwise specified

P_{av} = average power consumption at 50% duty cycle, unless otherwise specified. It is defined as: $P_{av} = V_P \cdot \frac{I_{PH} + I_{PL}}{2}$

P_{tot} = power dissipation, defined as the total power dissipated by the device. It is the sum of the products of all currents and voltages at each of the input, output and supply terminals, their polarities being taken into account. The logical state of the device indicated by a letter index H or L is normally referred to the output level, unless otherwise specified

T_{amb} = operating ambient temperature, i.e. the temperature of the free air in which the normally operating device is placed without external heat conduction, unless otherwise specified

T_{stg} = storage temperature, i.e. the temperature of the ambient medium in which the non-operating device is stored

V_{GLmax} = input voltage LOW at terminal G. With the specified level applied to the input of an inverting gate the output level will not be lower than the specified value V_{QHmin} at given I_{QH}.

V_{GHmin} = input voltage HIGH at terminal G, With the specified level applied to the input of an inverting gate the output level will not exceed the specified value V_{QLmax} at given I_{QL}.

ΔV_Q = change of output voltage caused by a specified change of output current

ADDITIONAL SYMBOLS FOR MOS CIRCUITS

2a. Terminal designations

I = shift register input
A = address input or decode matrix input
ϕ = clock input
WC = write control input
D = data input
CD = chip disable input
Q = output
C = chip inhibit input
P_o = common supply return and voltage reference
P_1, P_2, etc. = supply input

3a. Subscript sequence for voltages
First (with or without second) subscript: terminal designation
Second or third subscript: H (HIGH) or L (LOW) if applicable

5a. Time designations

Details are described in the data sheets

6a. Other designations

M_L = d.c. noise margin LOW ($M_L = V_{input\ L\ max} - V_{output\ L\ max}$)
M_H = d.c. noise margin HIGH($M_H = V_{output\ H\ min} - V_{input\ H\ min}$)
R_{QH} = output resistance HIGH
R_{QL} = output resistance LOW
P_{av} = average power consumption

DTL

FC family

FCH101	single 8-input NAND gate, without R_C
FCH111	single 8-input NAND gate, with R_C
FCH121	dual 4-input NAND gate, without R_C
FCH131	dual 4-input NAND gate, with R_C
FCH141	triple 3-3-2-input NAND gate, without R_C
FCH151	triple 3-input NAND gate, without R_C
FCH161	triple 3-3-2-input NAND gate, with R_C
FCH171	triple 3-input NAND gate, with R_C
FCH181	quadruple 2-input NAND gate, without R_C
FCH191	quadruple 2-input NAND gate, with R_C
FCH201	sextuple INVERTER, without R_C
FCH211	sextuple INVERTER, with R_C
FCH221	dual 3-input LINE DRIVER NAND gate
FCH231	dual 4-input LINE DRIVER NAND gate
FCH281	single 5-bit COMPARATOR
FCH291	single 10-bit PARITY CHECKER
FCH301	single 4-bit DECODER
FCH311	sextuple expandable INVERTER, without R_C
FCH321	sextuple expandable INVERTER, with R_C
FCJ101	single JK FLIP-FLOP
FCJ111	single JK master-slave FLIP-FLOP
FCJ121	dual JK master-slave FLIP-FLOP
FCJ131	dual JK master-slave FLIP-FLOP
FCJ141	single asynchronous 10-COUNTER
FCJ191	dual JK master-slave FLIP-FLOP (common set input; separate reset inputs)
FCJ201	single JK master-slave FLIP-FLOP (AND inputs)
FCJ211	dual JK master-slave FLIP-FLOP (common clock input and common set input; separate reset inputs)
FCJ221	quadruple latch FLIP-FLOP (common clock input and common set input)
FCK111	monostable MULTIVIBRATOR
FCL101	level DETECTOR
FCY101	triple gate EXPANDER

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

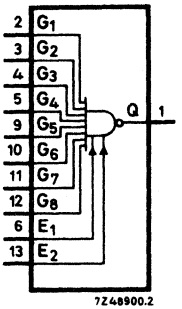
NAND GATES

	non-R_c	R_c
Single 8-input NAND gate	FCH101	FCH111
Dual 4-input NAND gate	FCH121	FCH131
Triple 3-3-2-input NAND gate	FCH141	FCH161
Triple 3-input NAND gate	FCH151	FCH171
Quadruple 2-input NAND gate	FCH181	FCH191
Sextuple inverter	FCH201	FCH211

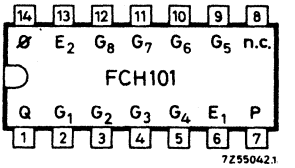
QUICK REFERENCE DATA					
Supply voltage		V_P	6.0 ± 5%		V
Operating ambient temperature range		T_{amb}	0 to +75		°C
Average propagation delay time N = 6, C_W = 60 pF, T_{amb} = 25 °C		t_{pd}	typ.	30	ns
Available d.c. fan out T_{amb} = 0 to +75 °C		N_a	⩾	8	
D.C. noise margin T_{amb} = 25 °C		M_L	typ.	1.2	V
Power consumption per gate 50% duty cycle, T_{amb} = 25 °C	non-R_c gate	P_{av}	typ.	7	mW
	R_c gate	P_{av}	typ.	11	mW

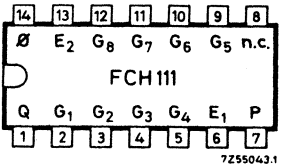
The FC family includes twelve NAND packages offering a wide selection of circuit configurations. It includes gate types with as well as without a collector resistor, ensuring optimum equipment design.
The fan-in of the circuits can easely be expanded by means of a diode array.
The outputs of these gates may be interconnected to perform the AND-OR-NOT function.

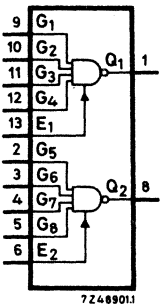
PACKAGE OUTLINE: 14 lead plastic dual in-line (type A). (See General Section)



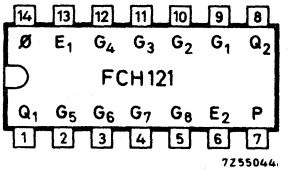
FCH101 (non-R_C)
FCH111 (R_C)

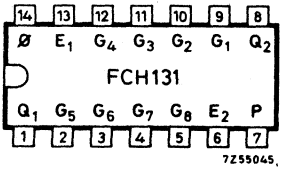


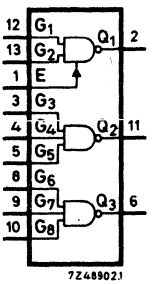




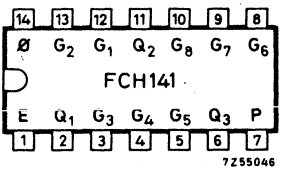
FCH121 (non-R_C)
FCH131 (R_C)

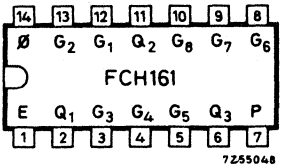


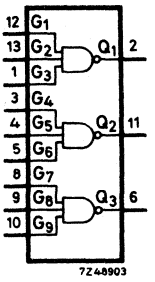




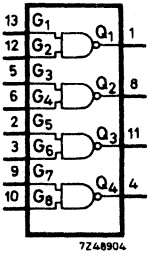
FCH141 (non-R_C)
FCH161 (R_C)



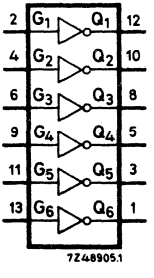




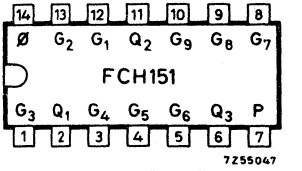
FCH151 (non-R_C)
FCH171 (R_C)

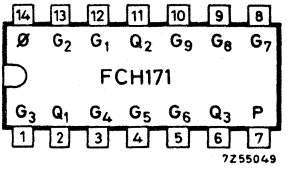


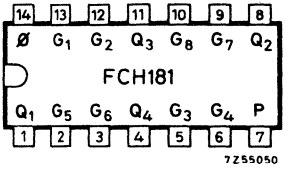
FCH181 (non-R_C)
FCH191 (R_C)

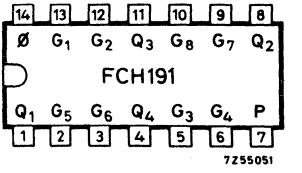


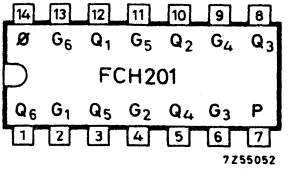
FCH201 (non-R_C)
FCH211 (R_C)

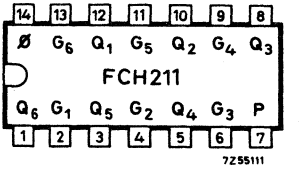






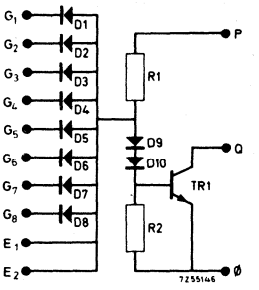




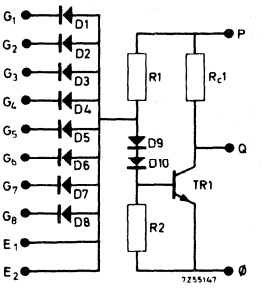


CIRCUIT DIAGRAMS

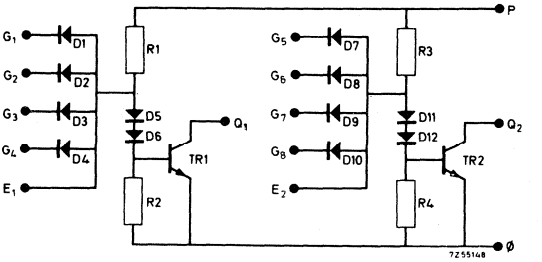
FCH101



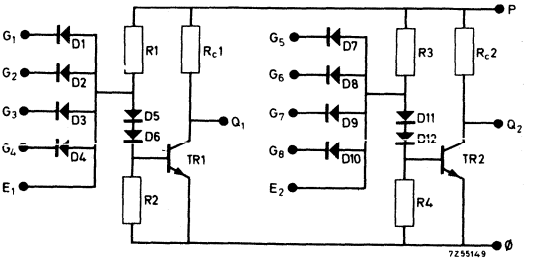
FCH111



FCH121

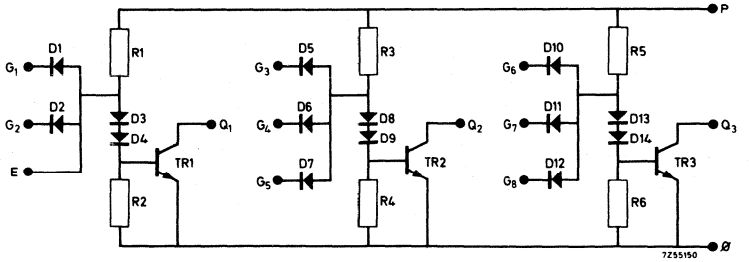


FCH131

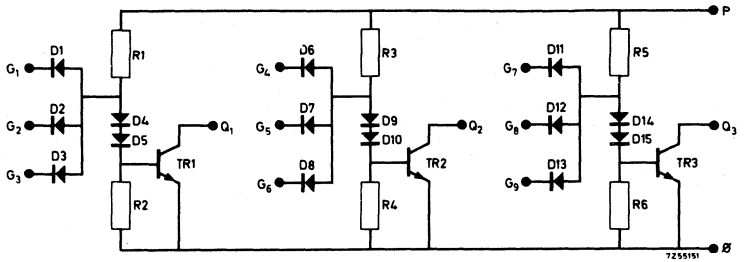


CIRCUIT DIAGRAMS (continued)

FCH141



FCH151



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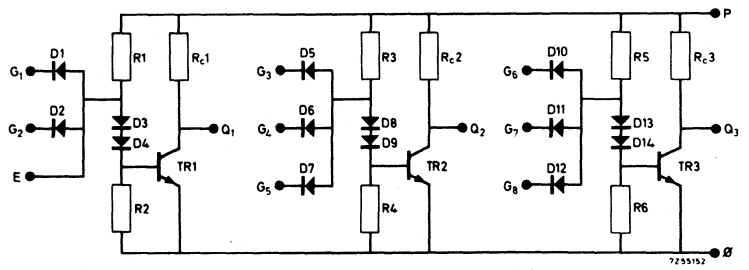

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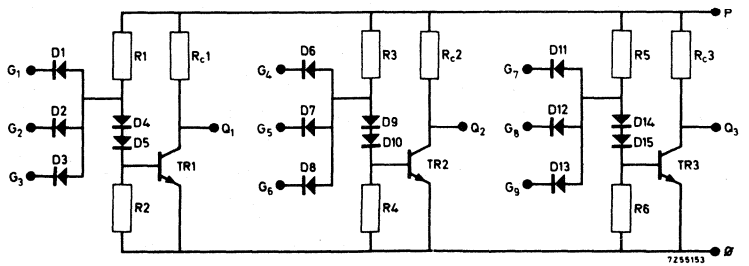
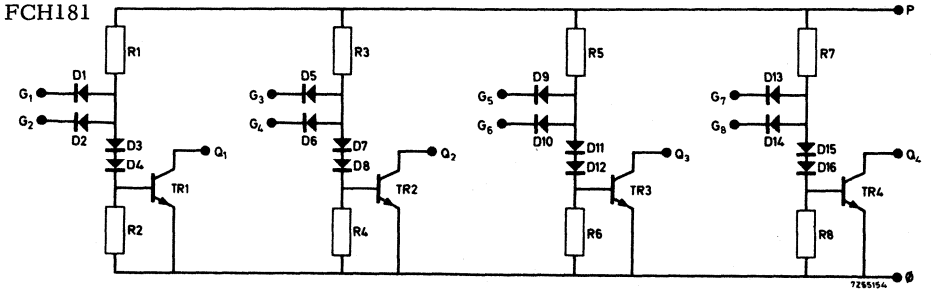
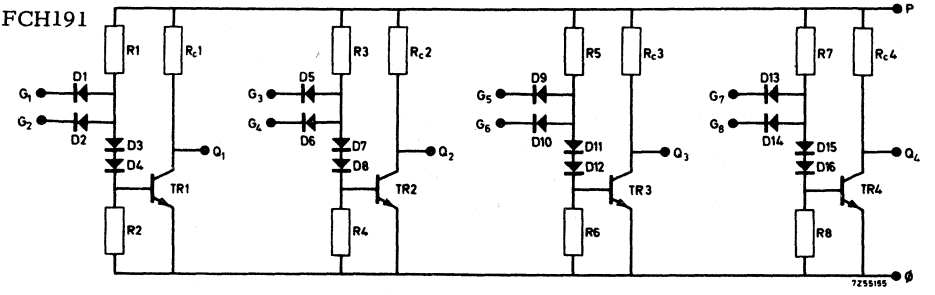


CIRCUIT DIAGRAMS (continued)

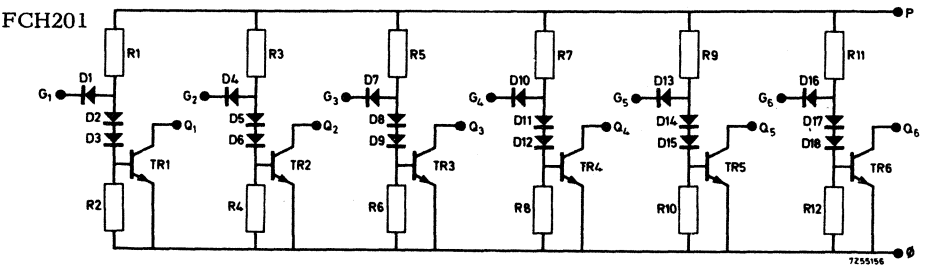
FCH181



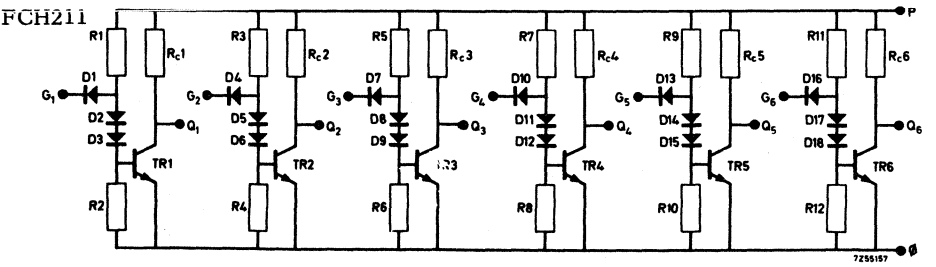
FCH191



FCH201



FCH211



LOGIC FUNCTION

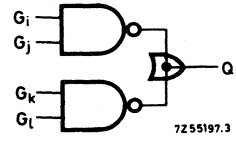
1. Individual gate operation

$Q = \overline{G_i \cdot G_j}$ for positive logic

Function table

G_i	G_j	Q
L	X	H
X	L	H
H	H	L

2. Commoned gate operation



Function table

G_i	G_j	G_k	G_l	Q
L	X	L	X	H
L	X	X	L	H
X	L	L	X	H
X	L	X	L	H
H	H	X	X	L
X	X	H	H	L

$Q = (\overline{G_i \cdot G_j}) \cdot (\overline{G_k \cdot G_l}) = \overline{(G_i \cdot G_j) + (G_k \cdot G_l)}$ for positive logic

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

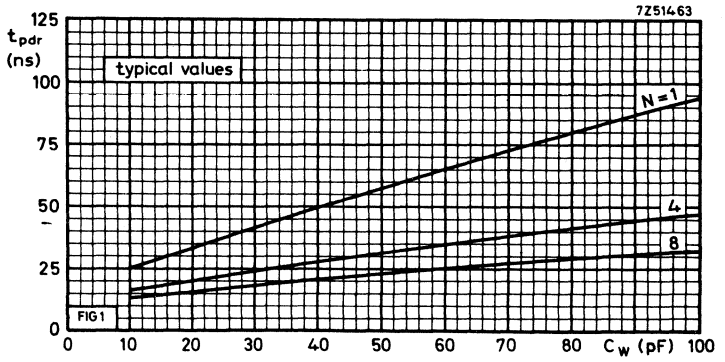
RATINGS (Limiting values) [1]

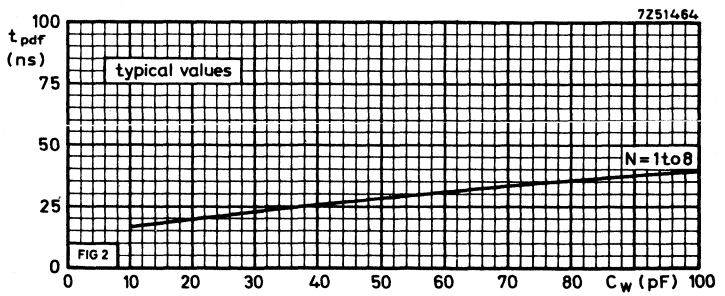
Supply voltage	V_P	max.	8.0	V
Output voltage	V_Q	max.	8.0	V
Input voltage	V_G	max.	8.0	V
Output current [2]	$-I_Q$	max.	20	mA
Input current [3]	$-I_G$	max.	20	mA
Voltage difference between any two inputs		max.	8.0	V
Expander input voltages				
with respect to supply	$V_P - V_E$	max.	8.0	V
with respect to other inputs	$V_G - V_E$	max.	8.0	V
Expander input current	I_E	max.	5.0	mA
Storage temperature	T_{stg}	−55 to	+125	°C
Operating ambient temperature	T_{amb}	0 to	+75	°C

[1] Limiting values according to the Absolute Maximum System as defined in IEC publication 134.
[2] For negative output voltage.
[3] At this limit, input voltage type.: −1.5 V.

SYSTEM DESIGN DATA (both non-R_c and R_c)

Uniform system temperature		T_{amb}	0 to +75	°C
Uniform system supply voltage		V_P	5.7 to 6.3	V
Available d.c. fan out		N_a	≥ 8	
D.C. noise margin		M_L	min. 0.4	V
		M_H	min. 1.8	V
Average propagation delay time		t_{pd}	max. 75	ns
Equivalent input capacitance		C_G	typ. 4	pF
Equivalent output capacitance		C_Q	typ. 10	pF
Supply current per gate (duty cycle 50%)	non-R_c	I_{Pav}	typ. 1.20	mA
	R_c	I_{Pav}	typ. 1.75	mA
Power dissipation at T_{amb} = 75 °C (each gate)	non-R_c	P_{tot}	max. 17.5	mW
	R_c	P_{tot}	max. 22	mW





CHARACTERISTICS of non-R_c gates

		T_{amb} (°C)				Conditions and references	
		0	+25	+75		V_P (V)	
STATIC DATA							
Output voltage LOW	V_{QLmax}	0.4	0.4	0.4	V	5.7 and 6.3	
at: Output current LOW	I_{QLmax}	16.0 18.0	15.1 17.0	14.2 16.0	mA mA	5.7 6.3	
and at: Input voltage HIGH	V_{GHmin}	2.3	2.2	2.1	V	5.7 and 6.3	
Input current LOW	$-I_{GLmax}$	1.75 2.0	1.65 1.9	1.55 1.8	mA mA	5.7 6.3	V_G = 0.4 V; other inputs floating
Input current HIGH	I_{GHmax}	1.0	1.0	25	μA	5.7	V_G = 5.3 V other inputs 0 V
Output current HIGH	I_{QHmax}	70	70	70	μA	5.7 and 6.3	V_Q = 5.3 V
at: Input voltage LOW	V_{GLmax}	1.0	1.0	0.8	V	5.7 and 6.3	
Supply current [1]	I_{Pmax}	2.0	1.9	1.8	mA	6.3	G inputs LOW
DYNAMIC DATA							
Rise propagation delay time	t_{pdrmax}	-	85	-	ns	6.0	V_{pd} = 1.5 V N = 1; C_L = 40 pF
	t_{pdrmax}	-	70	-	ns	6.0	V_{pd} = 1.5 V N = 6; C_L = 60 pF
Fall propagation delay time	t_{pdfmax}	-	65	-	ns	6.0	V_{pd} = 1.5 V N = 1; C_L = 40 pF
	t_{pdfmax}	-	85	-	ns	6.0	V_{pd} = 1.5 V N = 6; C_L = 60 pF

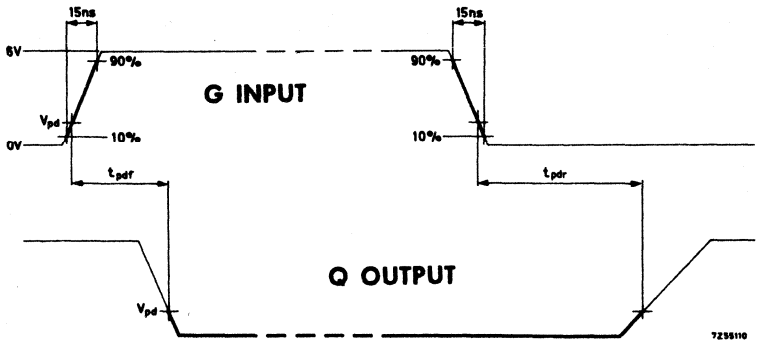
[1]) per gate

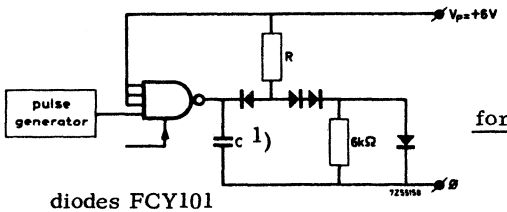
CHARACTERISTICS of R_C-gates

		T_{amb} (°C)				Conditions and references	
		0	+25	+75		V_P (V)	
STATIC DATA							
Output voltage LOW	V_{QLmax}	0.4	0.4	0.4	V	5.7 and 6.3	
at: Output current LOW	I_{QLmax}	14.0	13.2	12.4	mA	5.7	
		16.0	15.2	14.4	mA	6.3	
and at: Input voltage HIGH	V_{GHmin}	2.3	2.2	2.1	V	5.7 and 6.3	
Output voltage HIGH	V_{QHmin}	5.3	5.3	5.3	V	5.7	I_Q = 0
		4.1	4.1	3.9	V	5.7	I_Q = −200 μA
at: Input voltage LOW	V_{GLmax}	1.0	1.0	0.8	V	5.7 and 6.3	
Input current LOW	$-I_{GLmax}$	1.75	1.65	1.55	mA	5.7	V_G = 0.4 V; other inputs floating
		2.0	1.9	1.8	mA	6.3	
Input current HIGH	I_{GHmax}	1.0	1.0	25	μA	5.7	V_G = 5.3 V other inputs 0 V
Output current LOW (AND-OR-NOT function)	$-I_{QLLmax}$	2.2	2.1	2.0	mA	6.3	$V_G = V_{QLmax}$ Output forced LOW externally to V_Q = 0.4 V
Supply current	I_{Pmax}	4.2	3.8	3.6	mA	6.3	G inputs HIGH
DYNAMIC DATA							
Rise propagation delay time	t_{pdrmax}	-	85	-	ns	6.0	V_{pd} = 1.5 V N = 1; C_L = 40 pF
	t_{pdrmax}	-	70	-	ns	6.0	V_{pd} = 1.5 V N = 6; C_L = 60 pF
Fall propagation delay time	t_{pdfmax}	-	65	-	ns	6.0	V_{pd} = 1.5 V N = 1; C_L = 40 pF
	t_{pdfmax}	-	85	-	ns	6.0	V_{pd} = 1.5 V N = 6; C_L = 60 pF

CHARACTERISTICS (continued)

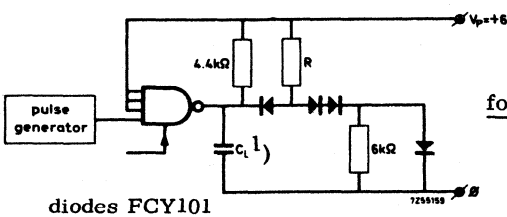
DYNAMIC DATA





diodes FCY101

for R_c gates



diodes FCY101

for non-R_c gates

Waveforms and loading circuits, illustrating measurement of t_{pdr} and t_{pdf}.

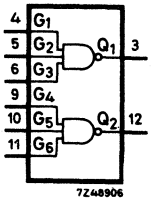
Equivalent load for N = 1 and C_L = 40 pF when R = 4 kΩ

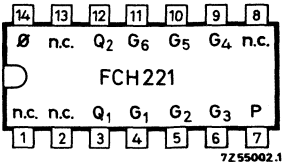
N = 6 and C_L = 60 pF when R = 670 Ω

1) Including probe and jig capacitance.

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

DUAL 3-INPUT LINE DRIVER NAND GATE



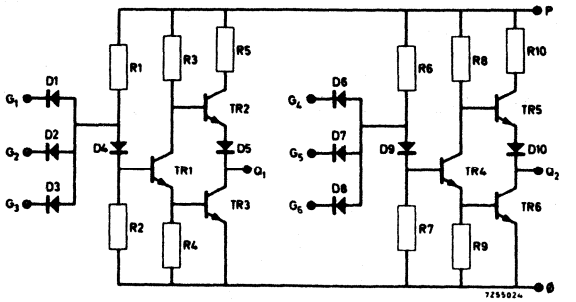


QUICK REFERENCE DATA			
Supply voltage	V_P	6.0 ± 5%	V
Operating ambient temperature range	T_{amb}	0 to +75	°C
Average propagation delay time N = 15, C_w = 250 pF, T_{amb} = 25 °C	t_{pd}	typ. 35	ns
Available d.c. fan-out T_{amb} = 0 to +75 °C	N_a	≥ 14	
D.C. noise margin T_{amb} = 25 °C	M_L	typ. 1.2	V
Power consumption per gate 50% duty cycle, T_{amb} = 25 °C	P_{av}	typ. 11	mW

The FCH221 comprises two independent NAND gates incorporating bi-directional output circuitry for achieving high fan-out and for driving large capacitive loads. Typical applications are in parallel setting of registers, shift pulse driving and driving of long lines.

PACKAGE OUTLINE : 14 lead plastic dual in-line (type A). (See General Section)

CIRCUIT DIAGRAM



LOGIC FUNCTION

G_1 G_4	G_2 G_5	G_3 G_6	Q_1 Q_2
L	X	X	H
X	L	X	H
X	X	L	H
H	H	H	L

$$Q_1 = \overline{G_1 \cdot G_2 \cdot G_3}$$
$$Q_2 = \overline{G_4 \cdot G_5 \cdot G_6}$$

for positive logic

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS (Limiting values) [1]

Supply voltage	V_P	max.	8.0	V
Output voltage	V_Q	max.	8.0	V
Input voltage	V_G	max.	8.0	V
Output current [2]	$-I_Q$	max.	20	mA
Input current [3]	$-I_G$	max.	20	mA
Voltage difference between any two inputs		max.	8.0	V
Storage temperature	T_{stg}	−55 to +125		°C
Operating ambient temperature	T_{amb}	0 to +75		°C
Output short-circuit duration; duty cycle 10% (either output, or both)	t_{Qsc}	max.	60	ms

1) Limiting values according to the Absolute Maximum System as defined in IEC publication 134.
2) For negative output voltage in LOW state
3) At this limit input voltage typ.: −1.5 V.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to +75	°C
Uniform system supply voltage	V_P	5.7 to 6.3	V
Available d.c. fan out	N_a	⩾ 14	
D.C. noise margin	M_L	min. 0.4	V
	M_H	min. 1.1	V
Average propagation delay time	t_{pd}	max. 113	ns
Equivalent input capacitance	C_G	typ. 7	pF
Supply current (duty cycle 50 %) [1]	I_{Pav}	typ. 3.6	mA
Power dissipation at T_{amb} = 75 °C [1]	P_{tot}	max. 65	mW

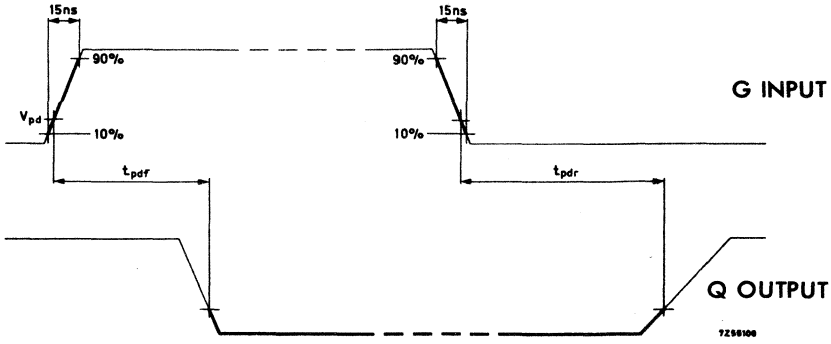
[1]) Both gates together; outputs not short-circuited.

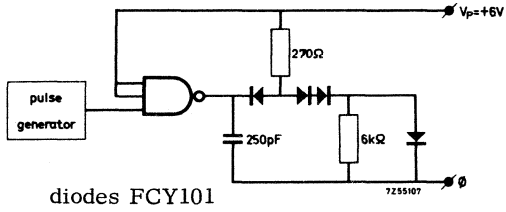
CHARACTERISTICS

		T_{amb} (°C)				Conditions and references	
		0	+25	+75		V_P (V)	
STATIC DATA							
Output voltage LOW	V_{QLmax}	0.4	0.4	0.4	V	5.7 and 6.3	
at: Output current LOW	I_{QLmax}	25 28	27 27	26 26	mA mA	5.7 6.3	
and at: Input voltage HIGH	V_{GHmin}	2.3	2.2	2.1	V	5.7 and 6.3	
Output voltage HIGH	V_{QHmin}	3.4 2.2	3.6 2.5	3.9 2.9	V V	5.7 5.7	I_Q = −30 μA I_Q = −5 mA
at: Input voltage LOW	V_{GLmax}	1.0	1.0	0.8	V	5.7 and 6.3	
Input current LOW	$-I_{GLmax}$	1.75 2.0	1.65 1.9	1.55 1.8	mA mA	5.7 6.3	V_G = 0.4 V; other inputs floating
Input current HIGH	I_{GHmax}	1.0	1.0	25	μA	5.7	$V_G = V_{QHmin}$ other inputs 0 V
Output short circuit current	$-I_{Qsc}$	16.5	19.5	18.0	mA	5.7	$V_G = V_{GLmax}$ V_Q = 0 V
Supply current (both gates together)	I_{Pmax}	–	7.5	–	mA	6.3	G inputs HIGH
DYNAMIC DATA							
Rise propagation delay time	$t_{pdr\,max}$	130	105	130	ns	6.0	V_{pd} = 1.5 V N = 15; C_L = 250 pF
Fall propagation delay time	$t_{pdf\,max}$	95	80	95	ns	6.0	V_{pd} = 1.5 V N = 15; C_L = 250 pF

CHARACTERISTICS (continued)

DYNAMIC DATA





diodes FCY101

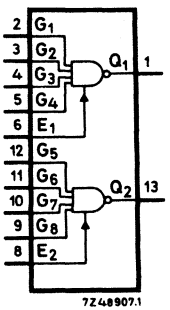
Equivalent load for N = 15 and C_L [1] = 250 pF

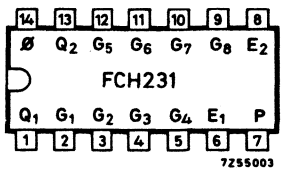
Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf}.

[1]) Including probe and jig capacitance.

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

DUAL 4-INPUT LINE DRIVER NAND GATE



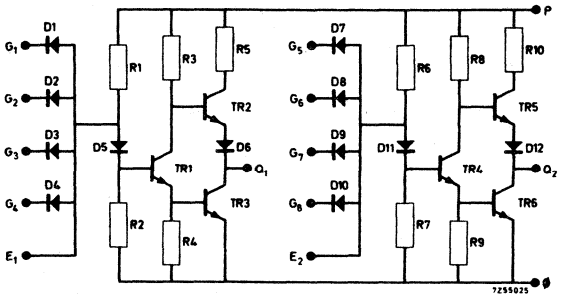


QUICK REFERENCE DATA			
Supply voltage	V_P	6.0 ± 5%	V
Operating ambient temperature range	T_{amb}	0 to +75	°C
Average propagation delay time N = 20, C_W = 250 pF, T_{amb} = 25 °C	t_{pd}	typ. 35	ns
Available d.c. fan-out T_{amb} = 0 to +75 °C	N_a	⩾ 20	
D.C. noise margin T_{amb} = 25 °C	M_L	typ. 1.2	V
Power consumption per gate 50% duty cycle, T_{amb} = 25 °C	P_{av}	typ. 11	mW

The FCH231 comprises two independent NAND gates incorporating bi-directional output circuitry for achieving very high fan-out and for driving large capacitive loads. Typical applications are in parallel setting of registers, shift pulse driving and driving of long lines.

PACKAGE OUTLINE 14 lead plastic dual in-line (type A).(See General Section)

CIRCUIT DIAGRAM



LOGIC FUNCTION

G_1 G_5	G_2 G_6	G_3 G_7	G_4 G_8	Q_1 Q_2
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

$$Q_1 = \overline{G_1 \cdot G_2 \cdot G_3 \cdot G_4 \cdot E_1}^{*}$$
$$Q_2 = \overline{G_5 \cdot G_6 \cdot G_7 \cdot G_8 \cdot E_2}^{*}$$

for positive logic

* When provided with diode

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS (Limiting values) [1]

Supply voltage	V_P	max.	8.0	V
Output voltage	V_Q	max.	8.0	V
Input voltage	V_G	max.	8.0	V
Output current [2]	$-I_Q$	max.	20	mA
Input current [3]	$-I_G$	max.	20	mA
Voltage difference between any two inputs		max.	8.0	V
Expander input voltages				
with respect to supply	$V_P - V_E$	max.	8.0	V
with respect to other inputs	$V_G - V_E$	max.	8.0	V
Expander input current	I_E	max.	5.0	mA
Storage temperature	T_{stg}	−55 to +125		°C
Operating ambient temperature	T_{amb}	0 to +75		°C
Output short-circuit duration; duty cycly 10% (either output, or both)	t_{Qsc}	max.	60	ms

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to +75		°C
Uniform system supply voltage	V_P	5.7 to 6.3		V
Available d.c. fan out	N_a	⩾	20	
D.C. noise margin	M_L	min.	0.4	V
	M_H	min.	1.2	V
Average propagation delay time	t_{pd}	max.	113	ns
Equivalent input capacitance	C_G	typ.	7	pF
Supply current (duty cycle 50 %) [4]	I_{Pav}	typ.	3.6	mA
Power dissipation at T_{amb} = 75 °C [4]	P_{tot}	max.	73	mW

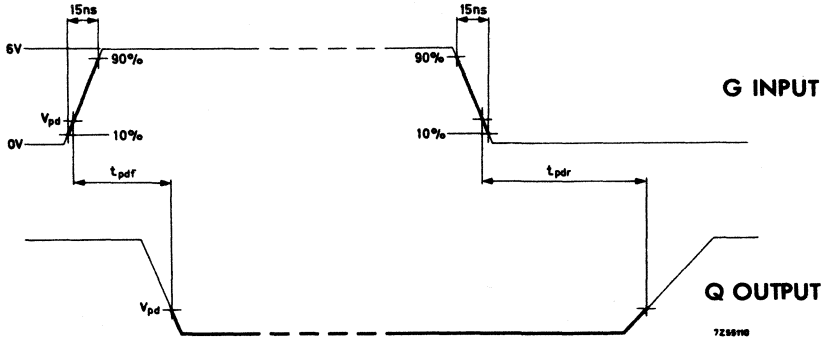
1) Limiting values according to the Absolute Maximum System as defined in IEC publication 134.
2) For negative output voltage in LOW state.
3) At this limit, input voltage typ. : −1.5V.
4) Both gates together; outputs not short-circuited.

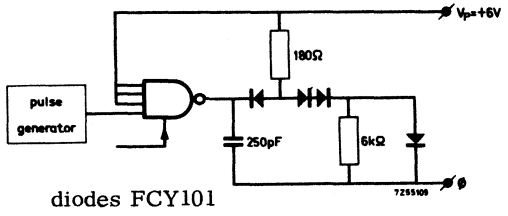
CHARACTERISTICS

		T_{amb} (°C)			Conditions and references	
		0	+25	+75	V_P (V)	
STATIC DATA						
Output voltage LOW	V_{QLmax}	0.4	0.4	0.4 V	5.7 and 6.3	
at: Output current LOW	I_{QLmax}	35	33	31 mA	5.7	
		40	38	36 mA	6.3	
and at: Input voltage HIGH	V_{GHmin}	2.3	2.2	2.1 V	5.7 and 6.3	
Output voltage HIGH	V_{QHmin}	3.5	3.7	4.0 V	5.7	I_Q = −30 μA
		2.6	2.8	2.9 V	5.7	I_Q = −5 mA
at: Input voltage LOW	V_{GLmax}	1.0	1.0	0.8 V	5.7 and 6.3	
Input current LOW	$-I_{GLmax}$	1.75	1.65	1.55 mA	5.7	V_G = 0.4 V; other inputs floating
		2.0	1.9	1.8 mA	6.3	
Input current HIGH	I_{GHmax}	1.0	1.0	25 μA	5.7	$V_G = V_{QHmin}$ other inputs 0 V
Output short circuit current	$-I_{Qscmin}$	16.5	19.5	18.0 mA	5.7	$V_G = V_{GLmax}$ V_Q = 0 V
Supply current (both gates together)	I_{Pmax}	–	7.5	– mA	6.3	G inputs HIGH
DYNAMIC DATA						
Rise propagation delay time	t_{pdrmax}	80	85	120 ns	6.0	V_{pd} = 1.5 V N = 20; C_L = 250 pF
Fall propagation delay time	t_{pdfmax}	55	50	55 ns	6.0	V_{pd} = 1.5 V N = 20; C_L = 250 pF

CHARACTERISTICS (continued)

DYNAMIC DATA





diodes FCY101

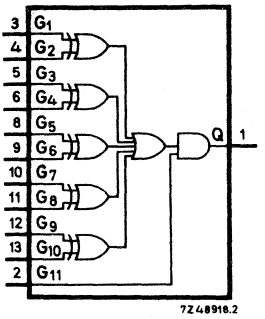
Equivalent load for N = 20 and C_L [1] = 250 pF

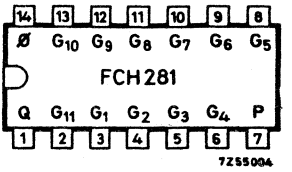
Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf}

[1] Including probe and jig capacitance.

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

SINGLE 5-BIT COMPARATOR



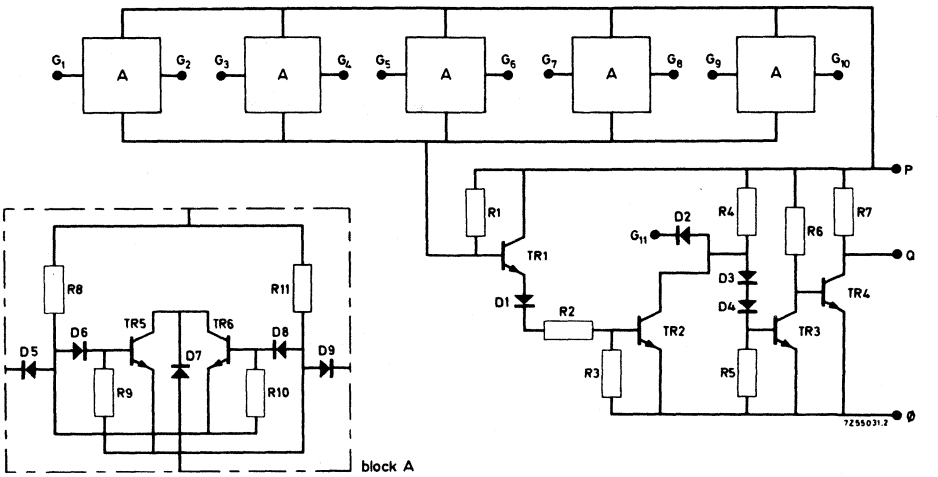


QUICK REFERENCE DATA			
Supply voltage	V_P	6.0 ± 5%	V
Operating ambient temperature range	T_{amb}	0 to +75	°C
Average propagation delay time N = 6, C_w = 60 pF, T_{amb} = 25 °C	t_{pd}	typ. 150	ns
Available d.c. fan-out T_{amb} = 0 to +75 °C	N_a	⩾ 8	
D.C. noise margin T_{amb} = 25 °C	M_L	typ. 1.2	V
Power consumption 50% duty cycle, T_{amb} = 25 °C	P_{av}	typ. 50	mW

The FCH281 comprises five exclusive-OR functions, an OR gate, and an AND gate. If on one or more pairs (G_1-G_2, --- G_9-G_{10}) one input is LOW and the other HIGH then the output will be HIGH provided G_{11} is HIGH. Otherwise the output will be LOW.

PACKAGE OUTLINE : 14 lead plastic dual in-line (type A). (See General Section)

CIRCUIT DIAGRAM



FUNCTION TABLE

G_1 G_2	G_3 G_4	G_5 G_6	G_7 G_8	G_9 G_{10}	G_{11}	Q
Equal	Equal	Equal	Equal	Equal	H	L
Unequal	X	X	X	X	H	H
X	Unequal	X	X	X	H	H
X	X	Unequal	X	X	H	H
X	X	X	Unequal	X	H	H
X	X	X	X	Unequal	H	H
X	X	X	X	X	L	L

G_1	G_2	
L	L	Equal
L	H	Unequal
H	L	Unequal
H	H	Equal

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

LOGIC FUNCTION (continued)

$$Q = \Big[\overline{(\bar{G}_1 \cdot \bar{G}_2 + G_1 \cdot G_2)} + \overline{(\bar{G}_3 \cdot \bar{G}_4 + G_3 \cdot G_4)} + \overline{(\bar{G}_5 \cdot \bar{G}_6 + G_5 \cdot G_6)} + \\ + \overline{(\bar{G}_7 \cdot \bar{G}_8 + G_7 \cdot G_8)} + \overline{(\bar{G}_9 \cdot \bar{G}_{10} + G_9 \cdot G_{10})}\Big] \cdot G_{11}.$$

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.	8.0	V
Output voltage	V_Q	max.	8.0	V
Input voltage	V_G	max.	8.0	V
Output current	$-I_Q$	max.	20	mA[1])
Input current	$-I_G$	max.	20	mA[2])
Voltage difference between any two inputs		max.	8.0	V
Storage temperature	T_{stg}	−55 to	+125	°C
Operating ambient temperature	T_{amb}	0 to	+75	°C

1) For negative output voltage.
2) At this limit input voltage typ. : −1.5 V.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to +75		°C
Uniform system supply voltage	V_P	5.7 to 6.3		V
Available d.c. fan out	N_a	⩾	8	
D.C. noise margin	M_L	min.	0.4	V
	M_H	min.	1.5	V
Average propagation delay time	t_{pd}	max.	250	ns
Equivalent input capacitance	C_G	typ.	4	pF
Supply current (duty cycle 50%)	I_{Pav}	typ.	10	mA
Power dissipation at T_{amb} = 75 °C	P_{tot}	max.	90	mW

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references	
		0	+25	+75		V_P (V)	
STATIC DATA							
Output voltage LOW	V_{QLmax}	0.4	0.4	0.4	V	5.7 and 6.3	see note 1
at: Output current LOW	I_{QLmax}	14.0 16.0	13.2 15.2	12.4 14.4	mA mA	5.7 6.3	see note 1
Output voltage HIGH	V_{QHmin}	5.3	5.3	5.3	V	5.7 and 6.3	I_Q = 0 (see note 1)
	V_{QHmin}	4.7	4.7	4.5	V	5.7	I_Q = −200 μA
Input voltage LOW	V_{GLmax}	1.0	1.0	0.8	V	5.7 and 6.3	
Input voltage HIGH	V_{GHmin}	3.0	2.8	2.5	V	5.7 and 6.3	
Input current LOW	$-I_{G1\ to\ 10\ Lmax}$	1.75	1.65	1.55	mA	5.7	$V_{G1\ to\ 10}$ = 0.4 V
	$-I_{G1\ to\ 10\ Lmax}$	2.0	1.9	1.8	mA	6.3	$V_{G1\ to\ 10}$ = 0.4 V
	$-I_{G11\ Lmax}$	1.2	1.1	1.05	mA	5.7	V_{G11} = 0.4 V
	$-I_{G11\ Lmax}$	1.35	1.25	1.20	mA	6.3	V_{G11} = 0.4 V
Input current HIGH	I_{GHmax}	1.0	1.0	25	μA	5.7	V_G = 5.3 V other inputs 0 V
Supply current	I_{Pmax}	15.3	14.5	13.5	mA	6.3	G inputs LOW

Note 1

For the proper combination of inputs to be HIGH or LOW see function table on page 2.

CHARACTERISTICS (continued)

		T_{amb} (°C) 0 +25 +75			Conditions and references		
					V_P (V)		Fig.
DYNAMIC DATA							
Propagation delay times from one G (G_1 to G_{10}) to Q							
Rise propagation delay time	t_{pdrmax}	-	200	- ns	6.0	V_{pd} = 1.5 V; N = 6 C_L = 80 pF all other inputs (including G_{11})	1; 2
Fall propagation delay time	t_{pdfmax}	-	200	- ns	6.0	at V_G = 5.3 V	
Rise propagation delay time	t_{pdrmax}	-	250	- ns	6.0	V_{pd} = 1.5 V; N = 6 C_L = 80 pF all other inputs (excluding G_{11}) at V_G = 0.4 V $V_{G_{11}}$ = 5.3 V	1; 3
Fall propagation delay time	t_{pdfmax}						
Propagation delay times from G_{11} to Q							
Rise propagation delay time	t_{pdrmax}	-	100	- ns	6.0	V_{pd} = 1.5 V; N = 6 C_L = 80 pF V_{G_1} = 0 V all other inputs at V_G = 6.0 V	1; 3
Fall propagation delay time	t_{pdfmax}	-	120	- ns	6.0		

CHARACTERISTICS (continued)

DYNAMIC DATA

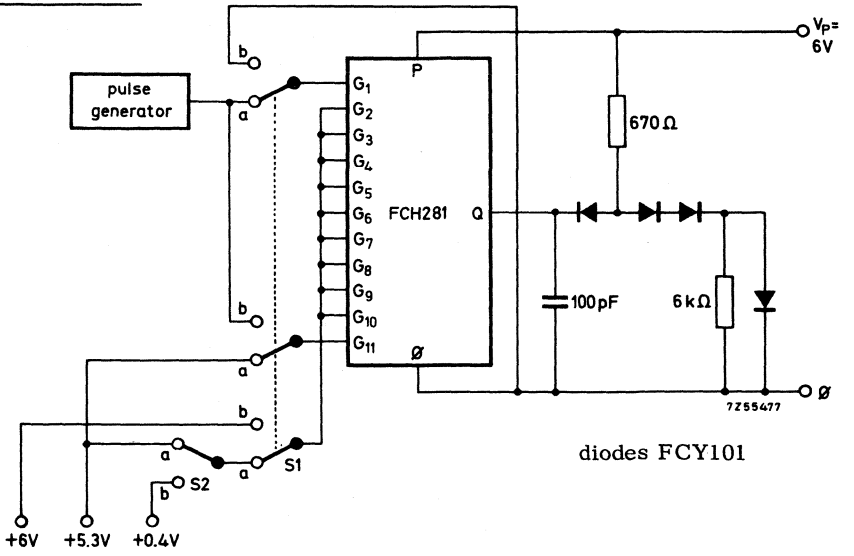


Fig. 1 Equivalent load for N = 6; C_L [1] = 80 pF

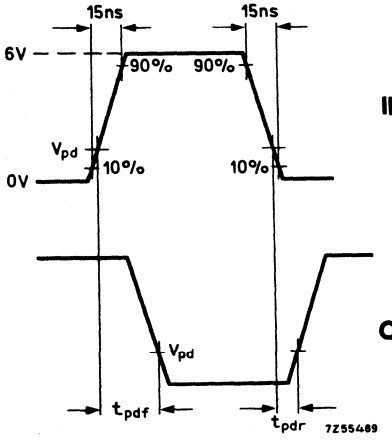


Fig. 2 Switch S1 in position a
Switch S2 in position a

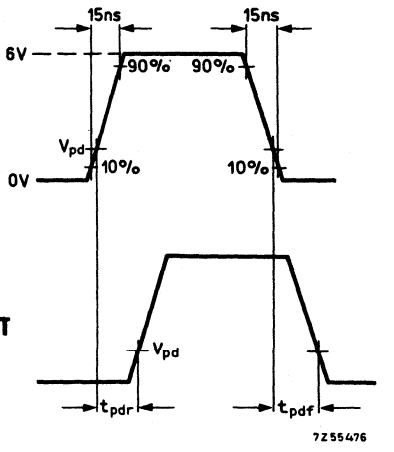


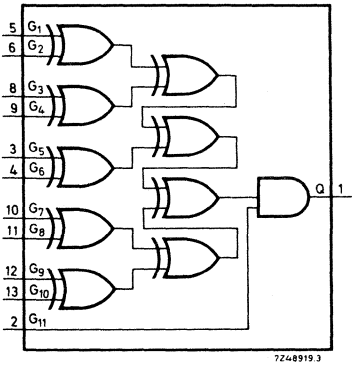
Fig. 3 Switch S1 in position a
Switch S2 in position b
or
Switch S1 in position b
Switch S2 immaterial

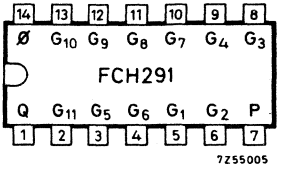
Waveforms illustrating measurement of t_{pdr} and t_{pdf}.

[1]) Including probe and jig capacitance.

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

SINGLE 10-BIT PARITY CHECKER



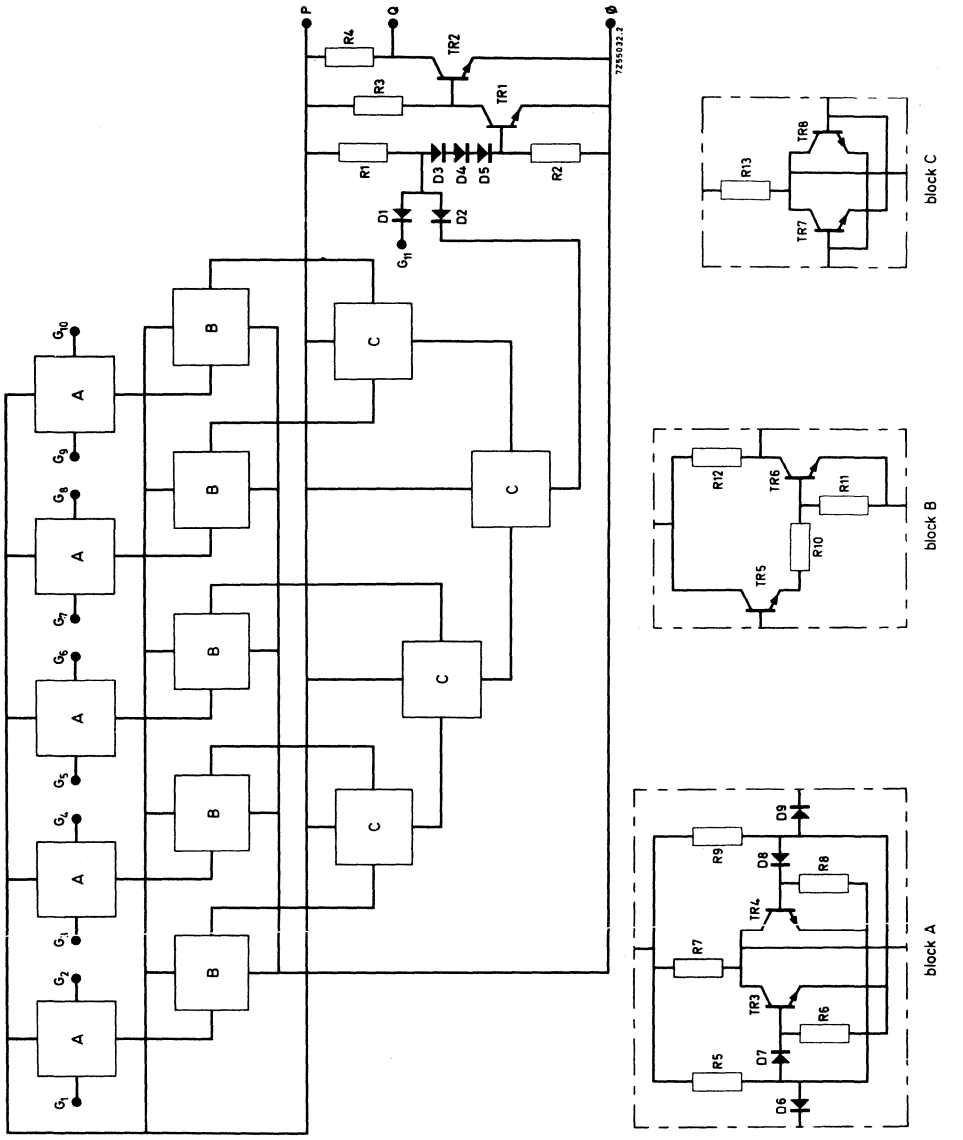


QUICK REFERENCE DATA			
Supply voltage	V_P	6.0 ± 5%	V
Operating ambient temperature range	T_{amb}	0 to +75	°C
Average propagation delay time N = 6, C_W = 60 pF, T_{amb} = 25 °C	t_{pd}	typ. 150	ns
Available d.c. fan-out T_{amb} = 0 to +75 °C	N_a	⩾ 7	
D.C. noise margin T_{amb} = 25 °C	M_L	typ. 1.2	V
Power consumption 50% duty cycle, T_{amb} = 25 °C	P_{av}	typ. 110	mW

The FCH291 comprises nine exclusive-OR functions followed by an AND gate. If an odd number of inputs (G_1 to G_{10}) are HIGH the output will be HIGH, provided G_{11} is HIGH. If an even number of inputs (G_1 to G_{10}) are HIGH the output will be LOW, provided G_{11} is HIGH. If G_{11} is LOW the output will be LOW regardless the condition of other inputs.

PACKAGE OUTLINE: 14 lead plastic dual in-line (type A). (See General Section)

CIRCUIT DIAGRAM



FUNCTION TABLE

G_1	G_2	G_3	G_4	G_5	G_6	G_7	G_8	G_9	G_{10}	G_{11}	Q
Even number of inputs HIGH										H	L
Odd number of inputs HIGH										H	H
X	X	X	X	X	X	X	X	X	X	L	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.	8.0	V
Output voltage	V_Q	max.	8.0	V
Input voltage	V_G	max.	8.0	V
Output current	$-I_Q$	max.	20	mA[1]
Input current	$-I_G$	max.	20	mA[2]
Voltage difference between any two inputs		max.	8.0	V
Storage temperature	T_{stg}	−55 to	+125	°C
Operating ambient temperature	T_{amb}	0 to	+75	°C

1) For negative output voltage.
2) At this limit input voltage typ.: −1.5 V.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to +75		°C
Uniform system supply voltage	V_P	5.7 to 6.3		V
Available d.c. fan-out	N_a	⩾	7	
D.C. noise margin	M_L	min.	0.4	V
	M_H	min.	0.8	V
Average propagation delay time	t_{pd}	max.	250	ns
Equivalent input capacitance	C_G	typ.	4	pF
Supply current (duty cycle 50%)	I_{Pav}	typ.	21	mA
Power dissipation at T_{amb} = +75 °C	P_{tot}	max.	190	mW

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references	
		0	+25	+75		V_P (V)	
STATIC DATA							
Output voltage LOW	V_{QLmax}	0.4	0.4	0.4	V	5.7 and 6.3	see note 1
at: Output current LOW	I_{QLmax}	14.0	13.2	12.4	mA	5.7	see note 1
		16.0	15.2	14.4	mA	6.3	see note 1
Output voltage HIGH	V_{QHmin}	5.3	5.3	5.3	V	5.7 and 6.3	I_Q = 0 (see note 1)
	V_{QHmin}	4.7	4.7	4.5	V	5.7	I_Q = −200 μA
Input voltage LOW	V_{GLmax}	1.0	1.0	0.8	V	5.7 and 6.3	
Input voltage HIGH	V_{GHmin}	3.8	3.8	3.4	V	5.7 and 6.3	
Input current LOW	$-I_{G1\ to\ 10\ Lmax}$	1.75	1.65	1.55	mA	5.7	$V_{G1\ to\ 10}$ = 0.4 V
		2.0	1.9	1.8	mA	6.3	$V_{G1\ to\ 10}$ = 0.4 V
	$-I_{G11max}$	1.9	1.8	1.7	mA	5.7	V_{G11} = 0.4 V
		2.1	2.0	1.9	mA	6.3	V_{G11} = 0.4 V
Input current HIGH	I_{GHmax}	1.0	1.0	25	μA	5.7	V_G = 5.3 V other inputs 0 V
Supply current	I_{Pmax}	32.0	30.5	28.0	mA	6.3	G inputs LOW

Note 1

For the proper combination of inputs to be HIGH or LOW see function table on page 2.

CHARACTERISTICS (continued)

		T_{amb} (°C) 0 +25 +75			Conditions and references		
					V_P (V)		Fig.
DYNAMIC DATA							
Propagation delay times from one G (G_1 to G_{10}) to Q							
Rise propagation delay time	t_{pdrmax}	– 200	–	ns	6.0	V_{pd} = 1.5 V; N = 6 C_L = 100 pF all other inputs (including G_{11}) at V_G = 5.3 V	1; 2
Fall propagation delay time	t_{pdfmax}	– 200	–	ns	6.0		
Rise propagation delay time	t_{pdrmax}	– 250	–	ns	6.0	V_{pd} = 1.5 V; N = 6 C_L = 100 pF all other inputs (excluding G_{11}) at V_G = 0.4 V V_{G11} = 5.3 V	1; 3
Fall propagation delay time	t_{pdfmax}						
Propagation delay times from G_{11} to Q							
Rise propagation delay time	t_{pdrmax}	– 100	–	ns	6.0	V_{pd} = 1.5 V; N = 6 C_L = 100 pF V_{G1} = 0 V all other inputs at V_G = 6.0 V	1; 3
Fall propagation delay time	t_{pdfmax}	– 120	–	ns	6.0		

CHARACTERISTICS (continued)

DYNAMIC DATA

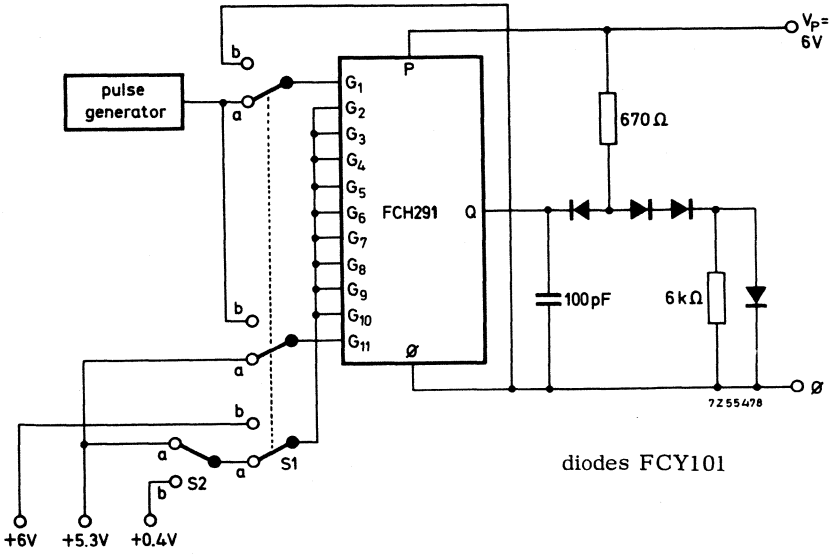


Fig. 1 Equivalent load for N = 6; C_L [1]) = 100 pF

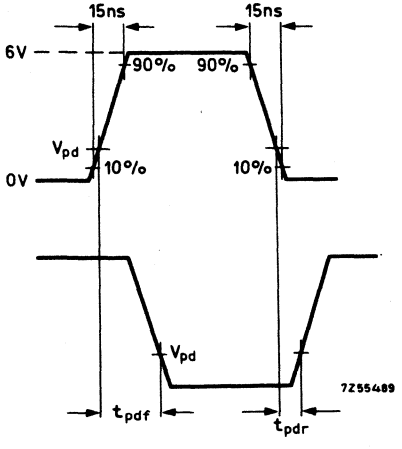


Fig. 2 Switch S2 in position a
Switch S1 in position a

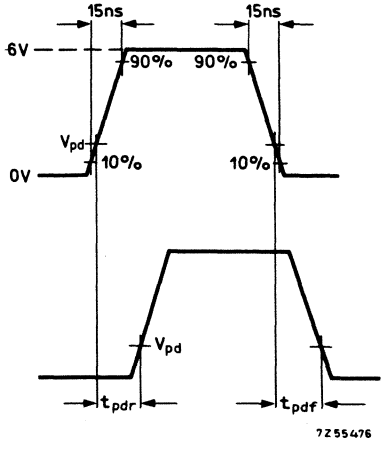


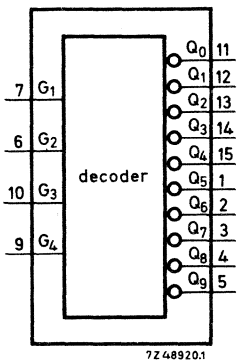
Fig. 3 Switch S1 in position a
Switch S2 in position b
or
Switch S1 in position b
Switch S2 immaterial

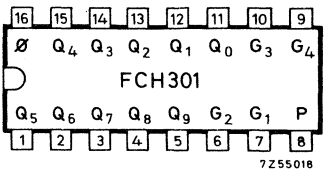
Waveforms illustrating measurement of t_{pdr} and t_{pdf}.

1) Including probe and jig capacitance.

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

SINGLE 4-BIT DECODER



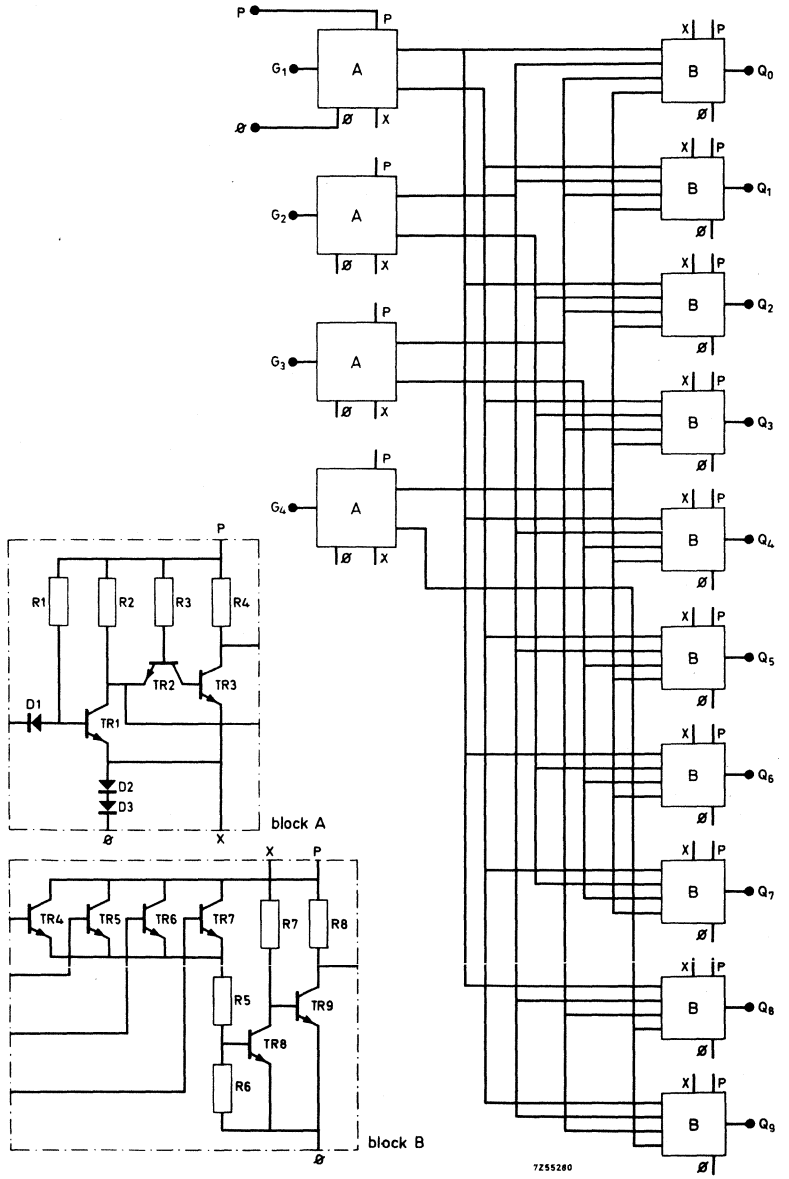


PACKAGE OUTLINE
16 lead plastic dual in-line (type A)
(See General Section)

QUICK REFERENCE DATA			
Supply voltage	V_P	6.0 ± 5%	V
Operating ambient temperature range	T_{amb}	0 to +75	°C
Average propagation delay time N = 1, C_W = 40 pF, T_{amb} = 25 °C	t_{pd}	⩽ 100	ns
Available d.c. fan out T_{amb} = 0 to +75 °C	N_a	⩾ 9	
D.C. noise margin T_{amb} = 25 °C	M_L	⩾ 0.6	V
Power consumption 50% duty cycle, T_{amb} = 25 °C	P_{av}	typ. 250	mW

The FCH301 is a fast binary (8-4-2-1) to decimal decoder formed by 18 gate functions. All outputs except the decoded one stay HIGH. If the input does not conform to the 8-4-2-1 code, all outputs remain HIGH.

CIRCUIT DIAGRAMS



FUNCTION TABLE

G_4	G_3	G_2	G_1	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8	Q_9
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

LOGIC FUNCTIONS

$$Q_0 = \overline{\overline{G_1} \cdot \overline{G_2} \cdot \overline{G_3} \cdot \overline{G_4}}$$

$$Q_1 = \overline{G_1 \cdot \overline{G_2} \cdot \overline{G_3} \cdot \overline{G_4}}$$

$$Q_2 = \overline{\overline{G_1} \cdot G_2 \cdot \overline{G_3} \cdot \overline{G_4}}$$

$$Q_3 = \overline{G_1 \cdot G_2 \cdot \overline{G_3} \cdot \overline{G_4}}$$

$$Q_4 = \overline{\overline{G_1} \cdot \overline{G_2} \cdot G_3 \cdot \overline{G_4}}$$

$$Q_5 = \overline{G_1 \cdot \overline{G_2} \cdot G_3 \cdot \overline{G_4}}$$

$$Q_6 = \overline{\overline{G_1} \cdot G_2 \cdot G_3 \cdot \overline{G_4}}$$

$$Q_7 = \overline{G_1 \cdot G_2 \cdot G_3 \cdot \overline{G_4}}$$

$$Q_8 = \overline{\overline{G_1} \cdot \overline{G_2} \cdot \overline{G_3} \cdot G_4}$$

$$Q_9 = \overline{G_1 \cdot \overline{G_2} \cdot \overline{G_3} \cdot G_4}$$

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage at T_{amb}: max. 40 °C	V_P	max.	8.0	V
Output voltage	V_Q	max.	8.0	V
Input voltage	V_G	max.	8.0	V
Input current [1]	$-I_G$	max.	20	mA
Voltage difference between any two inputs		max.	8.0	V
Storage temperature	T_{stg}	−35 to +125		°C
Operating ambient temperature	T_{amb}	0 to +75		°C

[1] At this limit, input voltage typ.: −1.5 V.

SYSTEM DESIGN DATA

Operating ambient temperature	T_{amb}		0 to +75	°C
Uniform system voltage	V_P		5.7 to 6.3	V
Available d.c. fan out	N_a		9	
D.C. noise margin	M_L	min.	0.4	V
	M_H	min.	2.9	V
Average propagation delay time	t_{pd}		100	ns
Equivalent input capacitance	C_G	typ.	4	pF
Power dissipation	P_{tot}	max.	300	mW

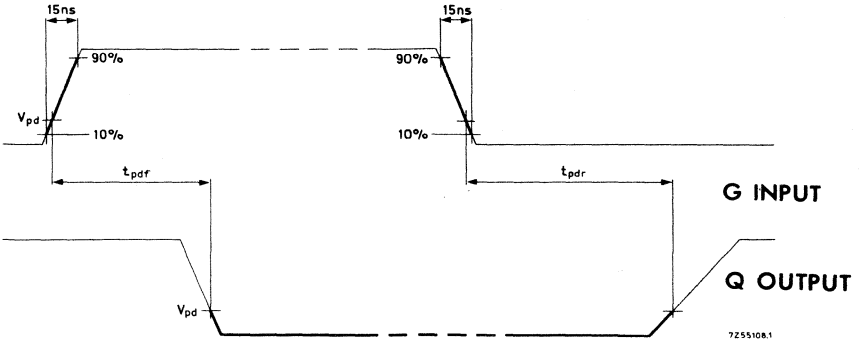
CHARACTERISTICS

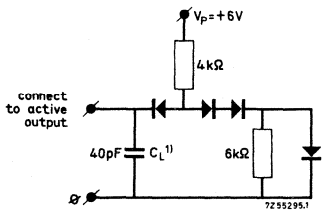
		T_{amb} (°C)				Conditions and References	
		0	25	75		V_P (V)	
STATIC DATA							
Output voltage LOW	V_{QLmax}	0.4	0.4	0.4	V	5.7 and 6.3	For the proper combination of inputs to be HIGH or LOW see Function Table
at:							
Output current LOW	I_{QLmax}	15.8	14.9	14.0	mA	5.7	
	I_{QLmax}	18.0	17.1	16.2	mA	6.3	
Output voltage HIGH	V_{QHmin}	5.2	5.2	5.2	V	5.7	$-I_Q = 0$
Input voltage LOW	V_{GLmax}	1.0	1.0	0.8	V	5.7 and 6.3	
Input voltage HIGH	V_{GHmin}	2.6	2.5	2.4	V	5.7 and 6.3	
Input current LOW	$-I_{GLmax}$	1.75	1.65	1.55	mA	5.7	$V_G = 0.4$ V
	$-I_{GLmax}$	2.0	1.9	1.8	mA	6.3	$V_G = 0.4$ V
Input current HIGH	I_{GHmax}	1.0	1.0	25	μA		$V_G = 6.3$ V other inputs 0 V
Supply current	I_{Pmax}	–	–	48	mA	6.3	G inputs 0 V

CHARACTERISTICS (continued)

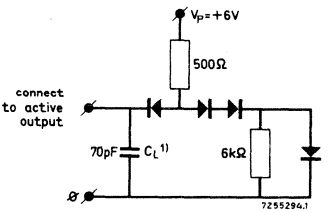
		T_{amb} (°C)				Conditions and References	
		0	25	75		V_P (V)	
DYNAMIC DATA*)							
Rise propagation delay time	t_{pdr} max	–	110	–	ns		V_{pd} = 1.5 V; N = 1; C_L = 40 pF
	t_{pdr} max	–	80	–	ns		V_{pd} = 1.5 V; N = 8; C_L = 70 pF
Fall propagation delay time	t_{pdf} max	–	85	–	ns		V_{pd} = 1.5 V; N = 1; C_L = 40 pF
	t_{pdf} max	–	100	–	ns		V_{pd} = 1.5 V; N = 8; C_L = 70 pF

*) See figures below





N = 1



N = 8

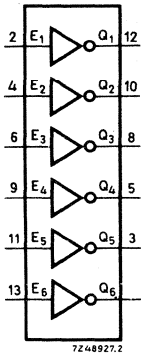
diodes FCY101

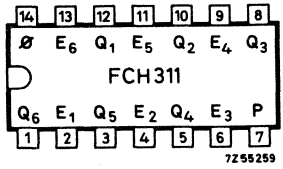
Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf}

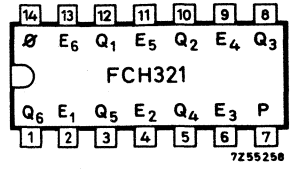
1) Including probe and jig capacitance

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

SEXTUPLE INVERTER







	non-R_C	R_C
Sextuple inverter	FCH311	FCH321

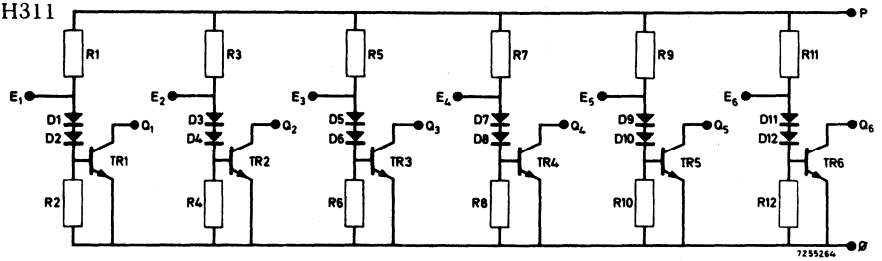
QUICK REFERENCE DATA				
Supply voltage		V_P	6.0 ± 5%	V
Operating ambient temperature range		T_{amb}	0 to +75	°C
Average propagation delay time N = 6, C_W = 60 pF, T_{amb} = 25 °C		t_{pd}	typ. 30	ns
Available d.c. fan out to FC gates T_{amb} = 0 to +75 °C		N_a	≥ 8	
Power consumption per inverter 50% duty cycle, T_{amb} = 25 °C	non-R_C	P_{av}	typ. 7	mW
	R_C	P_{av}	typ. 11	mW

The fan-in of the circuits can easily be expanded by means of a diode array.
The outputs of these inverters may be interconnected to perform the AND-OR-NOT function.

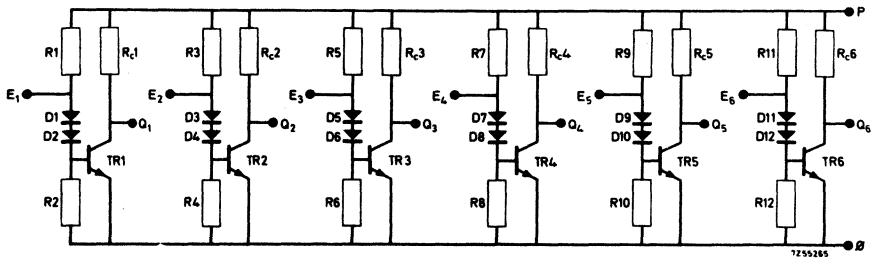
PACKAGE OUTLINES: 14 lead plastic dual in-line (type A). (See General Section)

CIRCUIT DIAGRAMS

FCH311

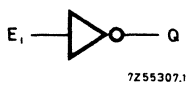


FCH321



LOGIC FUNCTION

1. Individual inverter operation

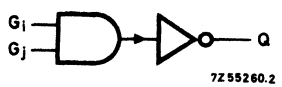


$Q = \overline{E_i}$ for positive logic

Function table

E_i	Q
L	H
H	L

2. Individual gate operation



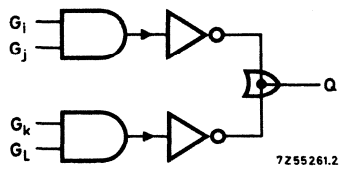
$Q = \overline{G_i \cdot G_j}$ for positive logic

Function table

G_i	G_j	Q
L	X	H
X	L	H
H	H	L

LOGIC FUNCTION (continued)

3. Commoned gate operation



Function table

G_i	G_j	G_k	G_l	Q
L	X	L	X	H
L	X	X	L	H
X	L	L	X	H
X	L	X	L	H
H	H	X	X	L
X	X	H	H	L

$Q = (\overline{G_i . G_j}) . (\overline{G_k . G_l}) = \overline{(G_i . G_j) + (G_k . G_l)}$ for positive logic

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

The AND-function is obtained by connecting a **diode array to the E input.**

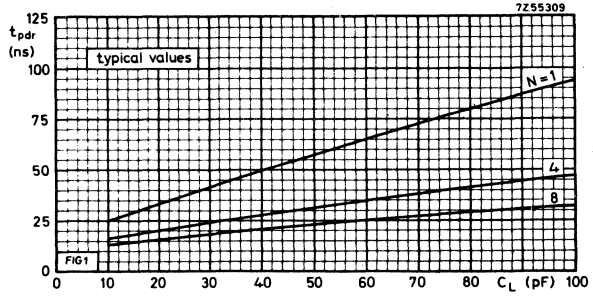
RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.	8.0	V
Output voltage (HIGH state)	V_Q	max.	8.0	V
Output current [1])	$-I_Q$	max.	20	mA
Expander input voltages with respect to supply	$V_P - V_E$	max.	8.0	V
Expander input current	I_E	max.	5.0	mA
Storage temperature	T_{stg}	−55 to +125		°C
Operating ambient temperature	T_{amb}	0 to +75		°C

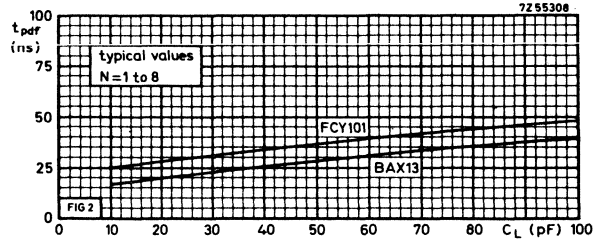
[1]) For negative output voltage.

SYSTEM DESIGN DATA (both non-R_c and R_c)

Uniform system temperature		T_{amb}	0 to +75		°C
Uniform system supply voltage		V_p	5.7 to 6.3		V
Available d.c. fan out to FC gates		N_a	≥	8	
Averaged propagation delay time with BAX13 diode		t_{pd}	max.	75	ns
Increase of t_{pdf} with increasing expander capacitance for C_w = 0 to 100 pF		Δt_{pdf}	typ.	1.4	ns/pF
Equivalent output capacitance		C_Q	typ.	10	pF
Supply current (duty cycle 50%)	non-R_c	I_{Pav}	typ.	7.2	mA
	R_c	I_{Pav}	typ.	10.5	mA
Power dissipation at T_{amb} = 75 °C	non-R_c	P_{tot}	max.	100	mW
	R_c	P_{tot}	max.	171	mW



t_{pdr} versus C_L for both BAX13 and FCY101 as input diode



t_{pdf} versus C_L for BAX13 and FCY101 as input diode

CHARACTERISTICS of FCH311 (non R_C)

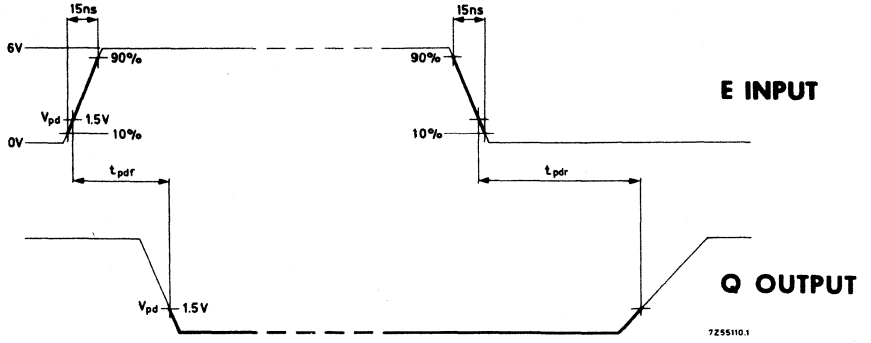
		T_{amb} (°C)				Conditions and references	
		0	+25	+75		V_P (V)	
STATIC DATA							
Output voltage LOW	V_{QLmax}	0.4	0.4	0.4	V	5.7 and 6.3	$-I_E$ = 50 μA
at:							
Output current LOW	I_{QLmax}	16.0 18.0	15.1 17.0	14.2 16.0	mA mA	5.7 6.3	
Expander input voltage HIGH	V_{EHmax}	3.0	2.8	2.6	V	5.7 and 6.3	I_{QL} = I_{QL} max $-I_E$ = 50 μA
Input current LOW	$-I_{ELmax}$	1.75 2.0	1.65 1.9	1.55 1.8	mA mA	5.7 6.3	
at: Expander input voltage LOW	V_{EL}	1.05	1.00	0.90	V		
Output current HIGH	I_{QHmax}	70	70	70	μA	5.7 and 6.3	V_Q = 5.3 V
at: Expander input voltage LOW	V_{ELmax}	1.8	1.7	1.4	V	5.7 and 6.3	
Supply current	I_{PHmax}	12.0	11.4	10.8	mA	6.3	
at: Expander input voltage LOW	V_{EL}	1.05	1.00	0.90	V		
Supply current	I_{PLmax}	11.4	10.2	10.2	mA	6.3	Expander inputs floating
DYNAMIC DATA see also page 7							
	t_{pdr} max	–	85	–	ns	6.0	R = 4 kΩ C_L = 40 pF
Rise propagation delay time	t_{pdr} max	–	70	–	ns	6.0	R = 670 Ω C_L = 60 pF
	t_{pdf} max	–	65	–	ns	6.0	R = 4 kΩ C_L = 40 pF
Fall propagation delay time	t_{pdf} max	–	85	–	ns	6.0	R = 670 Ω C_L = 60 pF

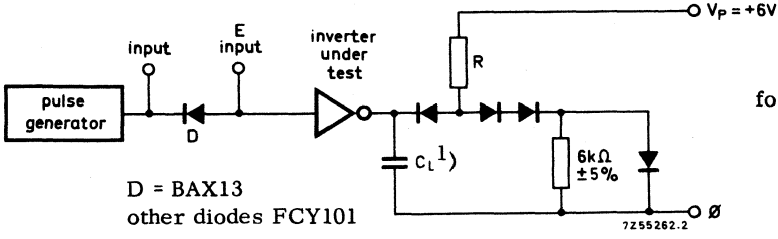
CHARACTERISTICS of FCH321 (R_c)

		T_{amb} (°C)				Conditions and references	
		0	+25	+75		V_P (V)	
STATIC DATA							
Output voltage LOW	V_{QLmax}	0.4	0.4	0.4	V	5.7 and 6.3	$-I_E$ = 50 μA
at:							
Output current LOW	I_{QLmax}	14.0 16.0	13.2 15.2	12.4 14.4	mA mA	5.7 6.3	
Expander input voltage HIGH	V_{EHmax}	3.0	2.8	2.6	V	5.7 and 6.3	$I_{QL} = I_{QL}$ max $-I_E$ = 50 μA
Output voltage HIGH	V_{QHmin}	5.3 4.1	5.3 4.1	5.3 3.9	V V	5.7 5.7	I_Q = 0 I_Q = −200 μA
at: Expander input voltage LOW	V_{ELmax}	1.8	1.7	1.4	V	5.7 and 6.3	
Input current LOW	$-I_{ELmax}$	1.75 2.0	1.65 1.9	1.55 1.8	mA mA	5.7 6.3	
at: Expander input voltage LOW	V_{EL}	1.05	1.00	0.90	V		
Output current LOW (AND-OR-NOT function)	$-I_{QLLmax}$	2.2	2.1	2.0	mA	6.3	Expander inputs LOW Output forced LOW externally to V_Q = 0.4 V
Supply current	I_{PLmax}	25.2	22.8	21.6	mA	6.3	Expander inputs floating
DYNAMIC DATA see also page 7							
Rise propagation delay time	t_{pdr} max	–	85	–	ns	6.0	R = 4 kΩ C_L = 40 pF
	t_{pdr} max	–	70	–	ns	6.0	R = 670 Ω C_L = 60 pF
Fall propagation delay time	t_{pdf} max	–	65	–	ns	6.0	R = 4 kΩ C_L = 40 pF
	t_{pdf} max	–	85	–	ns	6.0	R = 670 Ω C_L = 60 pF

CHARACTERISTICS (continued)

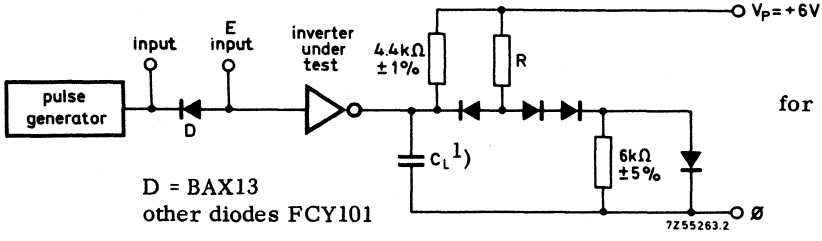
DYNAMIC DATA





for FCH321

D = BAX13
other diodes FCY101



for FCH311

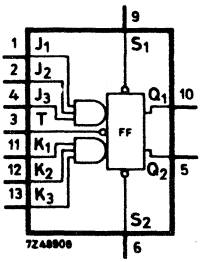
D = BAX13
other diodes FCY101

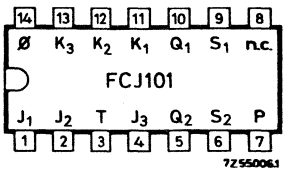
Waveforms and loading circuits, illustrating measurement of t_{pdr} and t_{pdf}.

1) Including probe and jig capacitance

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

SINGLE JK FLIP-FLOP



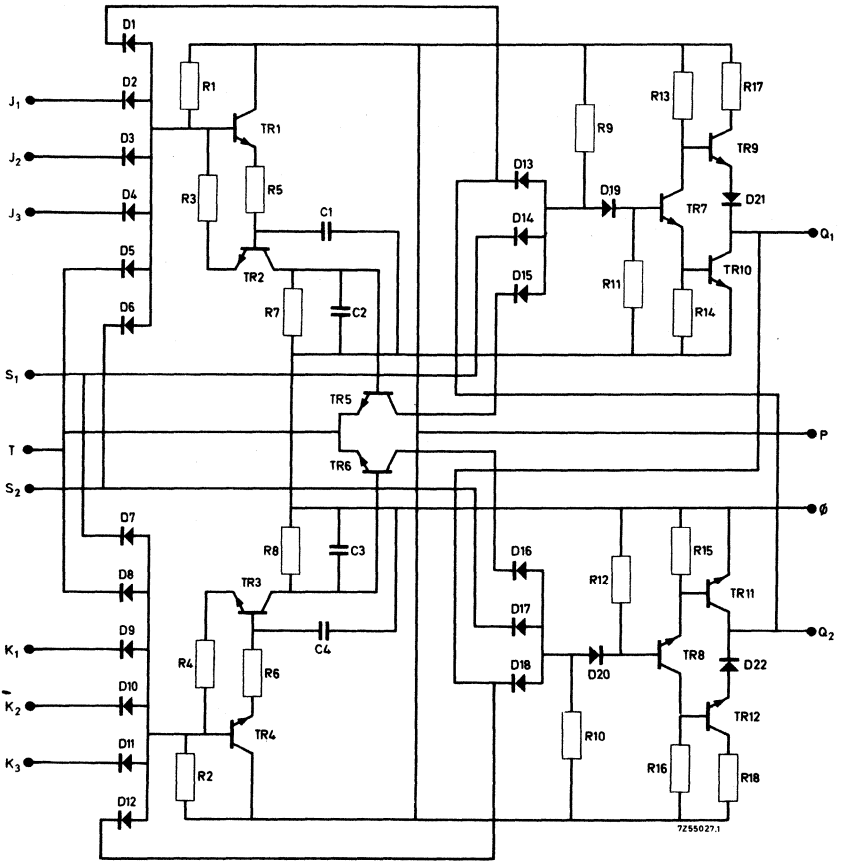


QUICK REFERENCE DATA			
Supply voltage	V_P	6.0 ± 5%	V
Operating ambient temperature range	T_{amb}	0 to +75	°C
Clock rate	f_c	typ. 10	MHz
Available d.c. fan out T_{amb} = 0 to +75 °C	N_a	⩾ 8	
D.C. noise margin T_{amb} = 25 °C	M_L	typ. 1.2	V
Power consumption 50% duty cycle, T_{amb} = 25 °C	P_{av}	typ. 36	mW

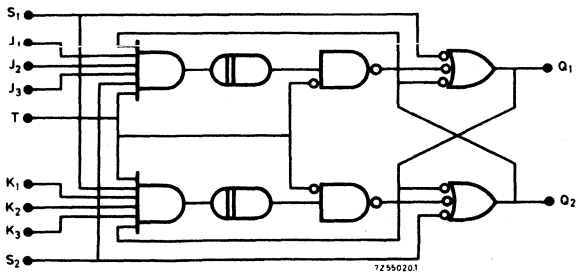
The FCJ101 performs the JK flip-flop operation. Three J and three K inputs permit an additional AND operation. Triggering occurs at the falling edge of a T signal. The direct-set inputs (overriding any other inputs) are active at the LOW level. The circuitry incorporates bi-directional outputs for driving capacitive loads. Typical applications are in high speed counters and shift registers.

PACKAGE OUTLINE: 14 lead plastic dual in-line (type A). (See General Section)

CIRCUIT DIAGRAM



LOGIC DIAGRAM (to MIL standard 806B)



FUNCTION TABLES

1. Trigger action via T terminal

T = HIGH		T = LOW	
J	K	Q_1	Q_2
H	H	reversed	
L	H	L	H
H	L	H	L
L	L	no change	

The information on J and K is transferred into the flip-flop by T becoming HIGH. When T subsequently goes LOW the outputs will assume the levels shown in the table. Inputs S_1 and S_2 should be HIGH or floating.

$J = J_1 \cdot J_2 \cdot J_3$
$K = K_1 \cdot K_2 \cdot K_3$
} for positive logic

2. Set or reset via S terminals

S_1	S_2	Q_1	Q_2
H	L	L	H
L	H	H	L
L	L	H	H
H	H	no change	

The set inputs override the other inputs and directly determine the outputs of the flip-flop.

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

RATINGS (Limiting values) [1]

Supply voltage	V_P	max.	8.0	V
Output voltage	V_Q	max.	8.0	V
Input voltage	V_J, V_K, V_T, V_S	max.	8.0	V
Output current [2]	$-I_Q$	max.	20	mA
Input current [3]	$-I_J, -I_K, -I_T, -I_S$	max.	20	mA
Voltage difference between any two inputs		max.	8.0	V
Storage temperature	T_{stg}	−55 to	+125	°C
Operating ambient temperature	T_{amb}	0 to	+75	°C

1) Limiting values according to the Absolute Maximum System as defined in IEC publication 134.
2) For negative output voltage in LOW state.
3) At this limit input voltage typ. : −1.5 V.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}		0 to +75	°C
Uniform system supply voltage	V_P		5.7 to 6.3	V
Available d.c. fan out				
to J or K input	$N_{aJ} = N_{aK}$	⩾	8	
to S input	N_{aS}	⩾	4	
to G input	N_{aG}	⩾	8	
Available a.c. fan out to T input	N_{aT}	⩾	2	
D.C. noise margin				
to T input	M_L	min.	0.3	V
	M_H	min.	0.2	V
to J or K input	M_L	min.	0.5	V
	M_H	min.	0.2	V
to S input	M_L	min.	0.3	V
	M_H	min.	0.2	V
to G input	M_L	min.	0.4	V
	M_H	min.	1.5	V
Average propagation delay time	t_{pd}	max.	85	ns
Maximum clock rate	f_c	⩾	6	MHz
Equivalent input capacitances				
for T input	C_T	typ.	30	pF
for J or K input	$C_J = C_K$	typ.	20	pF
for S input	C_S	typ.	25	pF
Supply current (duty cycle 50%)	I_{Pav}	typ.	6.0	mA
Power dissipation at T_{amb} = 75 °C	P_{tot}	max.	56	mW

CHARACTERISTICS

		T_{amb} (°C)			Conditions and references	
		0	+25	+75	V_P (V)	
STATIC DATA						
Output voltage LOW	V_{QLmax}	0.4	0.4	0.4 V	5.7 and 6.3	
at:						
Output current LOW	I_{QLmax}	14.0	16.5	12.4 mA	5.7	
		16.0	19.0	14.4 mA	6.3	
Output voltage HIGH	V_{QHmin}	3.8	3.9	4.1 V	5.7	$I_Q = -100\ \mu A$
Output voltage HIGH (lowest permissible)	V_{QHPmin}	3.6	3.3	3.0 V	5.7	
at:						
Output current HIGH	$-I_{QHmax}$	0.85	3.3	5.5 mA	5.7	
Input current LOW	$-I_{JLmax}$, $-I_{KLmax}$	1.75	1.65	1.55 mA	5.7	$V_J = V_K = 0.4$ V; other inputs floating
		2.0	1.9	1.8 mA	6.3	
	$-I_{TLmax}$	3.5	3.3	3.1 mA	5.7	$V_T = 0.4$ V; other inputs floating
		4.0	3.8	3.6 mA	6.3	
	$-I_{SLmax}$	3.5	3.3	3.1 mA	5.7	$V_S = 0.4$ V; other inputs floating
		4.0	3.8	3.6 mA	6.3	
Input current HIGH	$-I_{JHmax}$, $-I_{KHmax}$	1	1	25 μA	5.7	$V_J = V_K = 5.3$ V other inputs 0 V
	I_{THmax}	2	2	50 μA	5.7	$V_T = 5.3$ V other inputs 0 V
	I_{SHmax}	2	2	50 μA	5.7	$V_S = 5.3$ V other inputs 0 V
Supply current	I_{Pmax}	–	9	– mA	6.3	T input LOW J, K, S inputs HIGH

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references		
		0	+25	+75		V_P (V)		fig.
DYNAMIC DATA						5.7 and 6.3		
Change of state								
Input voltage HIGH during:	V_{THmin} V_{JHmin} V_{KHmin}	3.6	3.3	3.0	V		HIGH level at T and J and/or K to be present simultaneously	1
Input time HIGH	t_{THmin}	50	50	50	ns			1
followed by:	$(-\frac{dt}{dV})_{Tmax}$	18	18	18	ns/V			1
T-input slope to:	$(-\frac{dt}{dV})_{Tmin}$	4	4	4	ns/V			1
T-input voltage LOW	V_{TLmax}	0.7	0.7	0.7	V		$t_{TLmin} = t_{pdf}$	1
No change of state								
JK-input voltage LOW during:	V_{JLmax} V_{KLmax}	1.1	1.0	0 9	V		J and K turning LOW after T and J and/or K having	2
JK-input time LOW	t_{JLmin} t_{KLmin}	100	100	160	ns		been HIGH simultaneously	2
Clock skew protection								
Hold time LOW	$t_{holdLmax}$	15	15	15	ns			2
Hold time HIGH	$t_{holdHmax}$	7	10	10	ns			3
Set or Reset								
S-input voltage LOW	V_{SLmax}	1.0	0.9	0.7	V		active $t_{SLmin} = t_{pdf}$	4
S-input voltage HIGH	V_{SHmin}	3.6	3.3	3.0	V		inactive	
Propagation delay times from T to Q								
Rise propagation delay time	$t_{pdr\,max}$	–	70	–	ns	6.0	V_{pd} = 1.5 V N = 1; C_L = 60 pF	5
Fall propagation delay time	$t_{pdf\,max}$	–	100	–	ns	6.0	V_{pd} = 1.5 V N = 8; C_L = 60 pF other output N = 1 C_L = 60 pF	5

CHARACTERISTICS (continued)

DYNAMIC DATA

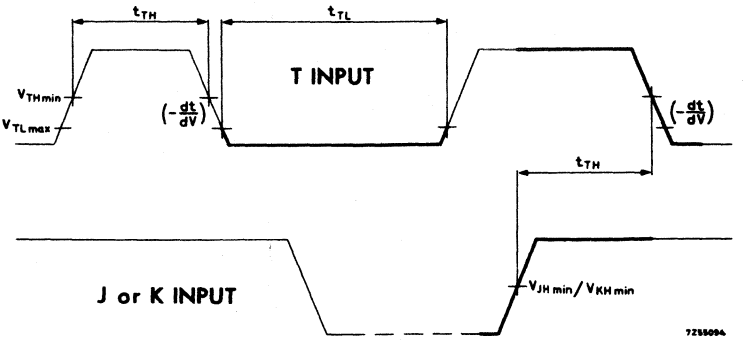


Fig.1. Waveforms illustrating conditions for change of state.

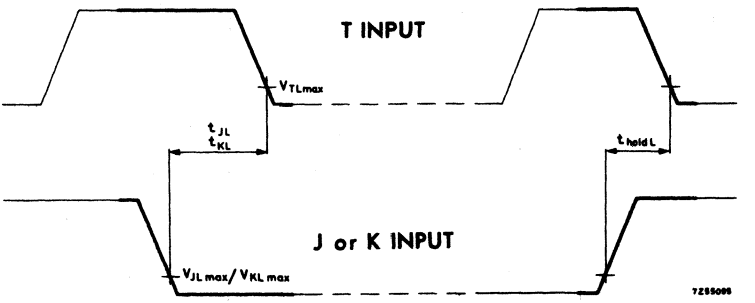


Fig.2. Waveforms illustrating conditions for no change of state.

For no change of state to result:

a. the time between J or K reaching V_{JLmax}, V_{KLmax} (going LOW) and T reaching V_{TLmax} (going LOW) must be at least t_{JLmin}, t_{KLmin}.

b. the time between J or K reaching V_{JLmax}, V_{KLmax} (going HIGH) and T reaching V_{TLmax} (going LOW) must be less than t_{holdL}.

CHARACTERISTICS (continued)

DYNAMIC DATA

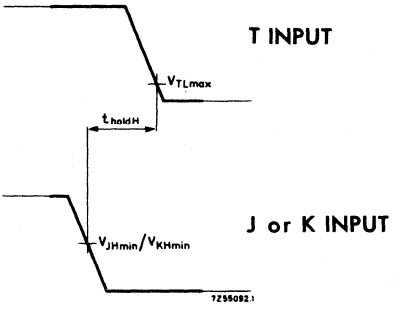


Fig.3. Waveforms illustrating conditions for change of state.
For a change of state still to result, the time between J or K reaching V_{JHmin}, V_{KHmin} (going LOW) and T reaching V_{TLmax} (going LOW) must be less than t_{holdH}

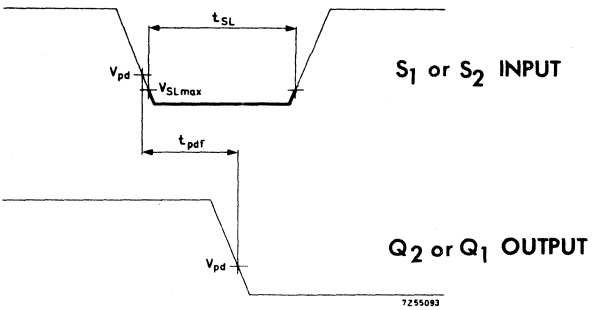
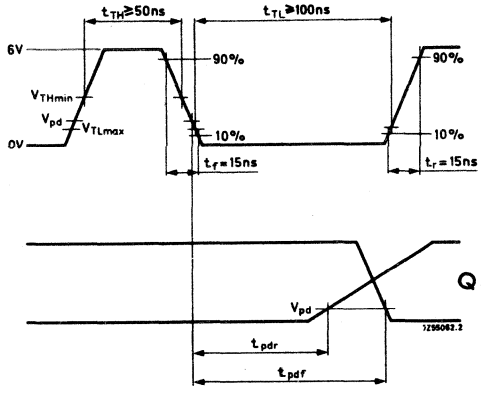
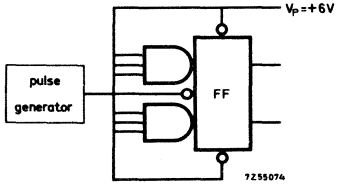


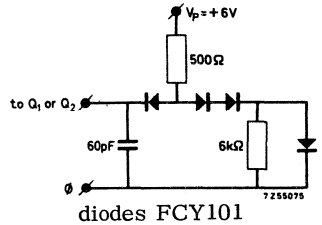
Fig.4. Waveforms illustrating conditions for set or reset.

CHARACTERISTICS (continued)

DYNAMIC DATA

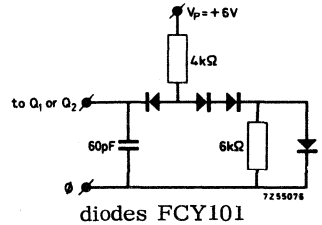






diodes FCY101

Equivalent load for N = 8 and C_L[1]) = 60 pF



diodes FCY101

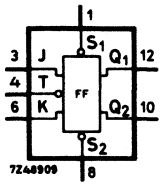
Equivalent load for N = 1 and C_L[1]) = 60 pF

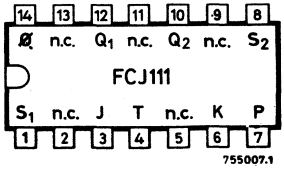
Fig. 5. Waveforms and loading circuits illustrating measurement of t_{pdr} and t_{pdf}.

[1]) Including probe and jig capacitance

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

SINGLE JK MASTER-SLAVE FLIP-FLOP



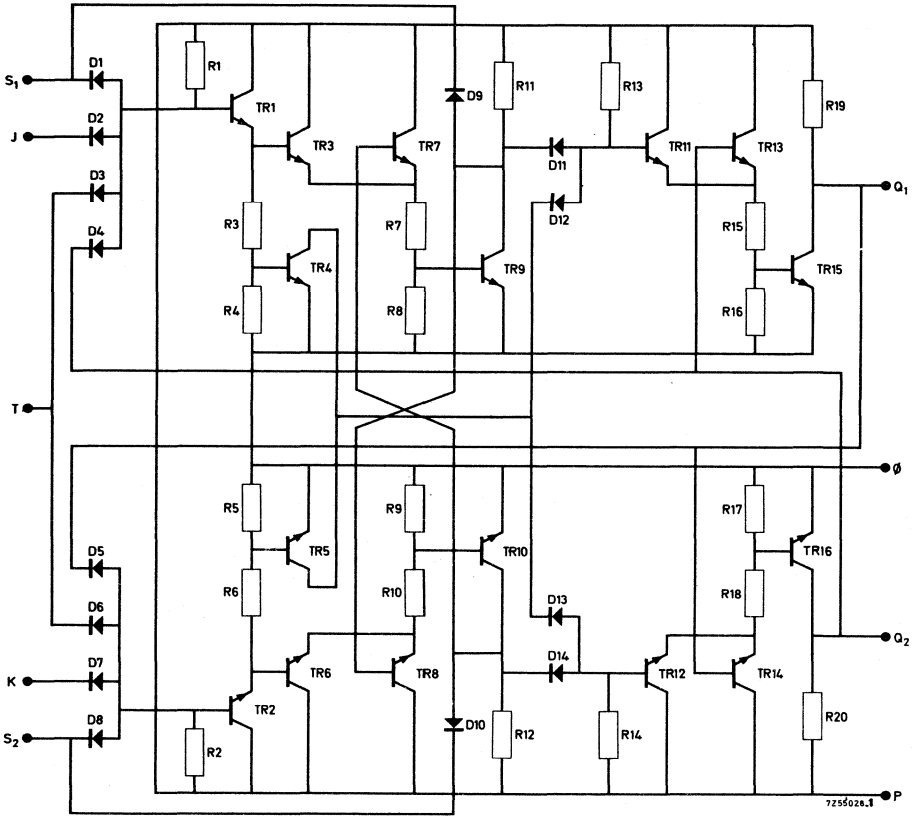


QUICK REFERENCE DATA			
Supply voltage	V_P	6.0 ± 5%	V
Operating ambient temperature range	T_{amb}	0 to +75	°C
Clock rate	f_c	typ. 5	MHz
Available d.c. fan-out T_{amb} = 0 to 75 °C	N_a	≥ 8	
D.C. noise margin T_{amb} = 25 °C	M_L	typ. 1.2	V
Power consumption 50% duty cycle, T_{amb} = 25 °C	P_{av}	typ. 67	mW

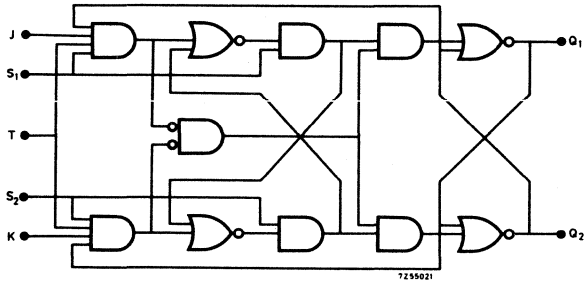
The FCJ111 is a direct-coupled JK flip-flop, operating on the master-slave principle. Operation depends on voltage levels only, i.e. rise and fall times of all input signals, including the trigger signal, are immaterial. The J, K and T inputs are logically equivalent, allowing the use of J and K for triggering. The direct set-inputs (overriding any other inputs) are active at the LOW level.

PACKAGE OUTLINE : 14 lead plastic dual in-line (type A). (See General Section)

CIRCUIT DIAGRAM



LOGIC DIAGRAM(to MIL standard 806B)



FUNCTION TABLES

1. Trigger action via T terminal (each flip-flop)

T = HIGH		T = LOW	
J	K	Q_1	Q_2
H	H	reversed	
L	H	L	H
H	L	H	L
L	L	no change	

The information on J and K is transferred into the master by T becoming HIGH. When T subsequently goes LOW the outputs will assume the levels shown in the table. Inputs S_1 or S_2 should be HIGH or floating.

2. Trigger action via J and K terminals

J	K	Q_1	Q_2
H→L	X	H	L
X	H→L	L	H
H→L	H→L	reversed	

If J or K go LOW with T HIGH, Q_1 and Q_2 assume the state shown. If both J and K go LOW with T HIGH, the outputs of Q_1 and Q_2 are reversed (exactly as if J and K remained HIGH and T were triggered). When triggering on J and K the T input requirements V_{TH} and V_{TL} (see CHARACTERISTICS) apply to J and K. S_1 and S_2 should be HIGH or floating.

3. Set or reset via S terminals

S_1	S_2	Q_1	Q_2
H	L	L	H
L	H	H	L
L	L	indeterminate	
H	H	no change	

The set inputs override the other inputs and directly determine the outputs of the flip-flop. In the case of both set inputs going LOW the first to reach LOW will determine the output conditions.

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	8.0	V
Output voltage	V_Q	max.	8.0	V
Input voltage	V_J, V_K, V_T, V_S	max.	8.0	V
Output current [1]	$-I_Q$	max.	20	mA
Input current [2]	$-I_J, -I_K, -I_T, -I_S$	max.	20	mA
Voltage difference between any two inputs		max.	8.0	V
Storage temperature	T_{stg}	−55 to +125		°C
Operating ambient temperature	T_{amb}	0 to +75		°C

[1] For negative output voltage.
[2] At this limit input voltage typ.: −1.5 V.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to +75		°C
Uniform system supply voltage	V_P	5.7 to 6.3		V
Available d.c. fan out				
to T input	N_{aT}	⩾	4	
to J or K input	$N_{aJ} = N_{aK}$	⩾	8	
to S input	N_{aS}	⩾	5	
to G input	N_{aG}	⩾	8	
D.C. noise margin				
to T input	M_L	min.	0.5	V
	M_H	min.	1.9	V
to J or K input	M_L	min.	0.9	V
	M_H	min.	1.9	V
to S input	M_L	min.	0.4	V
	M_H	min.	1.9	V
to G input	M_L	min.	0.4	V
	M_H	min.	2.3	V
Average propagation delay time	t_{pd}	max.	150	ns
Maximum clock rate	f_c	⩾	3	MHz
Equivalent input capacitances				
for T input	C_T	typ.	8	pF
for J or K input	$C_J = C_K$	typ.	4	pF
for S input	C_S	typ.	8	pF
Supply current (duty cycle 50%)	I_{Pav}	typ.	11.2	mA
Power dissipation at T_{amb} = 75 °C	P_{tot}	max.	110	mW

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references	
		0	+25	+75		V_P (V)	
STATIC DATA							
Output voltage LOW	V_{QLmax}	0.4	0.4	0.4	V	5.7 and 6.3	
at: Output current LOW	I_{QLmax}	14.0 16.0	13.2 15.2	12.4 14.4	mA mA	5.7 6.3	
Output voltage HIGH	V_{QHmin}	5.3	5.4	5.3	V	5.7	$I_Q = 0$
Output voltage HIGH (lowest permissible)	V_{QHPmin}	3.9	3.5	2.8	V	5.7	
at: Output current HIGH	$-I_{QHmax}$	350	450	550	μA	5.7	
Input current LOW	$-I_{JLmax}$, $-I_{KLmax}$	1.75 2.0	1.65 1.9	1.55 1.8	mA mA	5.7 6.3	$V_J = V_K = 0.4$ V; other inputs floating
	$-I_{TLmax}$	3.5 4.0	3.3 3.8	3.1 3.6	mA mA	5.7 6.3	$V_T = 0.4$ V; other inputs floating
	$-I_{SLmax}$	2.7 3.0	2.6 2.9	2.4 2.7	mA mA	5.7 6.3	$V_S = 0.4$ V; other inputs floating
Input current HIGH	I_{JHmax}, I_{KHmax}	1	1	25	μA	5.7	$V_J = V_K = 5.3$ V other inputs 0 V
	I_{THmax}	2	2	50	μA	5.7	$V_T = 5.3$ V other inputs 0 V
	I_{SHmax}	2	2	50	μA	5.7	$V_S = 5.3$ V other inputs 0 V
Supply current	I_{Pmax}	–	20	–	mA	6.3	J, K, S,T inputs HIGH

CHARACTERISTICS

		T_{amb} (°C)			Conditions and references		
		0	+25	+75	V_P (V)		fig.
DYNAMIC DATA					5.7 and 6.3		
Change of state							
Input voltage HIGH during: T-input time HIGH to: Input voltage LOW	V_{THmin} V_{JHmin} V_{KHmin}	3.1	2.9	2.5 V		HIGH level at T and J and/or K to be present simultaneously	1
	t_{THmin}	100	100	100 ns			1
	V_{TLmax}	1.3	1.1	0.9 V		$t_{TLmin} = t_{pdr}$	1
No change of state							
JK input voltage LOW	V_{JLmax} V_{KLmax}	1.8	1.6	1.3 V		LOW level at J and K to be present prior to T turning HIGH and to remain present during T is HIGH	2
Clock skew protection							
Hold time	$t_{holdmax}$	20	20	20 ns			2
Set or Reset							
S input voltage LOW	V_{SLmax}	1.2	1.0	0.8 V		active $t_{SLmin} = t_{pdr}$	3
S input voltage HIGH	V_{SHmin}	3.1	2.9	2.5 V		inactive	
DYNAMIC DATA							
Propagation delay times from T to Q							
Rise propagation delay time	t_{pdrmax}	–	200	– ns		$V_{pd} = 1.5$ V; N = 1; C_L = 60 pF; other output N = 8; C_L = 56 pF	4
Fall propagation delay time	t_{pdfmax}	–	100	– ns		$V_{pd} = 1.5$ V; N = 8; C_L = 56 pF	4

CHARACTERISTICS (continued)

DYNAMIC DATA

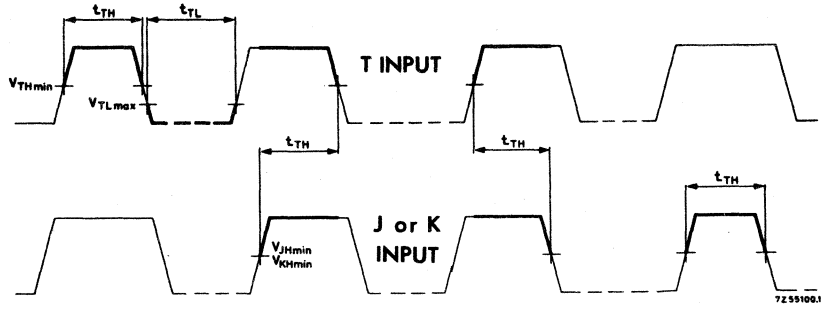


Fig. 1. Waveforms illustrating conditions for change of state.

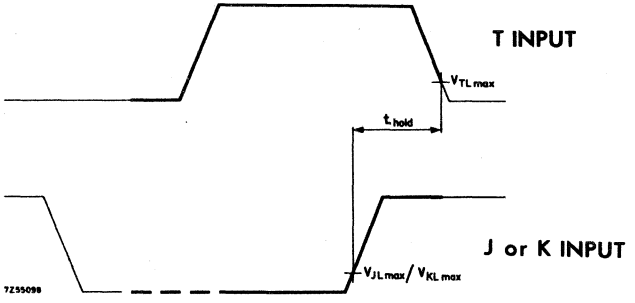


Fig. 2. Waveforms illustrating conditions for no change of state.

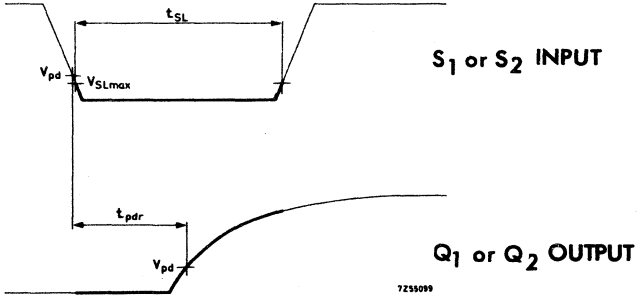
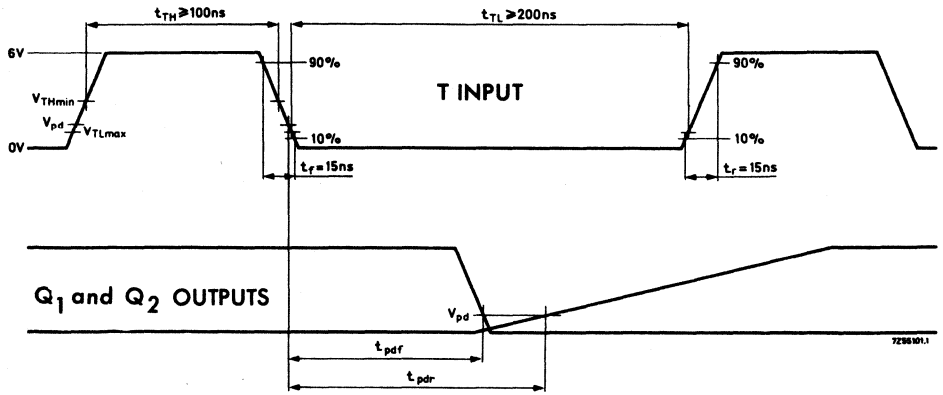
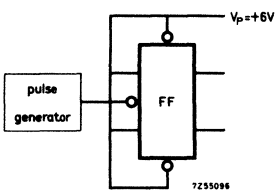


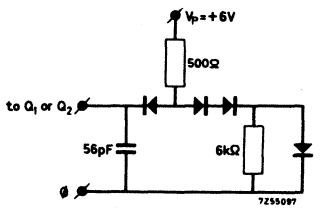
Fig. 3. Waveforms illustrating conditions for set or reset.

CHARACTERISTICS (continued)

DYNAMIC DATA

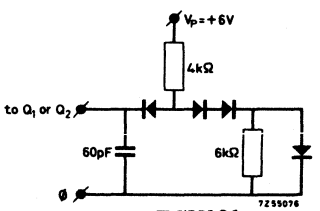






diodes FCY101

Equivalent load for N = 8 and C_L[1]) = 56 pF



diodes FCY101

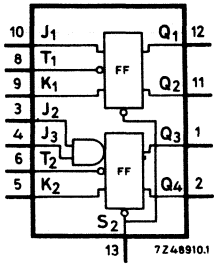
Equivalent load for N = 1 and C_L[1]) = 60 pF

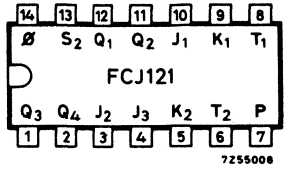
Fig. 4. Waveforms and loading circuits illustrating measurement of t_{pdr} and t_{pdf}.

[1]) Including probe and jig capacitance

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

DUAL JK MASTER-SLAVE FLIP-FLOP



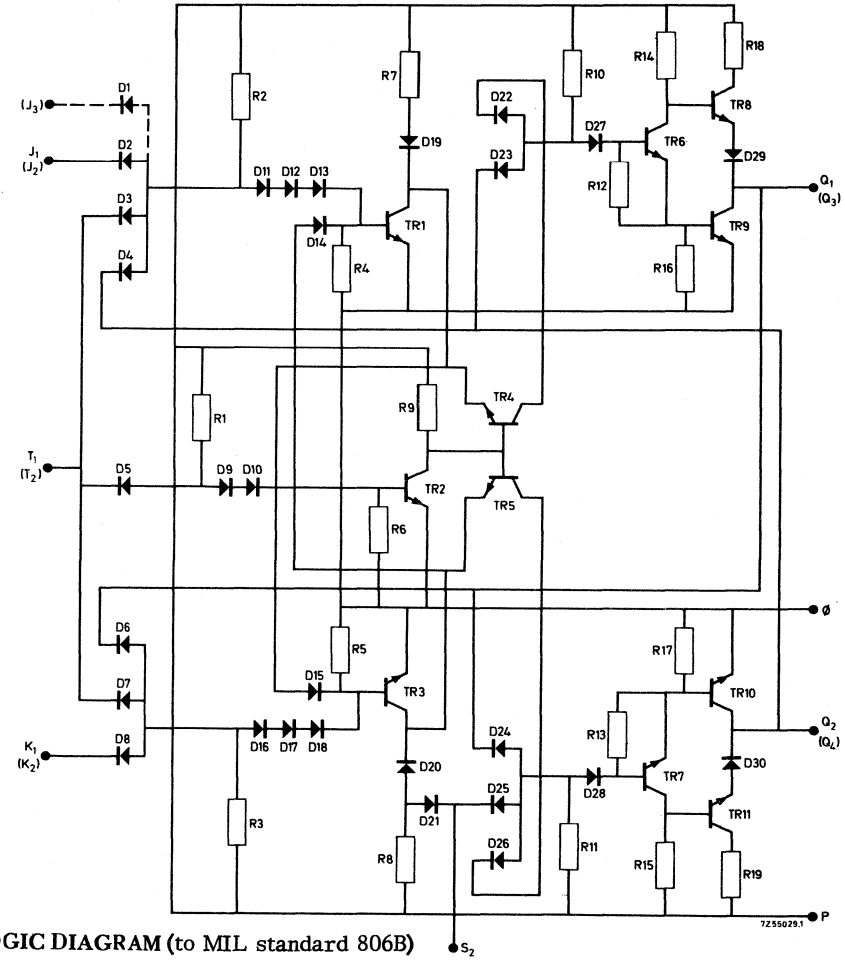


QUICK REFERENCE DATA			
Supply voltage	V_P	6.0 ± 5%	V
Operating ambient temperature range	T_{amb}	0 to +75	°C
Clock rate	f_c	typ. 7	MHz
Available d.c. fan out T_{amb} = 0 to +75 °C	N_a	⩾ 8	
D.C. noise margin T_{amb} = 25 °C	M_L	typ. 1.2	V
Power consumption 50% duty cycle, T_{amb} = 25 °C (each flip-flop)	P_{av}	typ. 50	mW

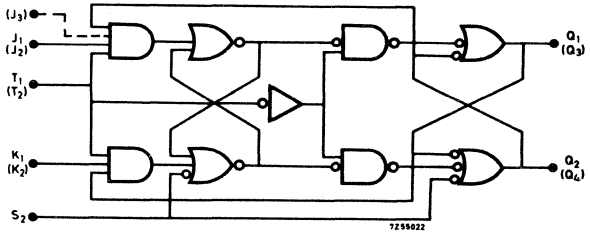
The FCJ121 comprises two independent direct coupled JK flip-flops, operating on the master-slave principle. Operation depends on voltage levels only, i.e. rise and fall times of all input signals including trigger signals are immaterial. The common set-input (overriding any other inputs) is active at the LOW level. Typical applications are in medium speed counters.

PACKAGE OUTLINE: 14 lead plastic dual in-line (type A). (See General Section)

CIRCUIT DIAGRAM



LOGIC DIAGRAM (to MIL standard 806B)



FUNCTION TABLES

1. Trigger action via T terminal (each flip-flop)

T = HIGH		T = LOW	
J_1 J_2	K_1 K_2	Q_1 Q_3	Q_2 Q_4
H	H	reversed	
L	H	L	H
H	L	H	L
L	L	no change	

The information on J and K is transferred into the master by T becoming HIGH. When T subsequently goes LOW the outputs will assume the levels shown in the table. Input S_2 should be HIGH or floating.

For the flip-flop with two J-inputs: $J = J_2 \cdot J_3$ for positive logic

2. Set or Reset via S_2 terminal (both flip-flops)

S_2 S_4	Q_1 Q_3	Q_2 Q_4
L	L	H
H	no change	

The set input overrides the other inputs and directly determines the outputs of both flip-flops.

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

RATINGS (Limiting values) [1]

Supply voltage	V_P	max.	8.0	V
Output voltage	V_Q	max.	8.0	V
Input voltage	V_J, V_K, V_T, V_S	max.	8.0	V
Output current [2]	$-I_Q$	max.	20	mA
Input current [3]	$-I_J, -I_K, -I_T, -I_S$	max.	20	mA
Voltage difference between any two inputs		max.	8.0	V
Storage temperature	T_{stg}	−55 to	+125	°C
Operating ambient temperature	T_{amb}	0 to	+75	°C

1) Limiting values according to the Absolute Maximum System as defined in IEC publication 134.

2) For negative output voltage in LOW state.

3) At this limit input voltage typ. : −1.5 V

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to +75		°C
Uniform system supply voltage	V_P	5.7 to 6.3		V
Available d.c. fan out				
to T input	N_{aT}	⩾	3	
to J or K input	$N_{aJ} = N_{aK}$	⩾	10	
to S input	N_{aS}	⩾	2	
to G input	N_{aG}	⩾	8	
D.C. noise margin				
to T input	M_L	min.	0.3	V
	M_H	min.	1.2	V
to J or K input	M_L	min.	0.7	V
	M_H	min.	1.2	V
to S input	M_L	min.	0.3	V
	M_H	min.	1.9	V
to G input	M_L	min.	0.4	V
	M_H	min.	1.5	V
Average propagation delay time	t_{pd}	max.	105	ns
Maximum clock rate	f_c	⩾	5	MHz
Equivalent input capacitances				
for T input	C_T	typ.	12	pF
for J or K input	$C_J = C_K$	typ.	4	pF
for S input	C_S	typ.	16	pF
Supply current (duty cycle 50%) [1]	I_{Pav}	typ.	16.8	mA
Power dissipation at T_{amb} = 75 °C [1]	P_{tot}	max.	150	mW

[1] Both flip-flops together.

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references	
		0	+25	+75		V_P (V)	
STATIC DATA							
Output voltage LOW	V_{QL}	0.4	0.4	0.4	V	5.7 and 6.3	
at: Output current LOW	I_{QLmax}	14.0	16.5	12.4	mA	5.7	
		16.0	19.0	14.4	mA	6.3	
Output voltage HIGH	V_{QHmin}	3.8	3.9	4.1	V	5.7	I_Q = −100 μA
Output voltage HIGH (lowest permissible)	V_{QHPmin}	3.6	3.3	3.0	V	5.7	
at: Output current HIGH	$-I_{QHmax}$	0.85	3.3	5.5	mA	5.7	
Input current LOW	$-I_{JLmax}$, $-I_{KLmax}$	1.4	1.3	1.2	mA	5.7	$V_J = V_K = 0.4$ V; other inputs floating
		1.6	1.5	1.4	mA	6.3	
	$-I_{TLmax}$	4.0	3.8	3.5	mA	5.7	$V_T = 0.4$ V; other inputs floating
		4.5	4.2	3.9	mA	6.3	
	$-I_{SLmax}$	5.7	5.5	5.2	mA	5.7	$V_S = 0.4$ V; other inputs floating
		6.6	6.3	5.8	mA	6.3	
Input current HIGH	I_{JHmax}, I_{KHmax}	1	1	25	μA	5.7	$V_J = V_K = 5.3$ V other inputs 0 V
	I_{THmax}	3	3	75	μA	5.7	$V_T = 5.3$ V other inputs 0 V
	I_{SHmax}	4	4	100	μA	5.7	$V_S = 5.3$ V other inputs 0 V
Supply current (both flip-flops together)	I_{Pmax}	–	26.7	–	mA	6.3	T input LOW J, K, S inputs HIGH

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references		
		0	+25	+75		V_P (V)		fig.
DYNAMIC DATA						5.7 and 6.3		
Change of state								
Input voltage HIGH during:	V_{THmin} V_{JHmin} V_{KHmin}	2.6	2.3	1.9	V		HIGH level at T and J and/or K to be present simultaneously	1
Input time HIGH to:	t_{THmin}	60	60	60	ns			1
T-input voltage LOW	V_{TLmax}	1.0	1.0	0.7	V		$t_{TLmin} = t_{pdf}$	1
No change of state								
J/K input voltage LOW	V_{JLmax} V_{KLmax}	1.6	1.4	1.1	V		LOW level at J and K to be present prior to T turning HIGH and to remain present during T is HIGH	2
Clock skew protection								
Hold time	$t_{hold\,max}$	10	10	10	ns			2
Reset								
S input voltage LOW	V_{SLmax}	1.0	1.0	0.7	V		active $t_{SLmin} = t_{pdf}$	3
S input voltage HIGH	V_{SHmin}	1.9	1.8	1.6	V		inactive	
DYNAMIC DATA								
Propagation delay times from T to Q								
Rise propagation delay time	$t_{pdr\,max}$	–	90	–	ns	6.0	V_{pd} = 1.5 V N = 1; C_L = 60 pF	4
Fall propagation delay time	$t_{pdf\,max}$	–	120	–	ns	6.0	V_{pd} = 1.5 N = 8; C_L = 60 pF other output: N = 1; C_L = 60 pF	4

CHARACTERISTICS(continued)

DYNAMIC DATA

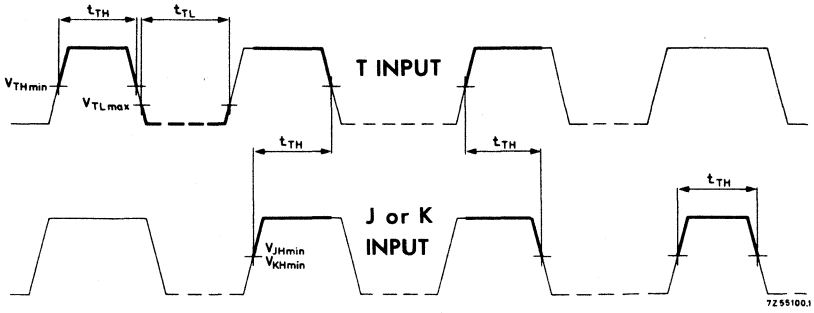


Fig. 1. Waveforms illustrating conditions for change of state.

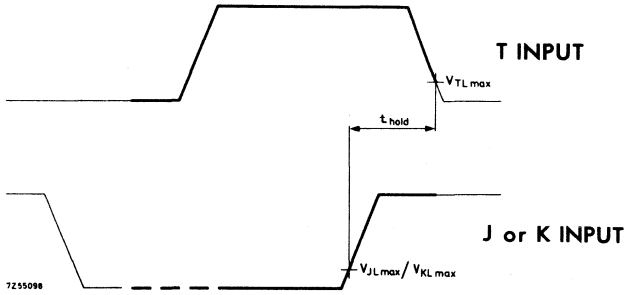


Fig. 2. Waveforms illustrating conditions for no change of state.

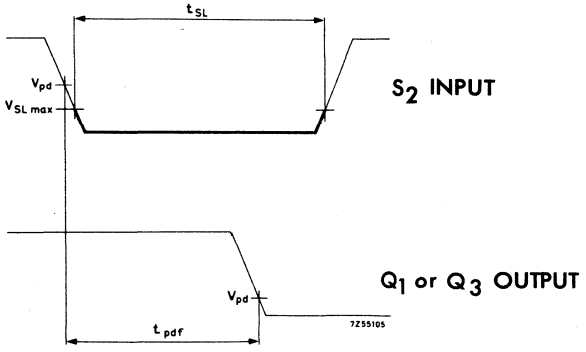
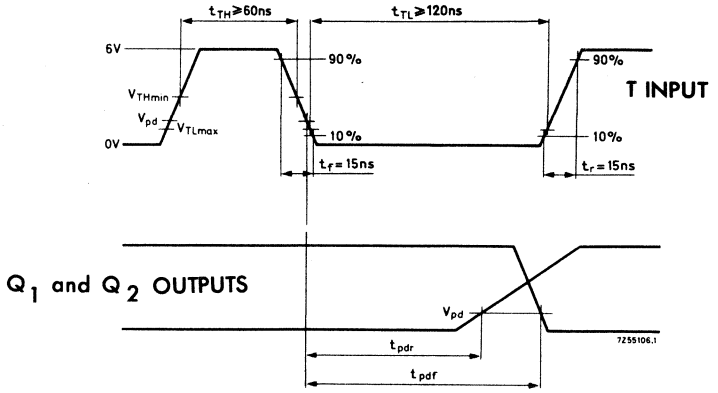
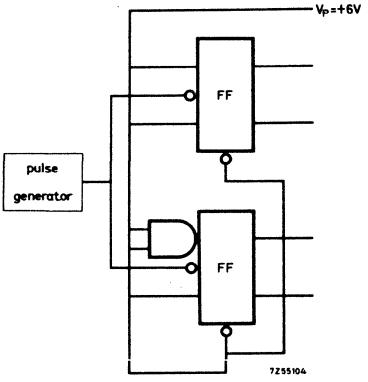


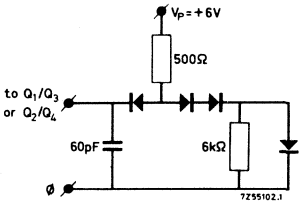
Fig. 3. Waveforms illustrating conditions for set or reset.

CHARACTERISTICS (continued)

DYNAMIC DATA

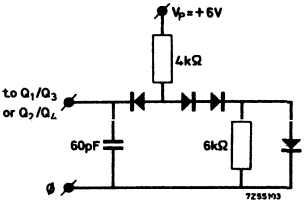






diodes FCY101

Equivalent load for N = 8 and C_L[1]) = 60 pF



diodes FCY101

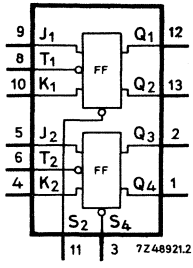
Equivalent load for N = 1 and C_L[1]) = 60 pF

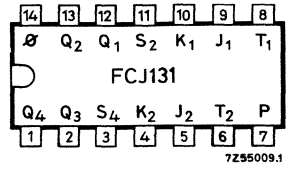
Fig. 4. Waveforms and loading circuits illustrating measurement of t_{pdr} and t_{pdf}

[1]) Including probe and jig capacitance

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

DUAL JK MASTER-SLAVE FLIP FLOP



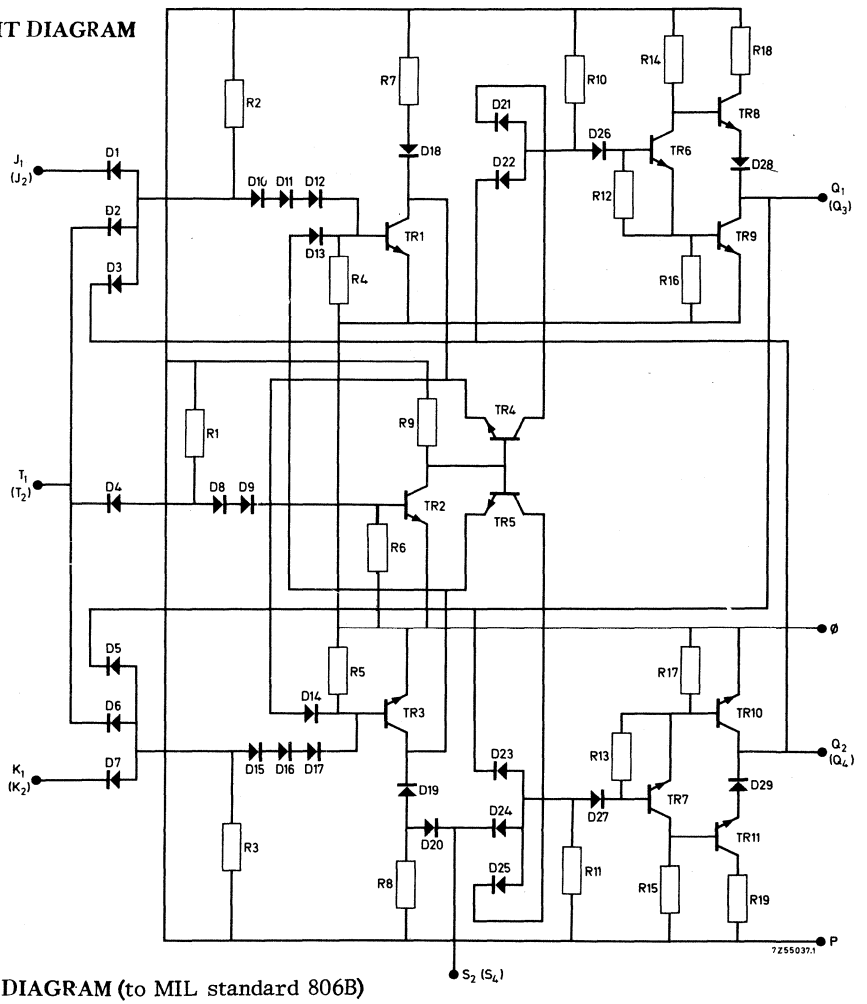


QUICK REFERENCE DATA			
Supply voltage	V_P	6.0 ± 5%	V
Operating ambient temperature range	T_{amb}	0 to +75	°C
Clock rate	f_c	typ. 7	MHz
Available d.c. fan out T_{amb} = 25 °C	N_a	⩾ 8	
D.C. noise margin T_{amb} = 25 °C	M_L	typ. 1.2	V
Power consumption 50% duty cycle, T_{amb} = 25 °C	P_{av}	typ. 100	mW

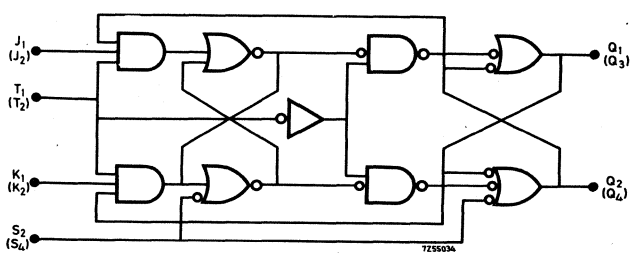
The FCJ131 comprises two independent direct coupled JK flip-flops, operating on the master-slave principle. Operation depends on voltage levels only, i.e. rise and fall times of all input signals, including the trigger signals, are immaterial. The separate set inputs (overriding any other inputs) are active at the LOW level. Typical applications include counters and shift registers.

PACKAGE OUTLINE 14 lead plastic dual in-line (type A). (See General Section)

CIRCUIT DIAGRAM



LOGIC DIAGRAM (to MIL standard 806B)



FUNCTION TABLES

1. Trigger action via T terminal (each flip-flop)

T = HIGH		T = LOW	
J_1 J_2	K_1 K_2	Q_1 Q_3	Q_2 Q_4
H	H	reversed	
L	H	L	H
H	L	H	L
L	L	no change	

The information on J and K is transferred into the master by T becoming HIGH. When T subsequently goes LOW the outputs will assume the levels shown in the table. Inputs S_2 and S_4 should be HIGH or floating.

2. Set or reset via S terminals (each flip-flop)

S_2 S_4	Q_1 Q_3	Q_2 Q_4
L	L	H
H	no change	

The set inputs override the other inputs and directly determine the outputs of the relevant flip-flop.

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.	8.0	V
Output voltage	V_Q	max.	8.0	V
Input voltage	V_J, V_K, V_T, V_S	max.	8.0	V
Output current [1]	$-I_Q$	max.	20	mA
Input current [2]	$-I_J, -I_K, -I_T, -I_S$	max.	20	mA
Voltage difference between any two inputs		max.	8.0	V
Storage temperature	T_{stg}	−55 to	+125	°C
Operating ambient temperature	T_{amb}	0 to	+75	°C

1) For negative output voltage in LOW state.
2) At this limit input voltages typ. : −1.5V.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}		0 to +75	°C
Uniform system supply voltage	V_P		5.7 to 6.3	V
Available d.c. fan out				
to T input	N_{aT}	⩾	3	
to J or K input	$N_{aJ} = N_{aK}$	⩾	10	
to S input	N_{aS}	⩾	4	
to G input	N_{aG}	⩾	8	
D.C. noise margin				
to T input	M_L	min.	0.3	V
	M_H	min.	1.2	V
to J or K input	M_L	min.	0.7	V
	M_H	min.	1.2	V
to S input	M_L	min.	0.3	V
	M_H	min.	1.9	V
to G input	M_L	min.	0.4	V
	M_H	min.	1.5	V
Average propagation delay time	t_{pd}	max.	105	ns
Maximum clock rate	f_c	⩾	5	MHz
Equivalent input capacitances				
for T input	C_T	typ.	12	pF
for J or K input	$C_J = C_K$	typ.	4	pF
for S input	C_S	typ.	8	pF
Supply current (duty cycle 50%) [1]	I_{Pav}	typ.	16.8	mA
Power dissipation at T_{amb} = 75 °C [1]	P_{tot}	max.	150	mW

[1] Both flip-flops together

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references	
		0	+25	+75		V_P (V)	
STATIC DATA							
Output voltage LOW	V_{QLmax}	0.4	0.4	0.4	V	5.7 and 6.3	
at: Output current LOW	I_{QLmax}	14.0 16.0	16.5 19.0	12.4 14.4	mA mA	5.7 6.3	
Output voltage HIGH	V_{QHmin}	3.8	3.9	4.1	V	5.7	$I_Q = -100\ \mu A$
Output voltage HIGH (lowest permissible)	V_{QHPmin}	3.6	3.3	3.0	V	5.7	
at: Output current HIGH	$-I_{QHmax}$	0.85	3.3	5.5	mA	5.7	
Input current LOW	$-I_{JLmax}$, $-I_{KLmax}$	1.4 1.6	1.3 1.5	1.2 1.4	mA mA	5.7 6.3	$V_J = V_K = 0.4$ V; other inputs floating
	$-I_{TLmax}$	4.0 4.5	3.8 4.2	3.5 3.9	mA mA	5.7 6.3	$V_T = 0.4$ V; other inputs floating
	$-I_{SLmax}$	2.9 3.3	2.8 3.2	2.6 2.9	mA mA	5.7 6.3	$V_S = 0.4$ V; other inputs floating
Input current HIGH	I_{JHmax}, I_{KHmax}	1	1	25	μA	5.7	$V_J = V_K = 5.3$ V other inputs 0 V
	I_{THmax}	3	3	75	μA	5.7	$V_T = 5.3$ V other inputs 0 V
	I_{SHmax}	2	2	50	μA	5.7	$V_S = 5.3$ V other inputs 0 V
Supply current (both flip-flops together)	I_{Pmax}	–	26.7	–	mA	6.3	T inputs LOW J, K, S inputs HIGH

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references		
		0	+25	+75		V_P (V)		fig.
DYNAMIC DATA						5.7 and 6.3		
Change of state								
Input voltage HIGH during:	V_{THmin} V_{JHmin} V_{KHmin}	2.6	2.3	1.9	V		HIGH level at T and J and/or K to be present simultaneously	1
Input time HIGH to:	t_{THmin}	60	60	60	ns			1
T-input voltage LOW	V_{TLmax}	1.0	1.0	0.7	V		$t_{TLmin} = t_{pdf}$	1
No change of state								
J/K input voltage LOW	V_{JLmax} V_{KLmax}	1.6	1.4	1.1	V		LOW level at J and K to be present prior to T turning HIGH and to remain present during T is HIGH	2
Clock skew protection								
Hold time	$t_{hold\,max}$	10	10	10	ns			2
Reset								
S input voltage LOW	V_{SLmax}	1.0	1.0	0.7	V		active $t_{SLmin} = t_{pdf}$	3
S input voltage HIGH	V_{SHmin}	1.9	1.8	1.6	V		inactive	
DYNAMIC DATA								
Propagation delay times from T to Q								
Rise propagation delay time	$t_{pdr\,max}$	–	90	–	ns	6.0	V_{pd} = 1.5 V N = 1; C_L = 60 pF	4
Fall propagation delay time	$t_{pdf\,max}$	–	120	–	ns	6.0	V_{pd} = 1.5 N = 8; C_L = 60 pF other output: N = 1; C_L = 60 pF	4

CHARACTERISTICS (continued)

DYNAMIC DATA

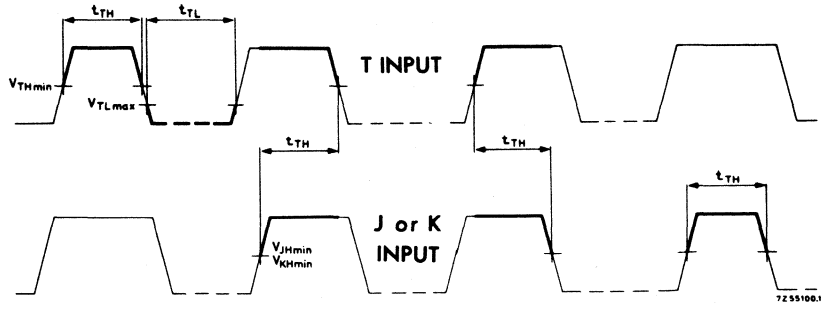


Fig. 1. Waveforms illustrating conditions for change of state.

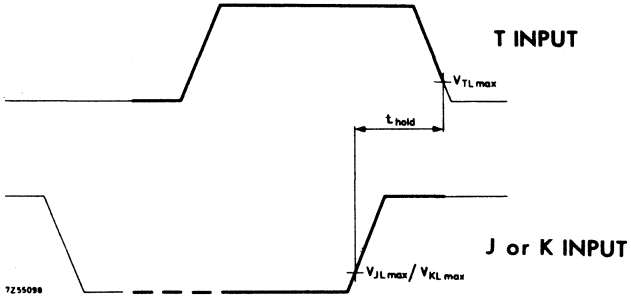


Fig. 2. Waveforms illustrating conditions for no change of state.

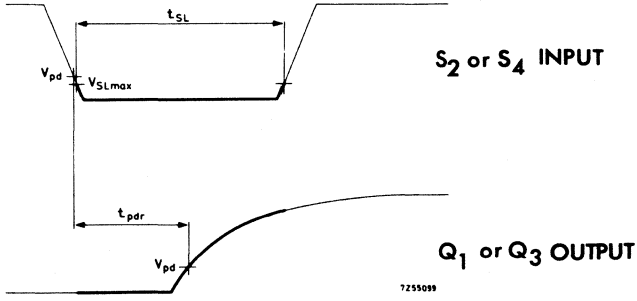
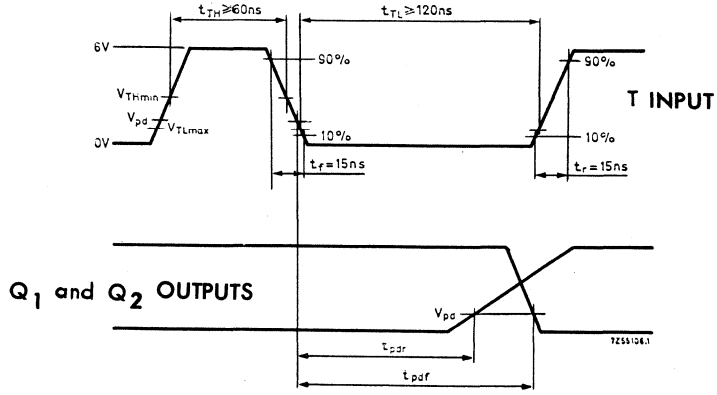
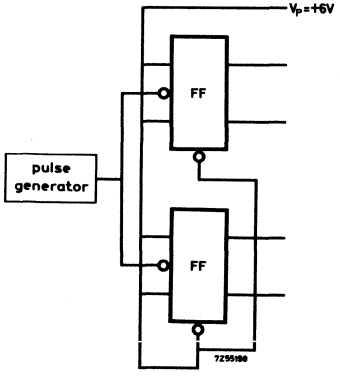


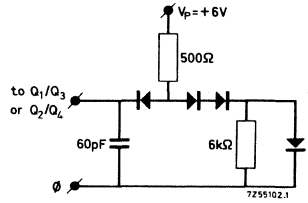
Fig. 3. Waveforms illustrating conditions for set or reset.

CHARACTERISTICS (continued)

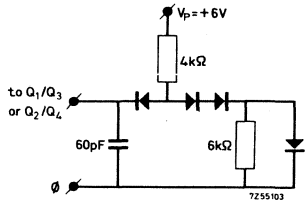
DYNAMIC DATA







Diodes FCY101
Equivalent load for N = 8 and C_L[1]) = 60 pF



Diodes FCY101
Equivalent load for N = 1 and C_L[1]) = 60 pF

Fig. 4. Waveforms and loading circuits illustrating measurement of t_{pdr} and t_{pdf}.
1) Including probe and jig capacitance

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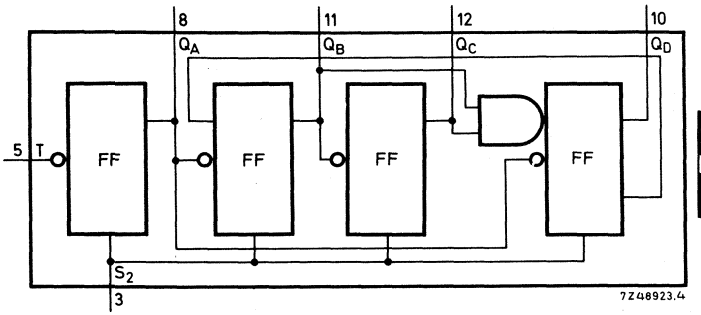
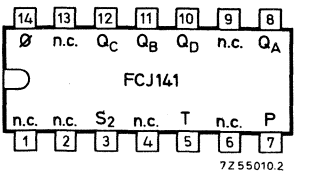
SINGLE ASYNCHRONOUS 10-COUNTER



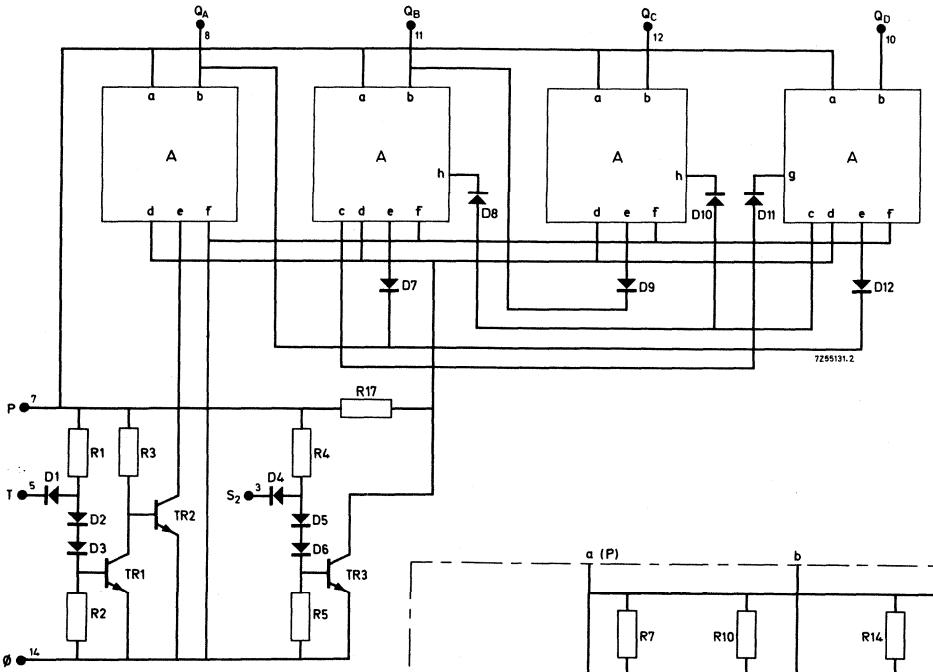


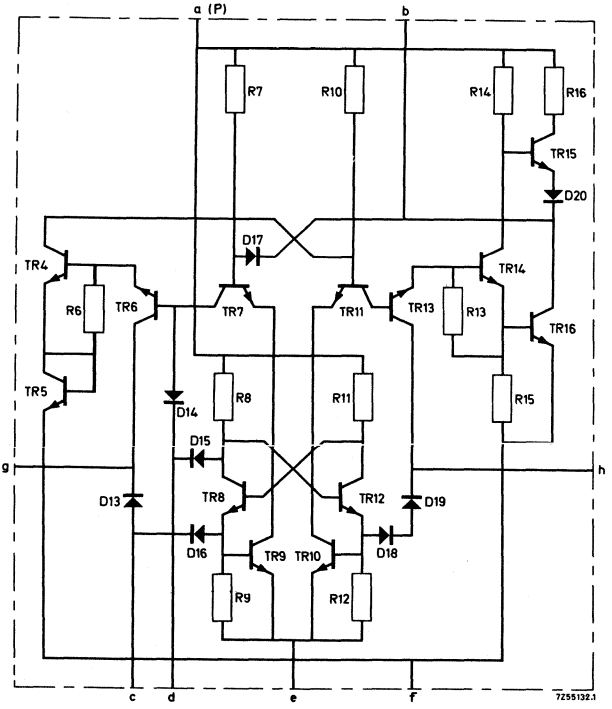
QUICK REFERENCE DATA			
Supply voltage	V_P	$6.0 \pm 5\%$	V
Operating ambient temperature range	T_{amb}	0 to +75	°C
Clock rate	f_c	typ. 7	MHz
Available d.c. fan out T_{amb} = 25 °C	N_a	⩾ 8	
D.C. noise margin T_{amb} = 25 °C	M_L	typ. 1.2	V
Power consumption 50% duty cycle, T_{amb} = 25 °C	P_{av}	typ. 180	mW

The FCJ141 is four master-slave flip-flops interconnected to form an a-synchronous decade counter in the 8-4-2-1 code. The information is transferred to the master when the trigger signal is HIGH (the first flip-flop is triggered by the count input at T). When the trigger signal is LOW the information is transferred to the slaves and appears at the outputs. A common reset input S_2 directly resets the outputs and overrides the T input.

PACKAGE OUTLINE: 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAMS





block A

FUNCTION TABLES

Count	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

S_2	Q_D	Q_C	Q_B	Q_A
L	count			
H	L	L	L	L

Input S when being at the HIGH state overrides the count input and directly resets all outputs in the LOW state

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	8.0	V
Input voltage	V_T; V_S	max.	8.0	V
Output voltage	V_Q	max.	8.0	V
Input current [1]	$-I_S$; $-I_T$	max.	20	mA
Output current [2]	$-I_Q$	max.	20	mA
Voltage difference between any two inputs		max.	8.0	V
Storage temperature	T_{stg}	−35 to +125		°C
Operating ambient temperature	T_{amb}	0 to +75		°C

1) At this limit, input voltage typ. −1.5 V.

2) For negative output voltage in LOW state.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}		0 to +75	°C
Uniform system supply voltage	V_P		5.7 to 6.3	V
Available d.c. fan out	N_a	≥	8	
D.C. noise margin				
to T input	M_L	min.	0.4	V
	M_H	min.	1.6	V
to S input	M_L	min.	0.4	V
	M_H	min.	1.6	V
Average propagation delay time T input to Q_3 output	t_{pd}	typ.	200	ns
Clock rate	f_c	max.	3.5	MHz
Equivalent input capacitances				
for T input	C_T	typ.	4	pF
for S input	C_S	typ.	4	pF
Supply current (duty cycle 50%)	I_{Pav}	max.	46	mA
Power dissipation at $T_{amb} = 75\,^{o}C$	P_{tot}	max.	270	mW

CHARACTERISTICS

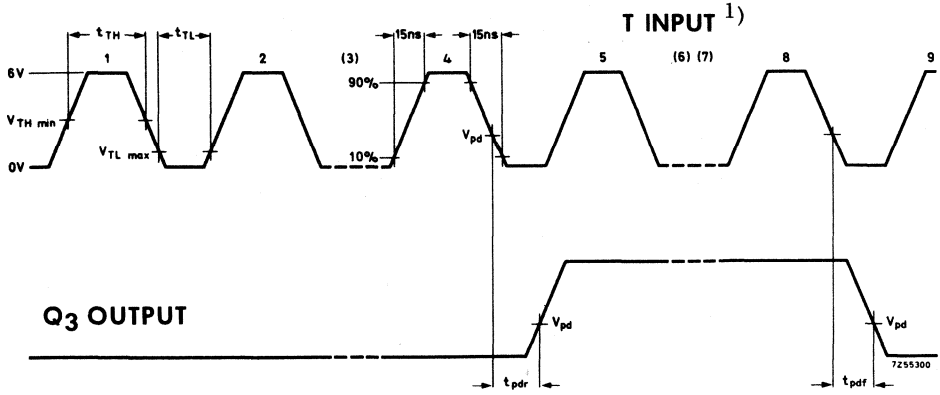
		T_{amb} (°C)				Conditions and references	
		0	25	75		V_P (V)	
STATIC DATA							
Output voltage LOW	V_{QL} max.	0.4	0.4	0.4	V	5.7 and 6.3	
at: Output current LOW	I_{QLmax}	14.0	13.2	12.4	mA	5.7	
	I_{QLmax}	16.0	15.2	14.4	mA	6.3	
Output voltage HIGH	V_{QH} min.	3.8	3.9	4.1	V	5.7	
at: Output current HIGH	$-I_{QH}$	100	100	100	µA	5.7	
Output voltage HIGH (lowest permissible)	V_{QHP} min.	3.6	3.3	3.0	V	5.7	
at: Output current HIGH	$-I_{QHmax}$	0.85	3.3	5.5	mA	5.7	
Input current LOW	$-I_{TL}$ max.	1.75	1.65	1.55	mA	5.7	$V_T = V_S = 0.4$ V
	$-I_{SL}$ max.	1.75	1.65	1.55	mA	5.7	
	$-I_{TL}$ max.	2.0	1.9	1.8	mA	6.3	
	$-I_{SL}$ max.	2.0	1.9	1.8	mA	6.3	
Input current HIGH	I_{TH} max. I_{SH} max.	1.0	1.0	25.0	µA	5.7	$V_T = V_S = 5.3$ V
Supply current	I_{Pmax}	–	45	40	mA	6.3	$V_T = 0$ V, V_S = floating

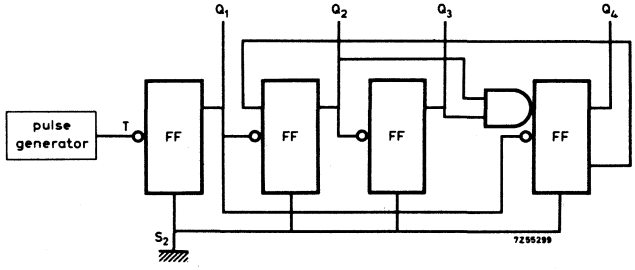
CHARACTERISTICS (continued)

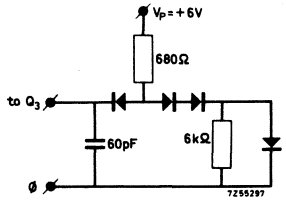
STATIC AND DYNAMIC DATA		T_{amb} (°C) 0	25	75		Conditions and references V_P (V)	
Reset input active HIGH level at S	V_{SHmin}	2.3	2.2	2.1	V	5.7 and 6.3	
to be present during	t_{SHmin}	100	100	140	ns		
Reset input inactive LOW level at S	V_{SLmax}	1.0	1.0	0.8	V	5.7 and 6.3	
Change of state of the master of the lowest order flip-flop HIGH level at T	V_{THmin}	2.3	2.2	2.1	V	5.7 and 6.3	
to be present during	t_{THmin}	-	100	-	ns		
Change of state of the slave of the lowest order flip-flop Slope of falling edge at T	$(-\frac{dt}{dV})_{Tmax}$	1	1	1	µs/V		
LOW level at T	V_{TLmax}	1.0	1.0	0.8	V	5.7 and 6.3	
to be present during	t_{TLmin}	100	100	140	ns		
Propagation delay times from T to Q_3							
Propagation delay reference level	V_{pd}		1.5		V		
Rise propagation delay time	$t_{pdr\ max}$	-	200	-	ns	6.0	
Fall propagation delay time	$t_{pdf\ max}$	-	200	-	ns	6.0	

CHARACTERISTICS (continued)

DYNAMIC DATA



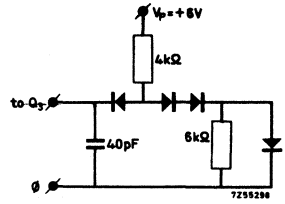




diodes FCY101

C_L 2) = 60 pF

Equivalent load for N = 6



diodes FCY101

C_L 2) = 40 pF

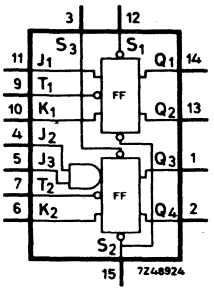
Equivalent load for N = 1

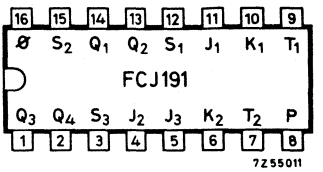
1) The falling edge of the T input signals is max. 1 µs/V

2) Including jig and probe capacitance

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

DUAL JK MASTER-SLAVE FLIP-FLOP



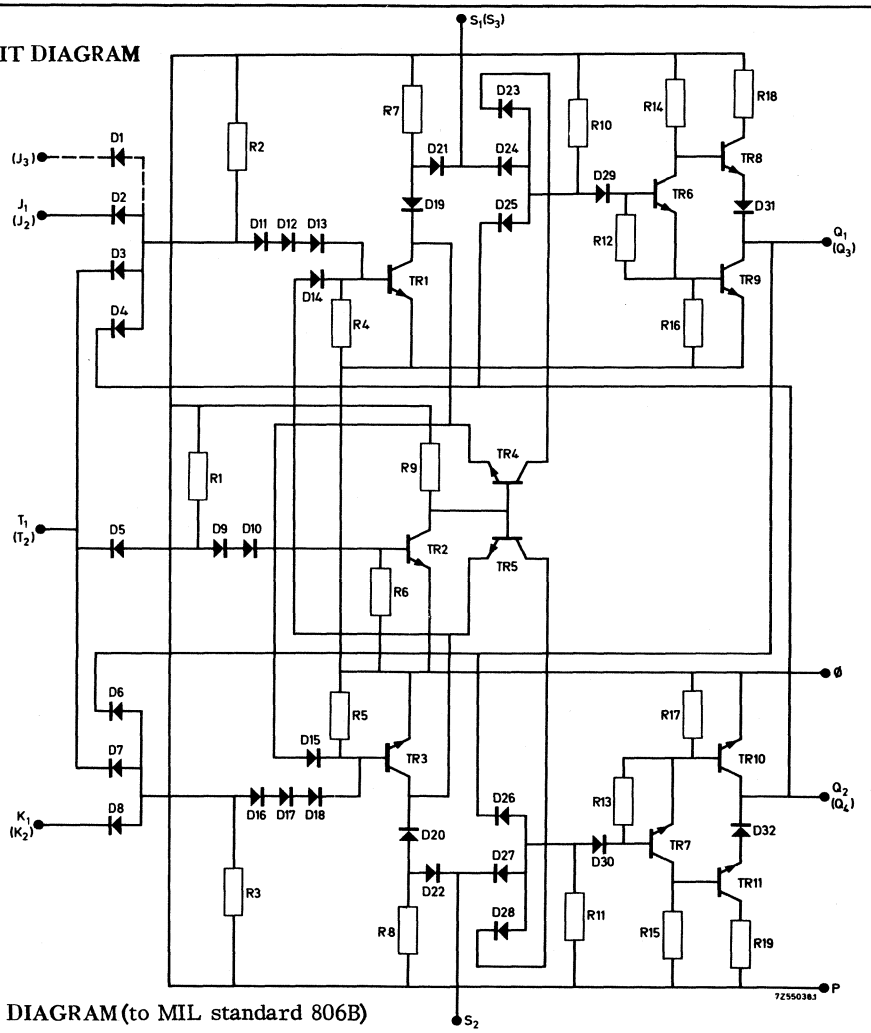


QUICK REFERENCE DATA			
Supply voltage	V_P	6.0 ± 5%	V
Operating ambient temperature range	T_{amb}	0 to +75	°C
Clock rate	f_c	typ. 7	MHz
Available d.c. fan-out T_{amb} = 0 to +75 °C	N_a	⩾ 8	
D.C. noise margin T_{amb} = 25 °C	M_L	typ. 1.2	V
Power consumption 50% duty cycle, T_{amb} = 25 °C	P_{av}	typ. 100	mW

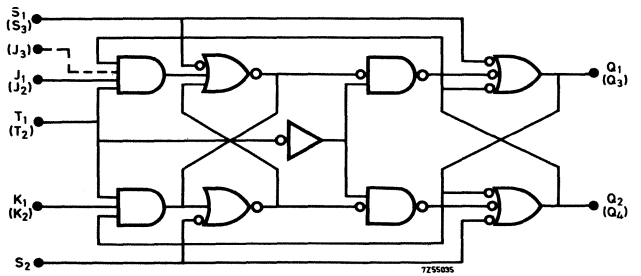
The FCJ191 comprises two independent direct coupled JK flip-flops, operating on the master-slave principle. Operation depends on voltage levels only, e.g. rise and fall times of all input signals including the trigger signal are immaterial. The set and reset inputs (overriding any other inputs) are active at the LOW level. Typical applications include counters and shift registers.

PACKAGE OUTLINE 16 lead plastic dual in-line (type A). (See General Section)

CIRCUIT DIAGRAM



LOGIC DIAGRAM (to MIL standard 806B)



FUNCTION TABLES

1. Trigger action via T terminal (each flip-flop)

T = HIGH		T = LOW	
J_1 J	K_1 K_2	Q_1 Q_3	Q_2 Q_4
H	H	reversed	
L	H	L	H
H	L	H	L
L	L	no change	

The information or J and K is transferred into the master by T becoming HIGH. When T subsequently goes LOW the outputs will assume the levels shown in the table. Inputs S_1, S_2 and S_3 should be HIGH or floating.

For the flip-flop with two J-inputs is $J = J_2 \cdot J_3$ for positive logic

2. Set or reset via S terminals

S_1 S_3	S_2 S_2	Q_1 Q_3	Q_2 Q_4
H	L	L	H
L	H	H	L
L	L	H	H
H	H	no change	

The set inputs override the other inputs and directly determine the outputs of the relevant flip-flop.

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.	8.0	V
Output voltage	V_Q	max.	8.0	V
Input voltage	V_J, V_K, V_T, V_S	max.	8.0	V
Output current [1]	$-I_Q$	max.	20	mA
Input current [2]	$-I_J, -I_K, -I_T, -I_S$	max.	20	mA
Voltage difference between any two inputs		max.	8.0	V
Storage temperature	T_{stg}	−55 to +125		°C
Operating ambient temperature	T_{amb}	0 to +75		°C

1) For negative output voltage in LOW state.
2) At this limit input voltage typ. : −1.5 V

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to +75		°C
Uniform system supply voltage	V_P	5.7 to 6.3		V
Available d.c. fan out				
to T input	N_{aT}	⩾	3	
to J or K input	$N_{aJ} = N_{aK}$	⩾	10	
to S input	N_{aS2}	⩾	2	
	$N_{aS1} = N_{aS3}$	⩾	4	
to G input	N_{aG}	⩾	8	
D.C. noise margin				
to T input	M_L	min.	0.3	V
	M_H	min.	1.2	V
to J or K input	M_L	min.	0.7	V
	M_H	min.	1.2	V
to S input	M_L	min.	0.3	V
	M_H	min.	1.9	V
to G input	M_L	min.	0.4	V
	M_H	min.	1.5	V
Average propagation delay time	t_{pd}	max.	105	ns
Maximum clock rate	f_c	⩾	5	MHz
Equivalent input capacitances				
for T input	C_T	typ.	12	pF
for J or K input	$C_J = C_K$	typ.	4	pF
for S input	C_{S2}	typ.	16	pF
	$C_{S1} = C_{S3}$	typ.	8	pF
Supply current (duty cycle 50%) [1]	I_{Pav}	typ.	16.8	mA
Power dissipation at T_{amb} = 75 °C [1]	P_{tot}	max.	150	mW

[1]) Both flip-flops together

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references	
		0	+25	+75		V_P (V)	
STATIC DATA							
Output voltage LOW	V_{QLmax}	0.4	0.4	0.4	V	5.7 and 6.3	
at: Output current LOW	I_{QLmax}	14.0 16.0	16.5 19.0	12.4 14.4	mA mA	5.7 6.3	
Output voltage HIGH	V_{QHmin}	3.8	3.9	4.1	V	5.7	I_Q = −100 μA
Output voltage HIGH (lowest permissible)	V_{QHPmin}	3.6	3.3	3.0	V	5.7	
at: Output current HIGH	$-I_{QHmax}$	0.85	3.3	5.5	mA	5.7	
Input current LOW	$-I_{JLmax}$, $-I_{KLmax}$	1.4 1.6	1.3 1.5	1.2 1.4	mA mA	5.7 6.3	$V_J = V_K = 0.4$ V; other inputs floating
	$-I_{TLmax}$	4.0 4.5	3.8 4.2	3.5 3.9	mA mA	5.7 6.3	$V_T = 0.4$ V; other inputs floating
	$-I_{S2Lmax}$	5.7 6.6	5.5 6.3	5.2 5.8	mA mA	5.7 6.3	$V_S = 0.4$ V; other inputs floating
	$-I_{S1Lmax}$ $-I_{S3Lmax}$	2.9 3.3	2.8 3.2	2.6 2.9	mA mA	5.7 6.3	$V_S = 0.4$ V; other inputs floating
Input current HIGH	I_{JHmax}, I_{KHmax}	1	1	25	μA	5.7	$V_J = V_K = 5.3$ V other inputs 0 V
	I_{THmax}	3	3	75	μA	5.7	$V_T = 5.3$ V other inputs 0 V
	I_{S2Hmax}	4	4	100	μA	5.7	$V_S = 5.3$ V other inputs 0 V
	I_{S1Hmax} I_{S3Hmax}	2	2	50	μA	5.7	$V_S = 5.3$ V other inputs 0 V
Supply current (both flip-flops together)	I_{Pmax}	–	26.7	–	mA	6.3	T input LOW J, K, S inputs HIGH

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references		
		0	+25	+75		V_P (V)		fig.
DYNAMIC DATA						5.7 and 6.3		
Change of state								
Input voltage HIGH during:	V_{THmin} V_{JHmin} V_{KHmin}	2.6	2.3	1.9	V		HIGH level at T and J and/or K to be present simultaneously	1
Input time HIGH to:	t_{THmin}	60	60	60	ns			1
T-input voltage LOW	V_{TLmax}	1.0	1.0	0.7	V		$t_{TLmin} = t_{pdf}$	1
No change of state								
J/K input voltage LOW	V_{JLmax} V_{KLmax}	1.6	1.4	1.1	V		LOW level at J and K to be present prior to T turning HIGH and to remain present during T is HIGH	2
Clock skew protection								
Hold time	$t_{hold\,max}$	10	10	10	ns			2
Reset								
S input voltage LOW	V_{SLmax}	1.0	1.0	0.7	V		active $t_{SLmin} = t_{pdf}$	3
S input voltage HIGH	V_{SHmin}	1.9	1.8	1.6	V		inactive	
DYNAMIC DATA								
Propagation delay times from T to Q								
Rise propagation delay time	$t_{pdr\,max}$	-	90	-	ns	6.0	$V_{pd} = 1.5$ V N = 1; $C_L = 60$ pF	4
Fall propagation delay time	$t_{pdf\,max}$	-	120	-	ns	6.0	$V_{pd} = 1.5$ N = 8; $C_L = 60$ pF other output: N = 1; $C_L = 60$ pF	4

CHARACTERISTICS (continued)

DYNAMIC DATA

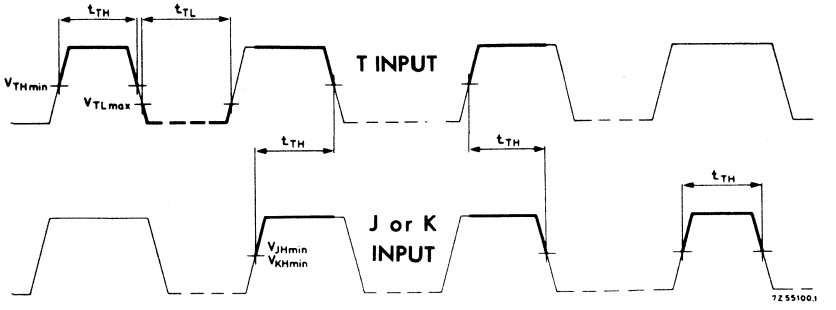


Fig. 1. Waveforms illustrating conditions for change of state.

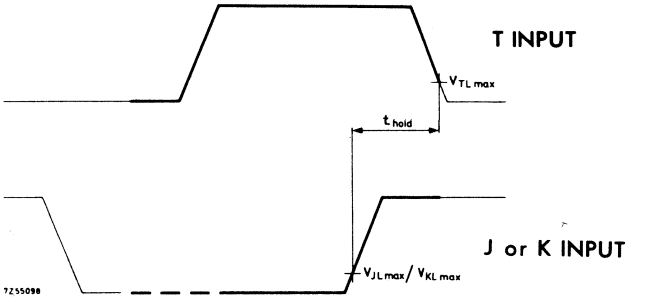


Fig. 2. Waveforms illustrating conditions for no change of state.

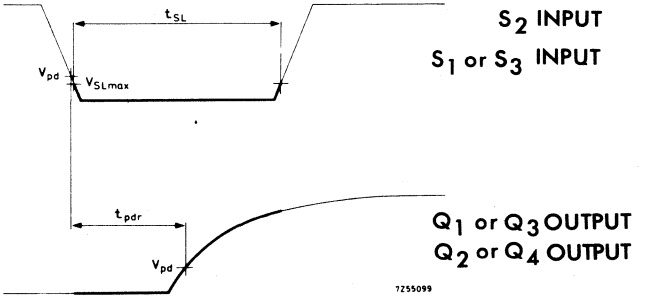
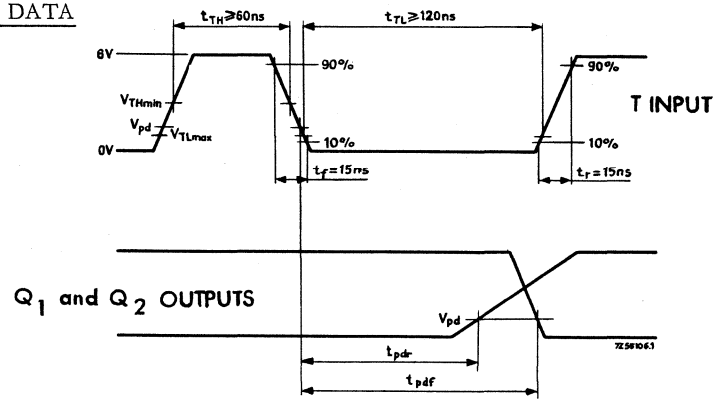
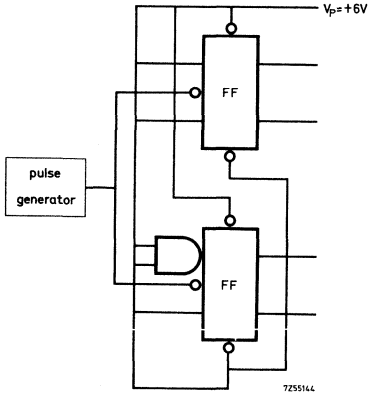


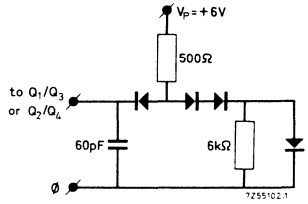
Fig. 3. Waveforms illustrating conditions for set or reset.

CHARACTERISTICS (continued)

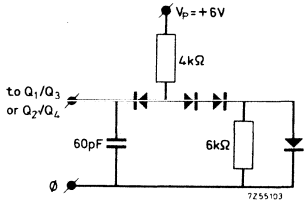
DYNAMIC DATA







Diodes FCY101
Equivalent load for N = 8 and C_L[1]) = 60 pF

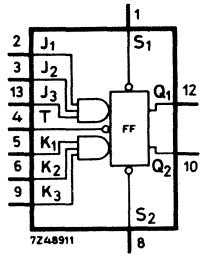


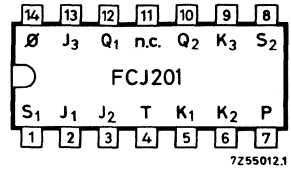
Diodes FCY101
Equivalent load for N = 1 and C_L[1]) = 60 pF

Fig. 4. Waveforms and loading circuits illustrating measurement of t_{pdr} and t_{pdf}.
1) Including probe and jig capacitance

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

SINGLE JK MASTER-SLAVE FLIP-FLOP



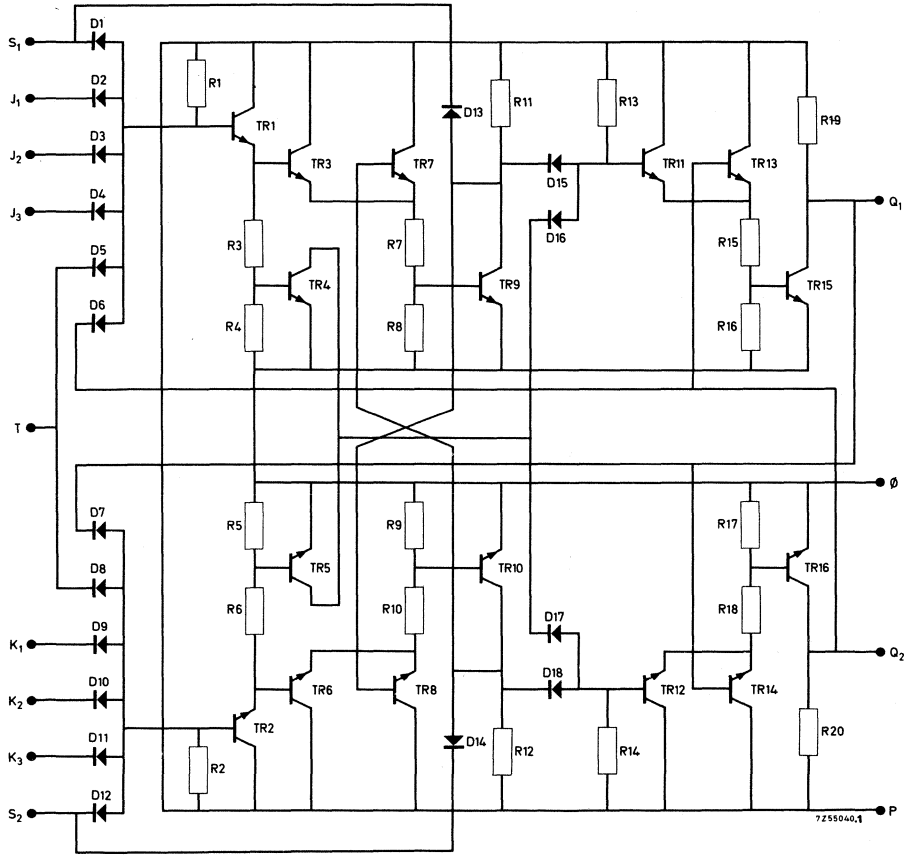


QUICK REFERENCE DATA			
Supply voltage	V_P	6.0 ± 5%	V
Operating ambient temperature range	T_{amb}	0 to +75	°C
Clock rate	f_c	typ. 5	MHz
Available d.c. fan out T_{amb} = 0 to +75 °C	N_a	⩾ 8	
D.C. noise margin T_{amb} = 25 °C	M_L	typ. 1.2	V
Power consumption 50% duty cycle, T_{amb} = 25 °C	P_{av}	typ. 67	mW

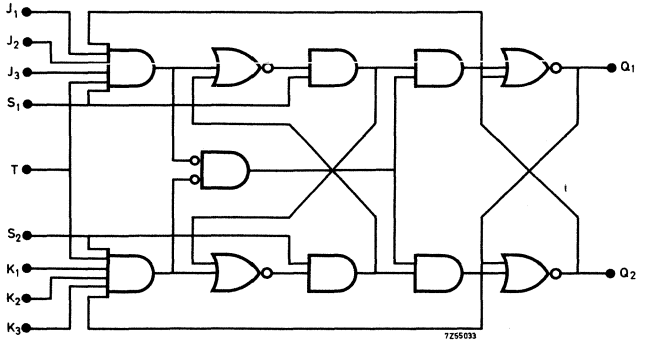
The FCJ201 is a direct-coupled JK flip-flop, operating on the master-slave principle. Operation depends on voltage levels only, i.e. rise and fall times of all input signals, including the trigger signal, are immaterial. The J, K and T inputs are logically equivalent, allowing the use of J and K for triggering. The direct set inputs (overriding any other inputs) are active at the LOW level.

PACKAGE OUTLINE: 14 lead plastic dual in-line (type A). (See General Section)

CIRCUIT DIAGRAM



LOGIC DIAGRAM (to MIL standard 806B)



FUNCTION TABLES

1. Trigger action via T terminal (each flip-flop)

T = HIGH		T = LOW	
J	K	Q_1	Q_2
H	H	reversed	
L	H	L	H
H	L	H	L
L	L	no change	

The information on J and K is transferred into the master by T becoming HIGH. When T subsequently goes LOW the outputs will assume the levels shown in the table. Inputs S_1 and S_2 should be HIGH or floating.

$J = J_1.J_2.J_3$; $K = K_1.K_2.K_3$ (for positive logic)

2. Trigger action via J and K terminals

J	K	Q_1	Q_2
H→L	X	H	L
X	H→L	L	H
H→L	H→L	reversed	

$J = J_1.J_2.J_3$; $K = K_1.K_2.K_3$
(for positive logic)

If J or K go LOW with T HIGH, Q_1 and Q_2 assume the state shown. If both J and K go LOW with T HIGH, the outputs of Q_1 and Q_2 are reversed (exactly as if J and K remained HIGH and T were triggered). When triggering on J and K the T input requirements V_{TH} and V_{TL} (see CHARACTERISTICS) apply to J and K. S_1 and S_2 should be HIGH or floating.

3. Set or reset via S terminals

S_1	S_2	Q_1	Q_2
H	L	L	H
L	H	H	L
L	L	indeterminate	
H	H	no change	

The set inputs override the other inputs and directly determine the output of the flip-flop.
In the case of both set inputs going LOW the first to reach LOW will determine the output conditions.

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS (Limiting values) [1])

Supply voltage	V_P	max.	8.0	V
Output voltage	V_Q	max.	8.0	V
Input voltage	V_J, V_K, V_T, V_S	max.	8.0	V
Output current [2])	$-I_Q$	max.	20	mA
Input current [3])	$-I_J, -I_K, -I_T, -I_S$	max.	20	mA
Voltage difference between any two inputs		max.	8.0	V
Storage temperature	T_{stg}	−55 to	+125	°C
Operating ambient temperature	T_{amb}	0 to	+75	°C

1) Limiting values according to the Absolute Maximum System as defined in IEC publication 134.
2) For negative output voltage.
3) At this limit input voltage type.: −1.5 V.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to +75		°C
Uniform system supply voltage	V_P	5.7 to 6.3		V
Available d.c. fan out				
to T input	N_{aT}	⩾	4	
to J or K input	$N_{aJ} = N_{aK}$	⩾	8	
to S input	N_{aS}	⩾	5	
to G input	N_{aG}	⩾	8	
D.C. noise margin				
to T input	M_L	min.	0.5	V
	M_H	min.	1.9	V
to J or K input	M_L	min.	0.9	V
	M_H	min.	1.9	V
to S input	M_L	min.	0.4	V
	M_H	min.	1.9	V
to G input	M_L	min.	0.4	V
	M_H	min.	2.3	V
Average propagation delay time	t_{pd}	max.	150	ns
Maximum clock rate	f_c	⩾	3	MHz
Equivalent input capacitances				
for T input	C_T	typ.	8	pF
for J or K input	$C_J = C_K$	typ.	4	pF
for S input	C_S	typ.	8	pF
Supply current (duty cycle 50%)	I_{Pav}	typ.	11.2	mA
Power dissipation at T_{amb} = 75 °C	P_{tot}	max.	110	mW

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references	
		0	+25	+75		V_P (V)	
STATIC DATA							
Output voltage LOW	V_{QLmax}	0.4	0.4	0.4	V	5.7 and 6.3	
at: Output current LOW	I_{QLmax}	14.0 16.0	13.2 15.2	12.4 14.4	mA mA	5.7 6.3	
Output voltage HIGH	V_{QHmin}	5.3	5.4	5.3	V	5.7	$I_Q = 0$
Output voltage HIGH (lowest permissible)	V_{QHPmin}	3.9	3.5	2.8	V	5.7	
at: Output current HIGH	$-I_{QHmax}$	350	450	550	μA	5.7	
Input current LOW	$-I_{JLmax}$, $-I_{KLmax}$	1.75 2.0	1.65 1.9	1.55 1.8	mA mA	5.7 6.3	$V_J = V_K = 0.4$ V; other inputs floating
	$-I_{TLmax}$	3.5 4.0	3.3 3.8	3.1 3.6	mA mA	5.7 6.3	$V_T = 0.4$ V; other inputs floating
	$-I_{SLmax}$	2.7 3.0	2.6 2.9	2.4 2.7	mA mA	5.7 6.3	$V_S = 0.4$ V; other inputs floating
Input current HIGH	I_{JHmax}, I_{KHmax}	1	1	25	μA	5.7	$V_J = V_K = 5.3$ V other inputs 0 V
	I_{THmax}	2	2	50	μA	5.7	$V_T = 5.3$ V other inputs 0 V
	I_{SHmax}	2	2	50	μA	5.7	$V_S = 5.3$ V other inputs 0 V
Supply current	I_{Pmax}	–	20	–	mA	6.3	J, K, S, T inputs HIGH

CHARACTERISTICS

		T_{amb} (°C)			Conditions and references		
		0	+25	+75	V_P (V)		fig.
DYNAMIC DATA					5.7 and 6.3		
Change of state							
Input voltage HIGH during: T-input time HIGH to: Input voltage LOW	V_{THmin} V_{JHmin} V_{KHmin}	3.1	2.9	2.5 V		HIGH level at T and J and/or K to be present simultaneously	1
	t_{THmin}	100	100	100 ns			1
	V_{TLmax}	1.3	1.1	0.9 V		$t_{TLmin} = t_{pdr}$	1
No change of state							
JK input voltage LOW	V_{JLmax} V_{KLmax}	1.8	1.6	1.3 V		LOW level at J and K to be present prior to T turning HIGH and to remain present during T is HIGH	2
Clock skew protection							
Hold time	$t_{holdmax}$	20	20	20 ns			2
Set or Reset							
S input voltage LOW	V_{SLmax}	1.2	1.0	0.8 V		active $t_{SLmin} = t_{pdr}$	3
S input voltage HIGH	V_{SHmin}	3.1	2.9	2.5 V		inactive	
DYNAMIC DATA							
Propagation delay times from T to Q							
Rise propagation delay time	t_{pdrmax}	–	200	– ns		$V_{pd} = 1.5$ V $N = 1$; $C_L = 60$ pF other output $N = 8$; $C_L = 56$ pF	4
Fall propagation delay time	t_{pdfmax}	–	100	– ns		$V_{pd} = 1.5$ V $N = 8$; $C_L = 56$ pF	4

CHARACTERISTICS (continued)

DYNAMIC DATA

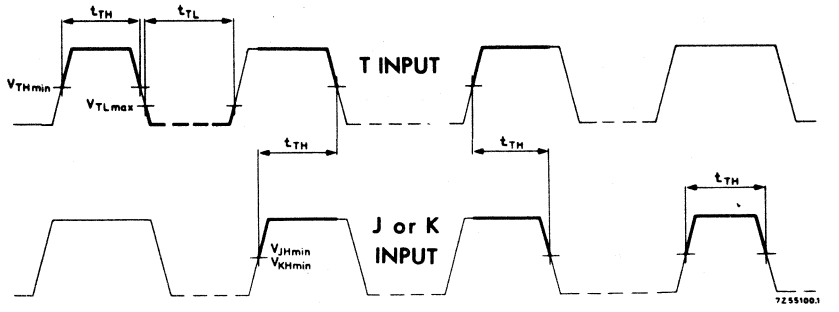


Fig. 1. Waveforms illustrating conditions for change of state.

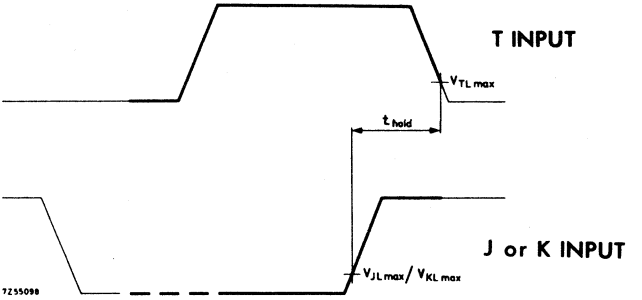


Fig. 2. Waveforms illustrating conditions for no change of state.

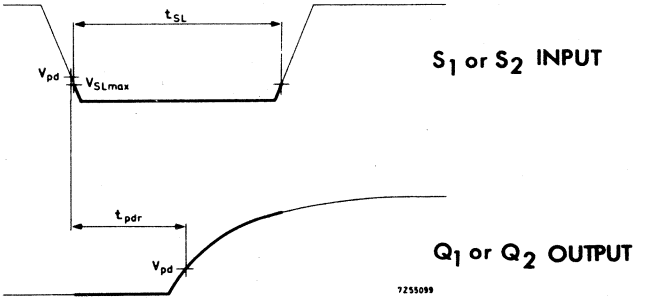
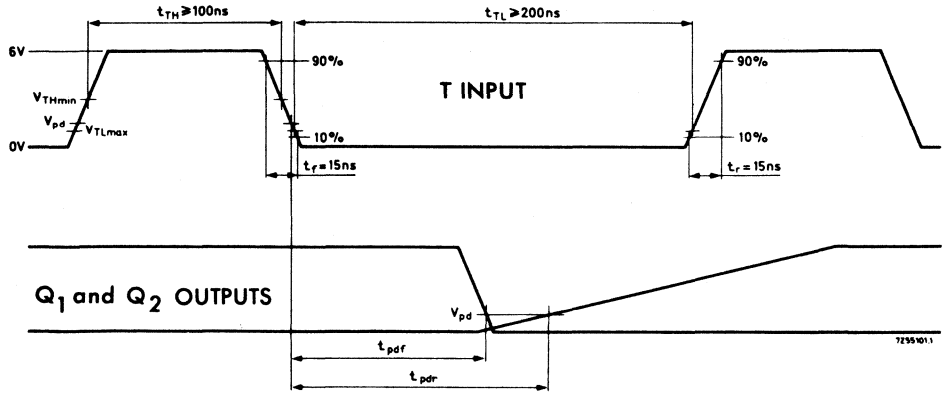
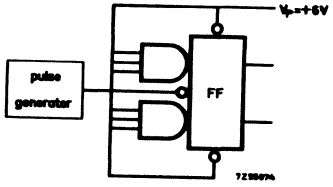


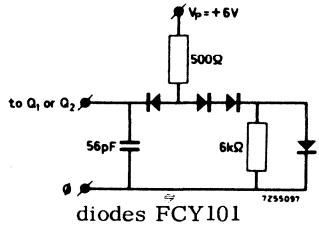
Fig. 3. Waveforms illustrating conditions for set or reset.

CHARACTERISTICS (continued)

DYNAMIC DATA

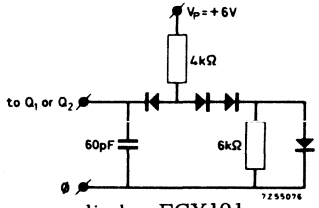






diodes FCY101

Equivalent load for N = 8 and C_L[1]) = 56 pF



diodes FCY101

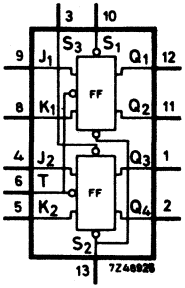
Equivalent load for N = 1 and C_L[1]) = 60 pF

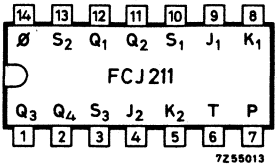
Fig. 4. Waveforms and loading circuits illustrating measurement of t_{pdr} and t_{pdf}.

1) Including probe and jig capacitance

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

DUAL JK MASTER SLAVE FLIP-FLOP



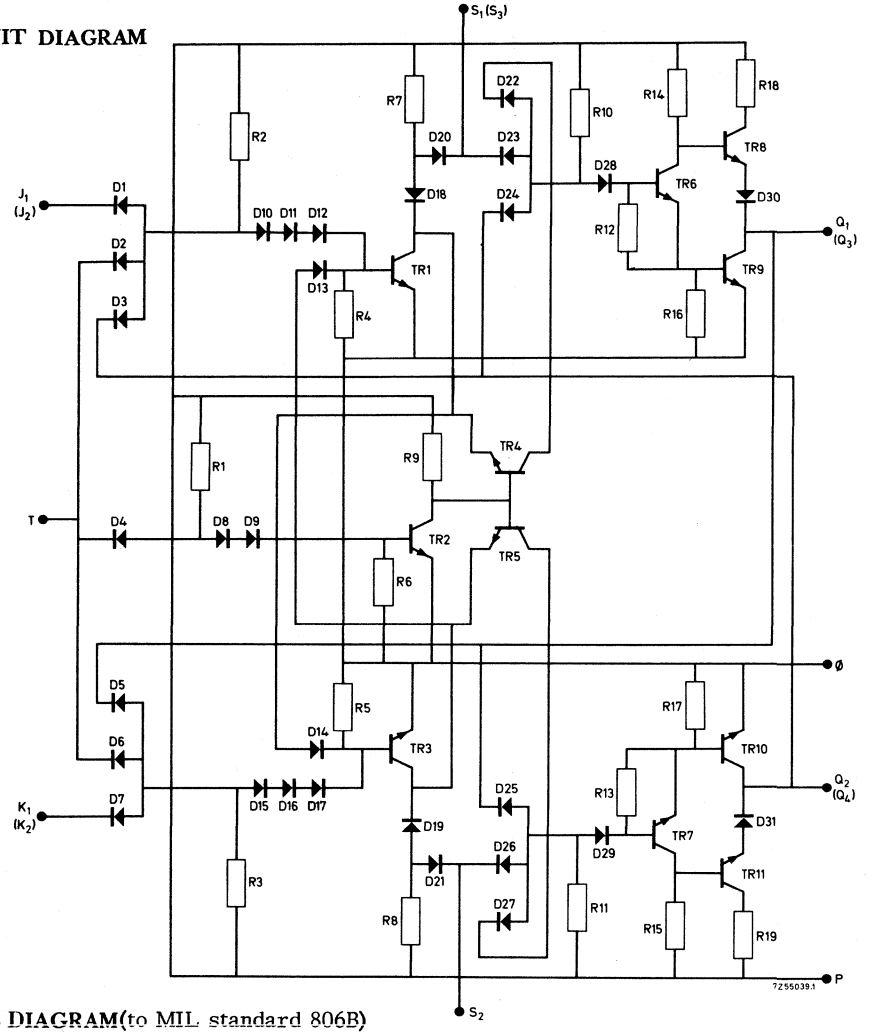


QUICK REFERENCE DATA			
Supply voltage	V_P	6.0 ± 5%	V
Operating ambient temperature range	T_{amb}	0 to +75	°C
Clock rate	f_c	typ. 7	MHz
Available d.c. fan-out T_{amb} = 0 to +75 °C	N_a	⩾ 8	
D.C. noise margin T_{amb} = 25 °C	M_L	typ. 1.2	V
Power consumption 50% duty cycle, T_{amb} = 25 °C	P_{av}	typ. 100	mW

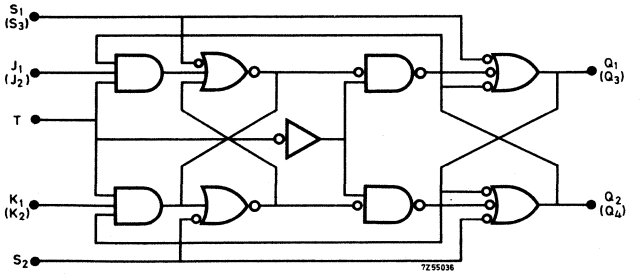
The FCJ211 comprises two independent direct-coupled JK flip-flops, operating on the master-slave principle. Operation depends on voltage levels only, i.e. rise and fall times of all input signals, including trigger signals, are immaterial. The set and reset inputs (overriding any other inputs) are active at the LOW level. Typical applications include synchronous counters and shift registers.

PACKAGE OUTLINE 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAM



LOGIC DIAGRAM(to MIL standard 806B)



FUNCTION TABLES

1. Trigger action via T terminal (each flip-flop)

T = HIGH		T = LOW	
J_1 J	K_1 K_2	Q_1 Q_3	Q_2 Q_4
H	H	reversed	
L	H	L	H
H	L	H	L
L	L	no change	

The information on J and K is transferred into the master by T becoming HIGH. When T subsequently goes LOW the outputs will assume the levels shown in the table. Inputs S_1, S_2 and S_3 should be HIGH or floating.

2. Set or reset via S terminals

S_1 S_3	S_2 S_4	Q_1 Q_3	Q_2 Q_4
H	L	L	H
L	H	H	L
L	L	H	H
H	H	no change	

The set inputs override the other inputs and directly determine the outputs of the relevant flip-flop.

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.	8.0	V
Output voltage	V_Q	max.	8.0	V
Input voltage	V_J, V_K, V_T, V_S	max.	8.0	V
Output current [1]	$-I_Q$	max.	20	mA
Input current [2]	$-I_J, -I_K, -I_T, -I_S$	max.	20	mA
Voltage difference between any two inputs		max.	8.0	V
Storage temperature	T_{stg}	−55 to	+125	°C
Operating ambient temperature	T_{amb}	0 to	+75	°C

[1]) For negative output voltage in LOW state.
[2]) At this limit input voltage typ. −1.5 V.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to +75		°C
Uniform system supply voltage	V_P	5.7 to 6.3		V
Available d.c. fan out				
to T input	N_{aT}	⩾	1	
to J or K input	$N_{aJ} = N_{aK}$	⩾	10	
to S input	N_{aS2}		2	
	$N_{aS1} = N_{aS3}$		4	
to G input	N_{aG}	⩾	8	
D.C. noise margin				
to T input	M_L	min.	0.3	V
	M_H	min.	1.2	V
to J or K input	M_L	min.	0.7	V
	M_H	min.	1.2	V
to S input	M_L	min.	0.3	V
	M_H	min.	1.9	V
to G input	M_L	min.	0.4	V
	M_H	min.	1.5	V
Average propagation delay time	t_{pd}	max.	105	ns
Maximum clock rate	f_c	⩾	5	MHz
Equivalent input capacitances				
for T input	C_T	typ.	24	pF
for J or K input	$C_J = C_K$	typ.	4	pF
for S input	C_{S2}	typ.	16	pF
	$C_{S1} = C_{S3}$	typ.	8	pF
Supply current (duty cycle 50%) [1]	I_{Pav}	typ.	16.8	mA
Power dissipation at T_{amb} = 75 °C [1]	P_{tot}	max.	150	mW

[1]) Both flip-flops together

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references	
		0	+25	+75		V_P (V)	
STATIC DATA							
Output voltage LOW	V_{QLmax}	0.4	0.4	0.4	V	5.7 and 6.3	
at: Output current LOW	I_{QLmax}	14.0 16.0	16.5 19.0	12.4 14.4	mA mA	5.7 6.3	
Output voltage HIGH	V_{QHmin}	3.8	3.9	4.1	V	5.7	$I_Q = -100\ \mu A$
Output voltage HIGH (lowest permissible)	V_{QHPmin}	3.6	3.3	3.0	V	5.7	
at: Output current HIGH	$-I_{QHmax}$	0.85	3.3	5.5	mA	5.7	
Input current LOW	$-I_{JLmax}$, $-I_{KLmax}$	1.4 1.6	1.3 1.5	1.2 1.4	mA mA	5.7 6.3	$V_J = V_K = 0.4$ V; other inputs floating
	$-I_{TLmax}$	8.0 9.0	7.6 8.4	7.0 7.8	mA mA	5.7 6.3	$V_T = 0.4$ V; other inputs floating
	$-I_{S2Lmax}$	5.7 6.6	5.5 6.3	5.2 5.8	mA mA	5.7 6.3	$V_S = 0.4$ V; other inputs floating
	$-I_{S1Lmax}$, $-I_{S3Lmax}$	2.9 3.3	2.8 3.2	2.6 2.9	mA mA	5.7 6.3	$V_S = 0.4$ V; other inputs floating
Input current HIGH	I_{JHmax}, I_{KHmax}	1	1	25	μA	5.7	$V_J = V_K = 5.3$ V other inputs 0 V
	I_{THmax}	6	6	150	μA	5.7	$V_T = 5.3$ V other inputs 0 V
	I_{S2Hmax}	4	4	100	μA	5.7	$V_S = 5.3$ V other inputs 0 V
	$-I_{S1Hmax}$ $-I_{S3Hmax}$	2	2	50	μA	5.7	$V_S = 5.3$ V other inputs 0 V
Supply current (both flip-flops together)	I_{Pmax}	–	26.7	–	mA	6.3	T input LOW J, K, S inputs HIGH

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references		
		0	+25	+75		V_P (V)		fig.
DYNAMIC DATA						5.7 and 6.3		
Change of state								
Input voltage HIGH during:	V_{THmin} V_{JHmin} V_{KHmin}	2.6	2.3	1.9	V		HIGH level at T and J and/or K to be present simultaneously	1
Input time HIGH to:	t_{THmin}	60	60	60	ns			1
T-input voltage LOW	V_{TLmax}	1.0	1.0	0.7	V		$t_{TLmin} = t_{pdf}$	1
No change of state								
J/K input voltage LOW	V_{JLmax} V_{KLmax}	1.6	1.4	1.1	V		LOW level at J and K to be present prior to T turning HIGH and to remain present during T is HIGH	2
Clock skew protection								
Hold time	$t_{hold\,max}$	10	10	10	ns			2
Reset								
S input voltage LOW	V_{SLmax}	1.0	1.0	0.7	V		active $t_{SLmin} = t_{pdf}$	3
S input voltage HIGH	V_{SHmin}	1.9	1.8	1.6	V		inactive	
DYNAMIC DATA								
Propagation delay times from T to Q								
Rise propagation delay time	$t_{pdr\,max}$	–	90	–	ns	6.0	V_{pd} = 1.5 V N = 1; C_L = 60 pF	4
Fall propagation delay time	$t_{pdf\,max}$	–	120	–	ns	6.0	V_{pd} = 1.5 N = 8; C_L = 60 pF other output: N = 1; C_L = 60 pF	4

CHARACTERISTICS (continued)

DYNAMIC DATA

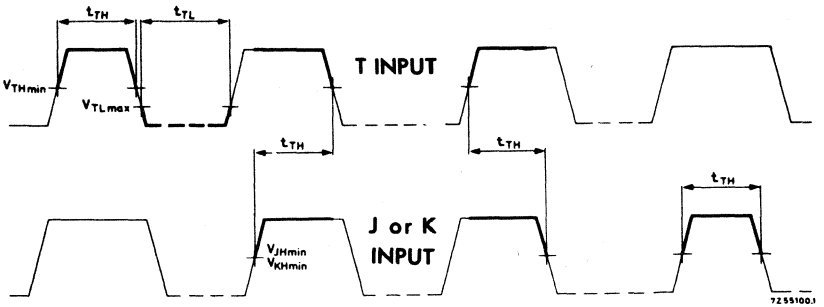


Fig. 1. Waveforms illustrating conditions for change of state.

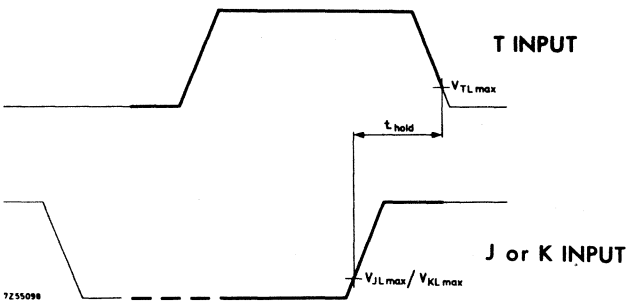


Fig. 2. Waveforms illustrating conditions for no change of state.

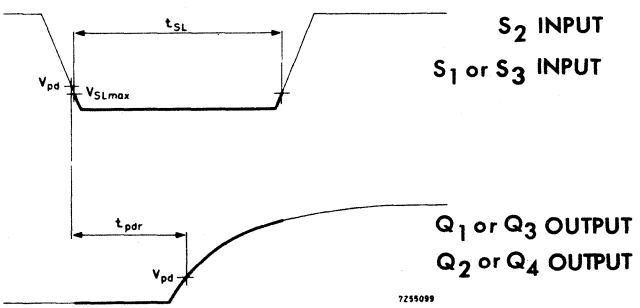
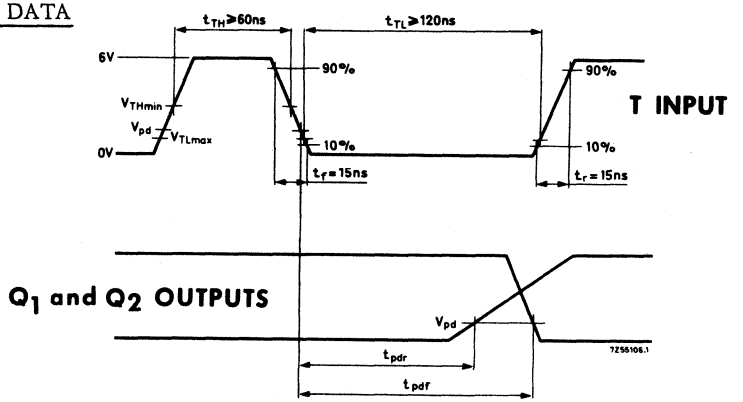
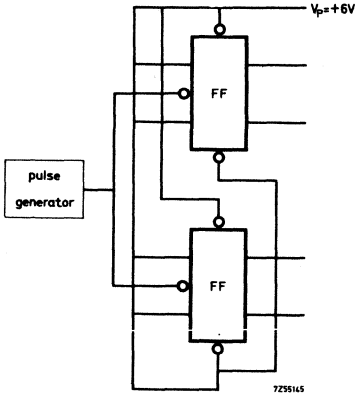


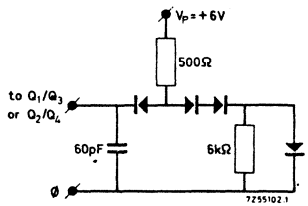
Fig. 3. Waveforms illustrating conditions for set or reset.

CHARACTERISTICS (continued)

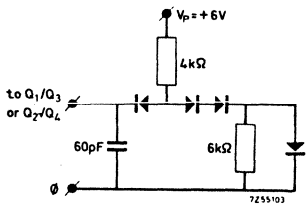
DYNAMIC DATA







Diodes FCY101
Equivalent load for N = 8 and C_L[1]) = 60 pF



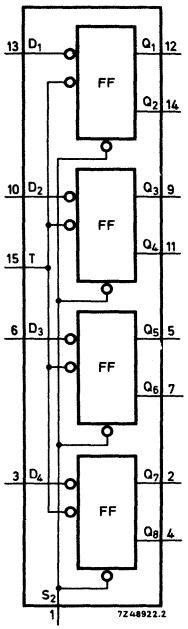
Diodes FCY101
Equivalent load for N = 1 and C_L[1]) = 60 pF

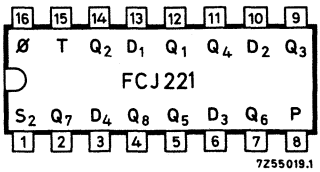
Fig. 4. Waveforms and loading circuits illustrating measurement of t_{pdr} and t_{pdf}

1) Including probe and jig capacitance

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication and industrial control.

QUADRUPLE LATCH FLIP-FLOP



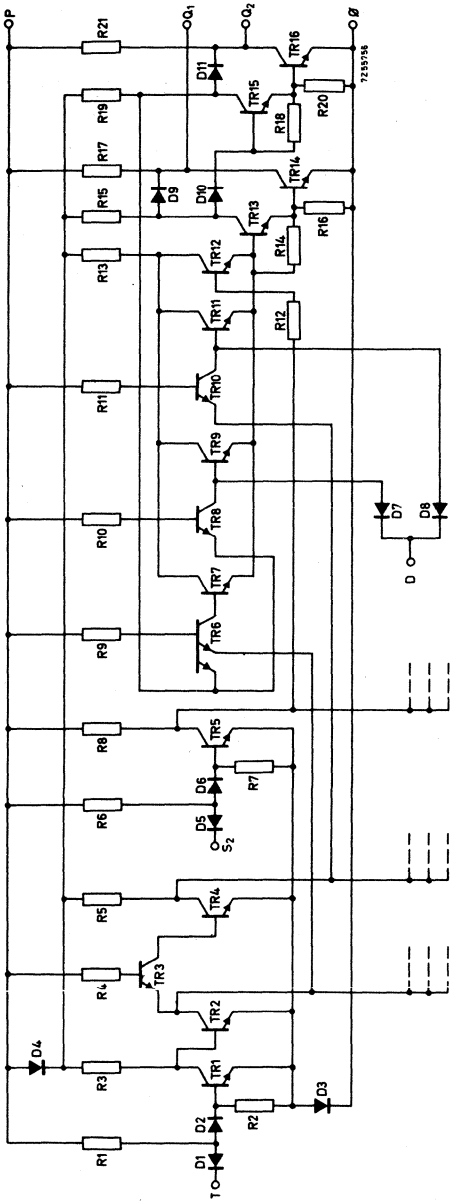


PACKAGE OUTLINE
16 lead plastic dual in-line (type A)
See General Section

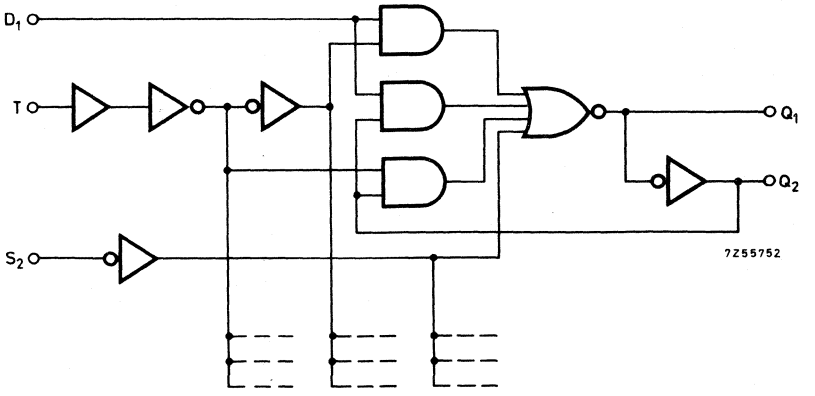
QUICK REFERENCE DATA				
Supply voltage	V_P	6.0	±5%	V
Operating ambient temperature range	T_{amb}	0 to	+75	°C
Clock rate at T_{amb} = 25 °C	f_c	typ.	5	MHz
Available d.c. fan out T_{amb} = 25 °C	N_a	≥	10	
D.C. noise margin T_{amb} = 25 °C	M_L	typ.	1.2	V
Power consumption 50% duty cycle, T_{amb} = 25 °C	P_{av}	typ.	250	mW

The FCJ221 is a quadruple latch flip-flop with D inputs, a common clock (T) and a reset input (S_2).
A LOW input signal at D arrives after the last T signal goes HIGH at output Q_1.
The information follows after a LOW signal at the T input.
It is possible to influence the output state of the flip-flop.

CIRCUIT DIAGRAM



LOGIC DIAGRAM



LOGIC FUNCTION

Function tables

t_n	t_{n+1}
D	Q_1
H	L
L	H

S2	Q_1
H	H
L	X

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
t_n = bit time before trigger pulse
t_{n+1} = bit time after trigger pulse
X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage at $T_{amb} < 40\,^{o}C$	V_P	max.	8	V
Output voltage	V_Q	max.	8	V
Input voltage	V_G	max.	8	V
Input current	$-I_D$; $-I_T$; $-I_{S2}$	max.	20	mA [1])
Storage temperature	T_{stg}	−55 to	+125	°C
Operating ambient temperature	T_{amb}	0	+75	°C

[1]) At negative input voltage

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to +75		°C
Uniform system supply voltage	V_P	5.7 to 6.3		V
Available d.c. fan-out	N_a	≥	10	
D.C. noise margin to D input	M_{DL}	min.	0.2	V
	M_{DH}	min.	3.0	V
to T, S_2 input	M_{TL}; M_{S2L}	min.	0.3	V
	M_{TH}; M_{S2H}	min.	3.1	V
Supply current	I_{Pav}	max.	47	mA[1])
Power dissipation at T_{amb} = 75 °C	P_{tot}	max.	300	mW

1) Input open and V_D = 0 V

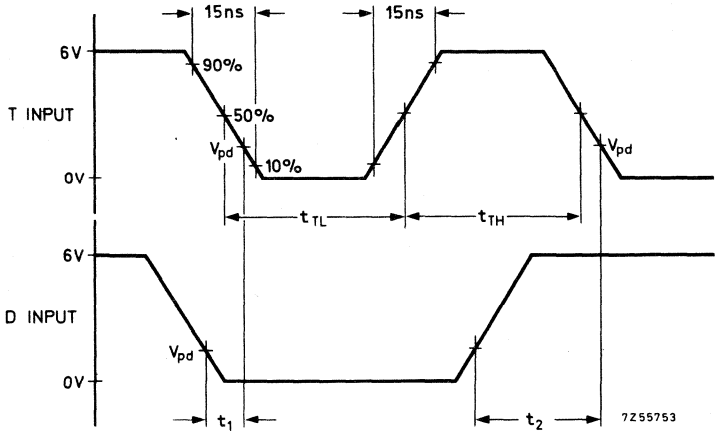
CHARACTERISTICS

STATIC DATA		T_{amb} (°C) 0	25	75		Conditions and references V_P (V)	
Output voltage LOW	V_{QLmax}	0.4	0.4	0.4	V	5.7 and 6.3	
at:							
Output current LOW	I_{QLmax}	17.5	16.5	15.5	mA	5.7	
		20.0	19.0	18.0	mA	6.3	
Output voltage HIGH	V_{QHmin}	5.3	5.3	5.3	V	5.7	$-I_Q = 0$
Input voltage LOW							
D	V_{DLmax}	0.9	0.8	0.6	V	5.7 and 6.3	
T; S_2	V_{TLmax} V_{S2Lmax}	1.0	0.9	0.7	V	5.7 and 6.3	
Input voltage HIGH							
D	V_{DHmin}	2.3	2.2	2.1	V	5.7 and 6.3	
T; S_2	V_{THmin} V_{S2Hmin}	2.2	2.1	2.0	V	5.7 and 6.3	
Input current LOW							
D	$-I_{DLmax}$	2.55	2.5	2.45	mA	5.7	$V_D = 0.4$ V
T; S_2	$-I_{TLmax}$ $-I_{S2Lmax}$	1.75	1.65	1.55	mA	5.7	$V_T = V_{S2} = 0.4$ V
D	$-I_{DLmax}$	2.85	2.8	2.75	mA	6.3	$V_D = 0.4$ V
T; S_2	$-I_{TLmax}$ $-I_{S2Lmax}$	2.0	1.9	1.8	mA	6.3	$V_T = V_{S2} = 0.4$ V
Input current HIGH							
D	I_{DHmax}	2	2	50	µA	6.3	$V_D = V_P$
T; S_2	I_{THmax} I_{S2Hmax}	1	1	25	µA	6.3	$V_T = V_{S2} = V_P$
Output current changing output state							
Q_1	$-I_{Q1max}$	4.2	4.05	3.75	mA	6.3	$V_Q = 0.4$ V
Q_2	$-I_{Q2max}$	6.3	6.1	5.65	mA	6.3	$V_Q = 0.4$ V
Supply current	I_{Pmax}	–	–	47	mA	6.3	$V_D = 0$ V; T and S_2 inputs open

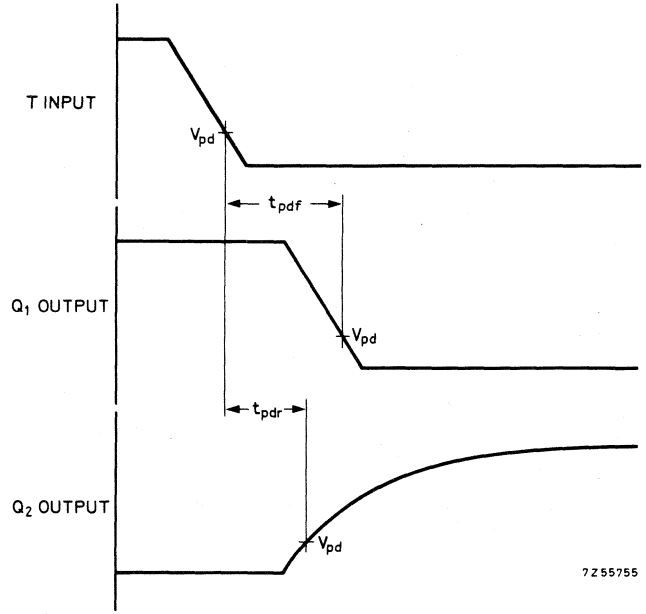
CHARACTERISTICS

		T_{amb} (°C)				Conditions and references	
		0	25	75		V_P (V)	
STATIC DATA							
D.C. noise margin							
LOW: D	M_{DLmin}	0.5	0.4	0.2	V		
T; S_2	M_{TLmin} / M_{S2Lmin}	0.6	0.5	0.3	V		
HIGH: D	M_{DHmin}	3.0	3.1	3.2	V		
T; S_2	M_{THmin} / M_{S2Hmin}	3.1	3.2	3.3	V		
DYNAMIC DATA							
Input time LOW							
T	t_{TLmin}	–	100	–	ns	5.7 and 6.3	
Input time HIGH							
T	t_{THmin}	–	70	–	ns	5.7 and 6.3	
Input time LOW							
S_2	t_{S2Lmin}	–	100	–	ns	5.7 and 6.3	
S_2 (changing output state)	t_{S2Lmin}	–	100	–	ns	5.7 and 6.3	
Set-up times:							
t_1	t_{su1min}	–	0	–	ns	5.7 and 6.3	
t_2	t_{su2min}	–	30	–	ns		
Propagation delay times:							
Rise propagation delay times							
$T \rightarrow Q_1$	t_{pdrmax}	–	95	–	ns	6.0	N = 1; C_L = 40 pF; V_{pd} = 1.5 V
$\overline{T} \rightarrow Q_2$	t_{pdrmax}	–	105	–	ns	6.0	
$S_2 \rightarrow Q_2$	t_{pdrmax}	–	85	–	ns	6.0	
Fall propagation delay times							
$T \rightarrow Q_1$	t_{pdfmax}	–	60	–	ns	6.0	N = 8; C_L = 70 pF; V_{pd} = 1.5 V
$\overline{T} \rightarrow Q_2$	t_{pdfmax}	–	120	–	ns	6.0	
$S_2 \rightarrow Q_2$	t_{pdfmax}	–	60	–	ns	6.0	

CHARACTERISTICS (continued)

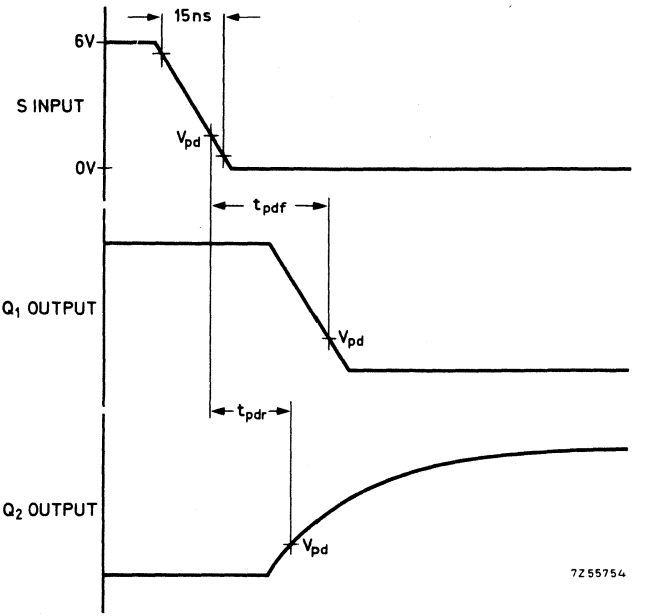


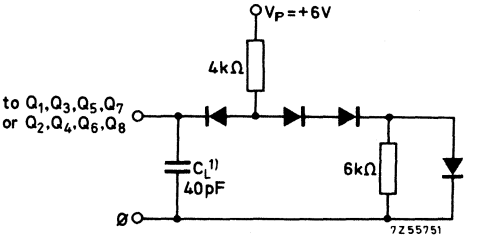
Waveform illustrating conditions for change of state



Waveforms illustrating t_{pdr} and t_{pdf}

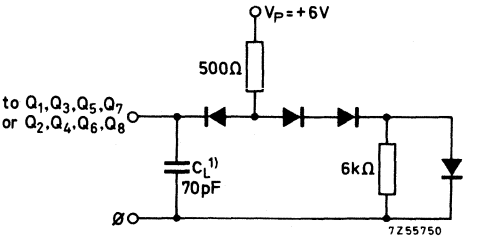
CHARACTERISTICS (continued)





diodes FCY101

N = 1



diodes FCY101

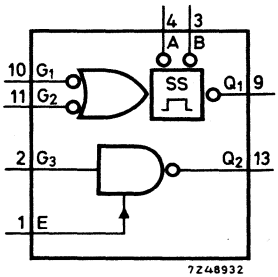
N = 8

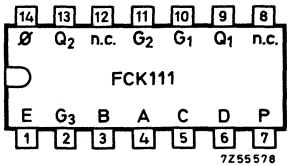
Waveforms and loading circuits illustrating measurement of t_{pdr} and t_{pdf}.

1) Including jig and probe capacitance.

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication and industrial control.

MONOSTABLE MULTIVIBRATOR





QUICK REFERENCE DATA				
Supply voltage	V_P		6.0 ± 5%	V
Operating ambient temperature	T_{amb}		0 to +75	°C
Propagation delay time $G_1 \rightarrow Q_1$	t_{pdf}	typ.	70	ns
T_{amb} = 25 °C at V_{pd} = 1.5 V $G_3 \rightarrow Q_2$	t_{pdf}	typ.	40	ns
Output pulse width:				
R_t = 10 kΩ ± 1%; C_t = 160pF ± 1%	t_{Q1L}	typ.	1.0	µs
Available d.c. fan-out Q_1	N_a	≥	14	
T_{amb} = 0 to +75 °C Q_2	N_a	≥	14	
A	N_a	=	1	
D.C. noise margin				
T_{amb} = 25 °C	M_L	typ.	1.2	V
Power consumption				
50% duty cycle, T_{amb} = 25 °C	P_{av}	typ.	58	mW

PACKAGE OUTLINE: 14 lead plastic dual in-line (type A) (See General Section)

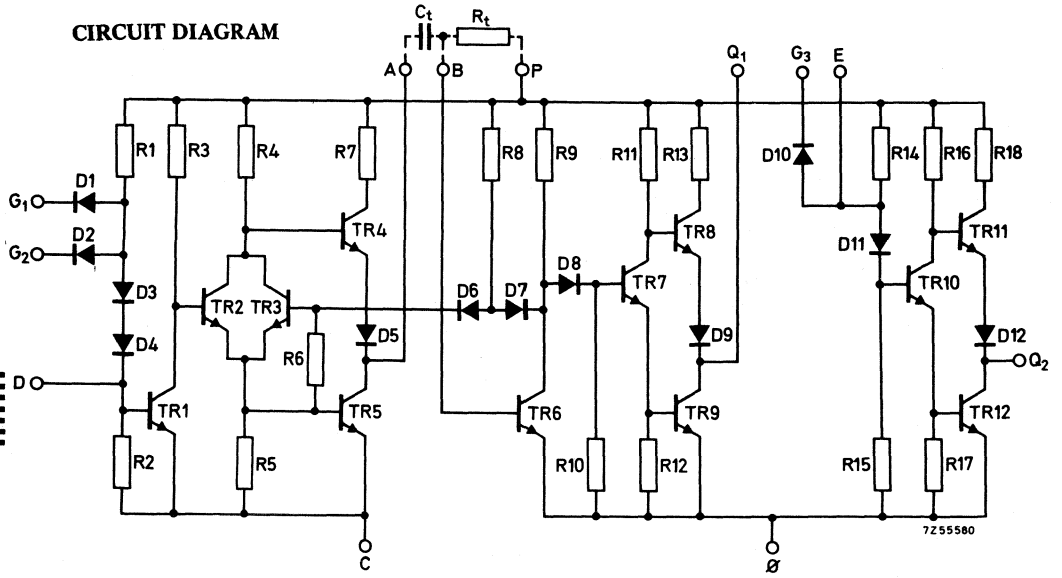
The FCK111 comprises a threshold triggered monostable circuit and an independent expandable inverter.

The monostable function is obtained by an externally connected resistor and capacitor. Each time one of the inputs G_1 or G_2 is going LOW a negative going pulse appears at output Q_1.

The pulse width is adjustable over a very wide range by varying the resistor and capacitor values.

If the input (G_3) of the inverter is connected to A a positive going pulse is obtained at the output Q_2, almost coinciding and practically having the same width as the output pulse Q1, provided that the width of the input pulse does not exceed the width of the output pulse. The outputs Q_1 and Q_2 are bi-directional and have a high fan-out drive capability.

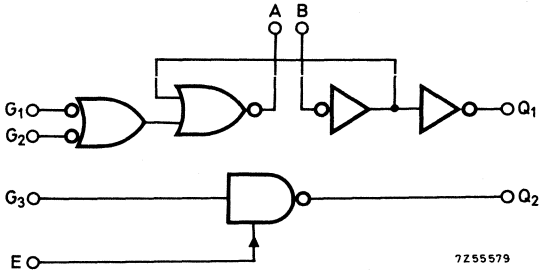
CIRCUIT DIAGRAM



Notes

1. Terminals C and D make the circuit compatible with the FCK101.
2. To ensure conformity with the characteristics given in the data sheets, terminal C must be connected to terminal ϕ.
   If terminals C and ϕ are not interconnected, the output pulse can be shortened by connecting a diode or a voltage source to C (positive to ϕ); however, this will alter a number of characteristics, including special input levels and output level A.
3. The noise margin for a.c. disturbances at the trigger inputs G_1 and G_2 can be increased by connecting a capacitor between terminals C and D, but this reduces the minimum operating frequency.

LOGIC DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	8.0	V
Output voltage	V_Q	max.	8.0	V
Input voltage	V_G	max.	8.0	V
Output current	$-I_Q$	max.	20.0	mA [1]
Input current	$-I_G$	max.	20.0	mA [2]
Voltage difference between any two inputs		max.	8.0	V
Expander input voltages:				
– with respect to supply	V_P-V_E	max.	8.0	V
– with respect to other inputs	V_G-V_E	max.	8.0	V
Expander input current	I_E	max.	5.0	mA
Storage temperature	T_{stg}		−55 to +125	°C
Operating ambient temperature	T_{amb}		0 to +75	°C
Output short circuit duration (duty cycle 10%, either output, or both)	t_{Qsc}	max.	60	ms
Timing resistor (R_t connected to 6.3 V)	R_t	min.	5	kΩ
		max.	20	kΩ
Timing capacitor	C_t	max.	160	µF
		min.	30	pF [3]

[1]) for negative output voltage in LOW state.

[2]) at this limit, input voltage typ: − 1.5 V.

[3]) C_t min 30 pF is not a rating, but is to be considered as the minimum value at which the circuit still performs its function.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}		0 to +75	°C
Uniform system supply voltage	V_P		5.7 to 6.5	V
Available d.c. fan-out Q_1	N_a	≥	14	
Available d.c. fan-out Q_2	N_a	≥	14	
Available d.c. fan-out A	N_a	=	1	
D.C. noise margin FCK111 → gate	M_L	min.	0.4	V
	M_H	min.	1.2	V
gate → FCK111	M_L	min.	0.4	V
	M_H	min.	1.8	V
Propagation delay time: $G_1 \rightarrow Q_1$	t_{pdf}	max.	170	ns
$G_1 \rightarrow Q_2$	t_{pdr}	max.	200	ns
$G_3 \rightarrow Q_2$	t_{pdr}	max.	120	ns
$G_3 \rightarrow Q_2$	t_{pdf}	max.	55	ns
Equivalent input capacitance	C_G	typ.	4	pF
Supply current (duty cycle 50%)	I_{Pav}	typ.	10.9	mA
Power dissipation at T_{amb} = 75 °C	P_{tot}	max.	98	mW
Relative change of output pulse width vs supply voltage	see page 10			
Output pulse width vs timing capacitor (C_t)	see page 10			

CHARACTERISTICS : (pin C connected to pin ϕ)

STATIC DATA		T_{amb} (°C) 0	25	75	Conditions and References V_P (V)	
Output Q_1						
Output voltage LOW at:	V_{Q1L} max	0.4	0.4	0.4 V	5.7 and 6.3	V_B (pin 3) at 0 V
Output current LOW	I_{Q1L} max	25	27	26 mA	5.7	
		28	27	26 mA	6.3	
Output voltage HIGH	V_{Q1H}min	3.5	3.7	4.0 V	5.7	$-I_{Q1H}$ = 30 µA } and
		2.6	2.8	2.9 V	5.7	$-I_{Q1H}$ = 5 mA } B (pin 3) connected to V_P via 20 kΩ (± 1 %)
Output short circuit current	$-I_{Q1sc}$ min	16.5	19.5	18.0 mA	5.7	B (pin 3) connected to V_P via 20 kΩ (± 1 %) (max. duration 60 ms; duty cycle 10 %)
Output Q_2						
Output voltage LOW at:	V_{Q2L} max	0.4	0.4	0.4 V	5.7 and 6.3	
Output current LOW	I_{Q2L} max	25	27	26 mA	5.7	
		28	27	26 mA	6.3	
and Input voltage HIGH G_3	V_{GH} min	2.3	2.2	2.1 V	5.7 and 6.3	
Output voltage HIGH at:	V_{Q2H} min	3.5	3.7	4.0 V	5.7	$-I_{Q2H}$ = 30 µA
		2.6	2.8	2.9 V	5.7	$-I_{Q2H}$ = 5 mA
Input voltage LOW G_3	V_{GL} max	1.0	1.0	0.8 V	5.7 and 6.3	
Output short circuit current	$-I_{Q2sc}$ min	16.5	19.5	18.0 mA	5.7	V_{GL} max (max. duration 60 ms; duty cycle 10 %)

CHARACTERISTICS (continued)

STATIC DATA (continued)		T_{amb} (°C) 0	25	75	Conditions and references V_P (V)	
Output A						
Output voltage LOW	V_{AL} max	0.4	0.4	0.4 V	5.7 and 6.3	
at:						
Output current LOW	I_{AL} max	2.0	2.0	2.0 mA	5.7 and 6.3	see note
and						
Input voltage LOW; G_1, G_2 or V_B (pin 3) at 0 V	V_{GL} max	1.0	1.0	0.8 V	5.7 and 6.3	
Output voltage HIGH	V_{AH} min	3.9	4.0	4.1 V	5.7	$-I_{AH}$ = 30 μA
		3.2	3.4	3.4 V	5.7	$-I_{AH}$ = 5 mA
at:						
Input voltage HIGH	V_{GH} min	2.3	2.2	2.1 V	5.7 and 6.3	
or: B (pin 3) connected to V_P via 20 kΩ (± 1%)						
Output short circuit current	$-I_{Asc}$ min	30	30	25 mA	5.7	B (pin 3) connected to V_P via 20 kΩ (± 1%) (max. duration 60 ms; duty cycle 10%)

Note

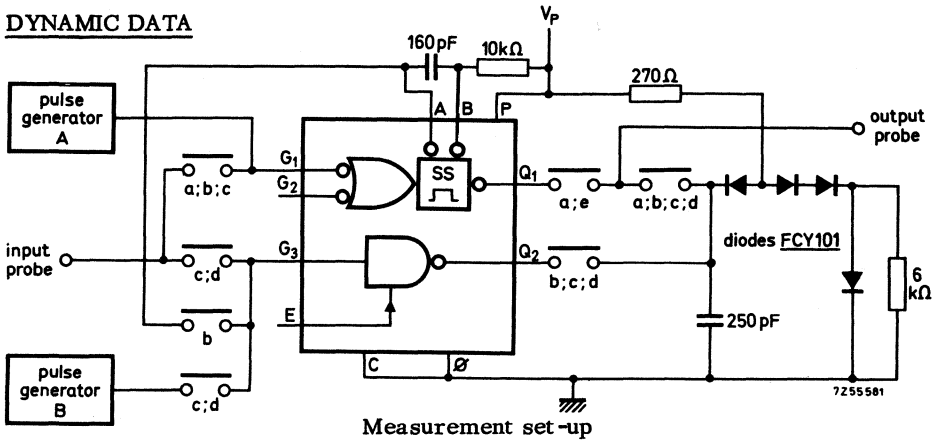
I_{AL} max is an extra static current, which can be applied to output A under both static and dynamic conditions without dusturbing the output pulse width.

CHARACTERISTICS (continued)

STATIC DATA (continued)		T_{amb} (°C) 0	25	75		V_P (V)	Conditions and references
Input current LOW	$-I_{GL}$ max	1.75	1.65	1.85	mA	5.7	V_G = 0.4 V other inputs
		2.00	1.90	1.80	mA	6.3	V_G = 0.4 V floating
Input current HIGH	I_{GH} max	1.0	1.0	25.0	µA	5.7	V_G = 5.3 V, other inputs at V_G = 0 V
Supply current (unloaded)							current flow in R_t not included
output Q_1 HIGH, output Q_2 LOW	I_{PH} typ	8.3	8.0	7.5	mA	6.0	
output Q_1 LOW, output Q_2 LOW	I_{PL} typ	13.5	11.3	10.3	mA	6.0	
	I_{PL} max	17.3	16.6	15.6	mA	6.3	
Average supply current	I_{Pav}	14.7	14.1	13.2	mA	6.3	duty cycle 50%
DYNAMIC DATA							
Propagation delay times							
Rise : $G_1 \rightarrow Q_2$	t_{pdr} max	170	150	200	ns	6.0	V_{pd} = 1.5 V; N = 15; C_L = 250 pF; $t_f = t_r$ = 15 ns
$G_3 \rightarrow Q_2$	t_{pdr} max	80	85	120	ns	6.0	
Fall : $G_1 \rightarrow Q_1$	t_{pdf} max	170	130	170	ns	6.0	
$G_3 \rightarrow Q_2$	t_{pdf} max	55	50	55	ns	6.0	
Pulse width	t_{Q1Lmax}		1.10		µs	6.0	R_t = 10 kΩ ± 1 %; C_t = 160 pF ± 1 %
	t_{Q1Ltyp}		1.00		µs	6.0	
	t_{Q1Lmin}		0.90		µs	6.0	
Duration input LOW	t_{GL} min	30	30	40	ns	5.7 and 6.3	

CHARACTERISTICS (continued)

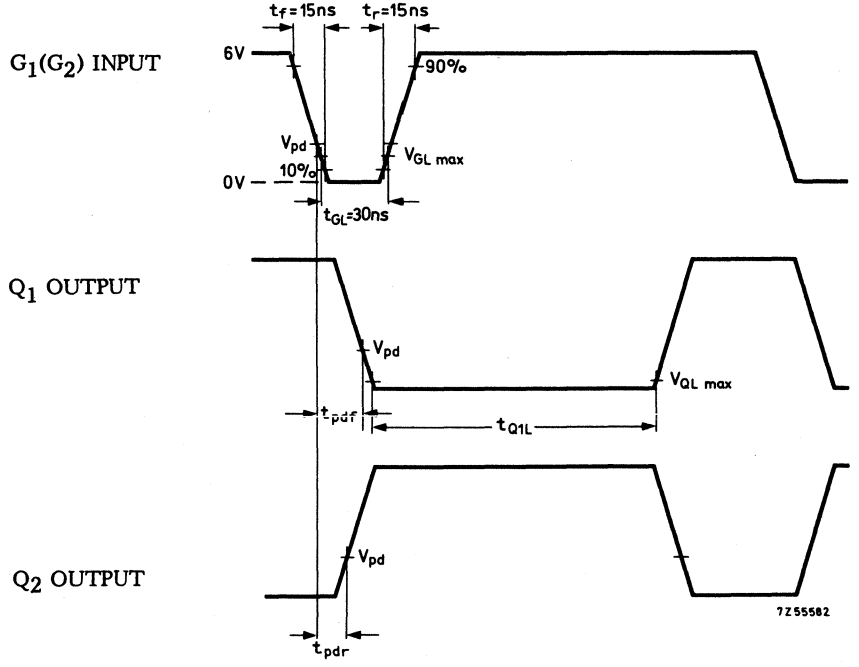
DYNAMIC DATA



Measurement set-up

a = t_{pdf} : $G_1 \rightarrow Q_1$ c = t_{pdf} : $G_3 \rightarrow Q_2$ e = t_{Q1L}

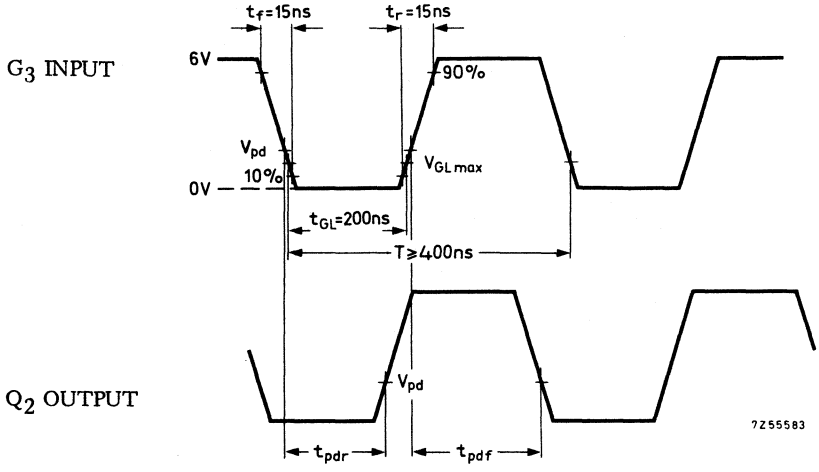
b = t_{pdr} ; $G_1 \rightarrow Q_2$ d = t_{pdr} ; $G_3 \rightarrow Q_2$



Waveform illustrating measurement of t_{pdr}, t_{pdf}, t_{GL} and t_{Q1L} for A pulse generator.

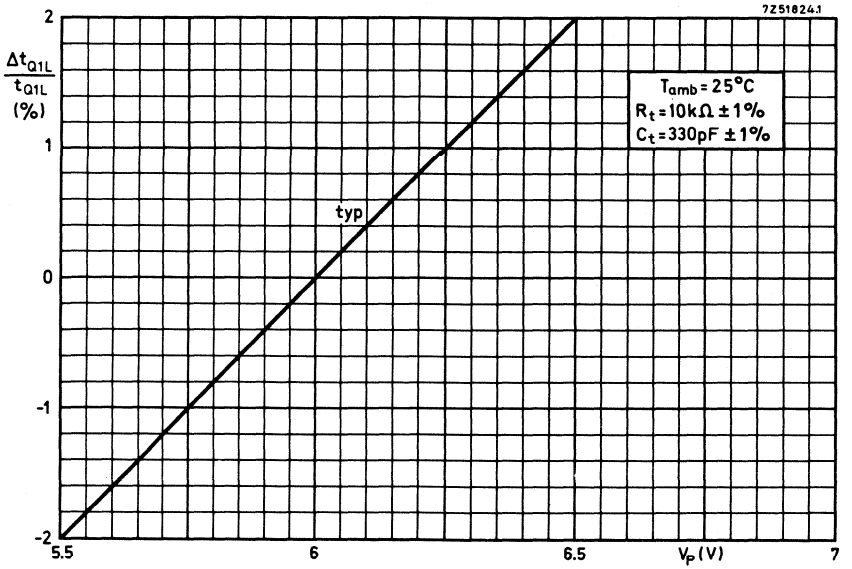
CHARACTERISTICS (continued)

DYNAMIC DATA

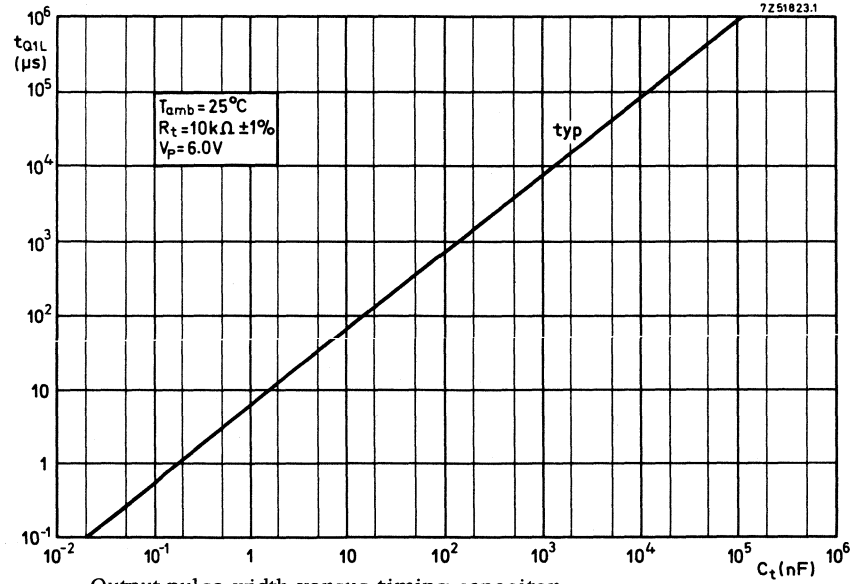


Waveforms illustrating measurement of t_{pdr}, t_{pdf} and t_{GL} for B pulse generator.

CHARACTERISTICS (continued)



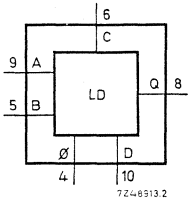
Relative change of output pulse width versus supply voltage.

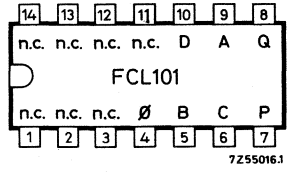


Output pulse width versus timing capacitor.

The FC family of DTL silicon monolithic integrated circuit has been designed for medium speed digital applications in computing, office electronics, telecommunication and industrial control.

LEVEL DETECTOR



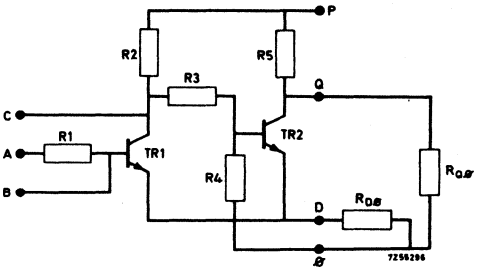


QUICK REFERENCE DATA			
Supply voltage	V_P	6.0 ± 5%	V
Operating ambient temperature range	T_{amb}	0 to +75	°C
Input hysteresis voltage $R_{D\emptyset}$ = 100 Ω, T_{amb} = 25 °C	ΔV_{At}	min. 60 max. 200	mV mV
Available output current $R_{D\emptyset}$ = 100 Ω, T_{amb} = 25 °C	I_{QL}	2.7	mA
Operating frequency T_{amb} = 25 °C	f	typ. 5	MHz
Power consumption 50% duty cycle, T_{amb} = 25 °C	P_{av}	typ. 12	mW

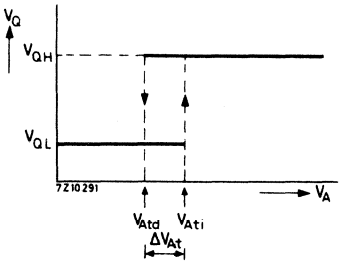
The FCL101 is a non-inverting Schmitt-trigger circuit. Tripping levels are set by an external resistor or zener diode.
Typical applications are discrimination, restoration, level shifting and pulse-shaping (squaring).

PACKAGE OUTLINE 14 lead dual in-line (See General Section)

CIRCUIT DIAGRAM



VOLTAGE TRANSFER CURVE



Letter symbols:

$R_{Q\emptyset}$ = external resistor between Q and Ø

$R_{D\emptyset}$ = external resistor between D and Ø

V_Q = short for $V_{Q\emptyset}$ = voltage at Q with respect to Ø, the common reference and supply return terminal

V_{Ati} = tripping level for increasing input voltage V_A (short for $V_{A\emptyset}$)

V_{Atd} = tripping level for decreasing input voltage V_A

$\Delta V_{At} = V_{Ati} - V_{Atd}$ = input hysteresis voltage.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	8.0	V
Output voltage	V_Q	max.	8.0	V
Input voltage	V_A	max.	8.0	V
with respect to supply voltage	$V_A - V_P$	max.	2.0	V
Output current [1]	$-I_Q$	max.	20	mA
Input current [2]	$-I_A$	max.	0.5	mA
Other terminals	I_B	max.	5	mA
	V_C	max.	5.0	V
	V_D	max.	5.0	V
Storage temperature	T_{stg}	−55 to	+125	°C
Operating ambient temperature	T_{amb}	0 to	+75	°C

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to	+75	°C
Uniform system supply voltage	V_P	5.7 to	6.3	V
Output resistance	P_o	max.	7.6	kΩ
Supply current at T_{amb} = 25 °C, V_P = 6 V duty cycle 50%	I_{Pav}	typ.	2.0	mA
Power dissipation at T_{amb} = 75 °C	P_{tot}	max.	27	mW

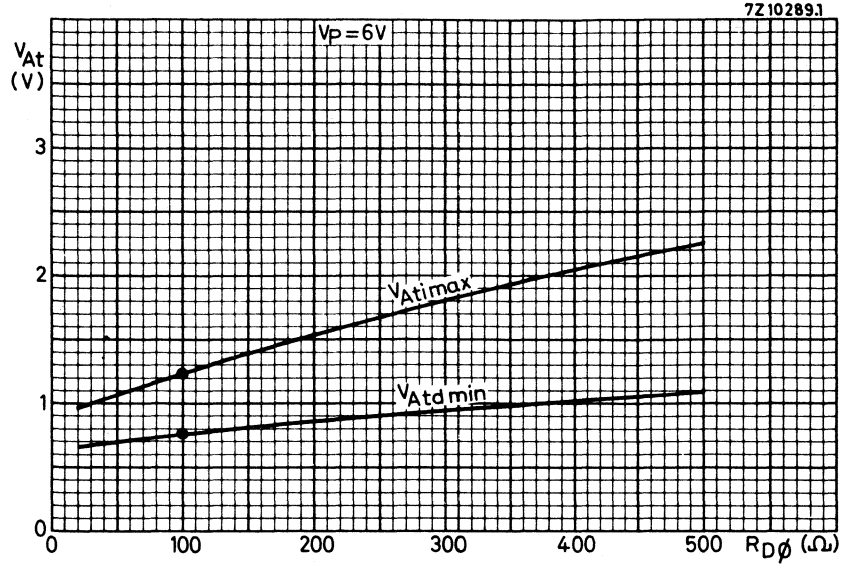
[1]) For negative output voltage.

[2]) Input voltage typ. −9 V when D grounded; no input current protection required for input voltages down to −5 V.

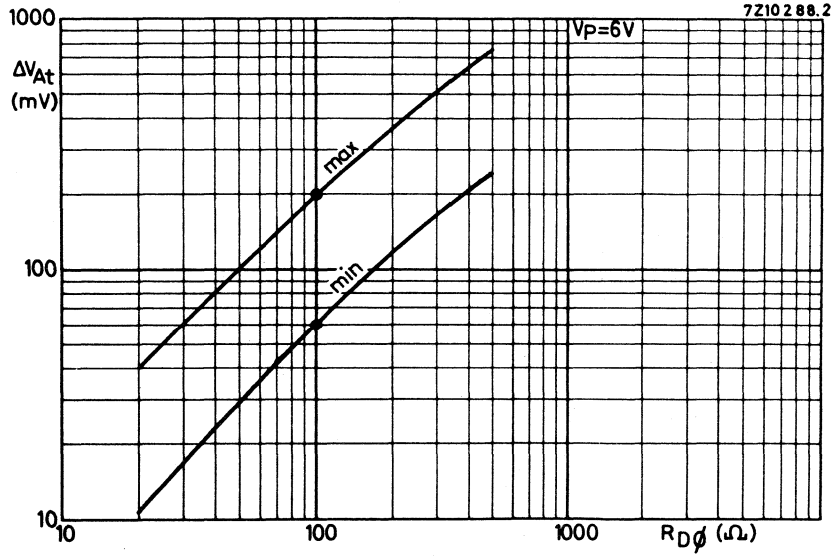
CHARACTERISTICS

		T_{amb} (°C)				Conditions and references		
		0	+25	+75		$V_{P(V)}$	$R_{D\emptyset(\Omega)}$	
STATIC DATA								
Tripping levels								
- input voltage increasing	V_{Atimax}	1.40	1.25	1.15	V	6.0	100 ± 1%	
- input voltage decreasing	V_{Atdmin}	0.75	0.75	0.60	V	6.0	100 ± 1%	
Input hysteresis voltage	ΔV_{Atmin}	60	60	50	mV	6.0	100 ± 1%	
	ΔV_{Atmax}	220	200	180	mV	6.0	100 ± 1%	
Output voltage LOW	V_{QLmax}	0.4	0.4	0.4	V	5.7 and 6.3	0	
at:								
Output current LOW	I_{QLmax}	10	10	7	mA			
and at:								
Input voltage LOW	V_{ALmax}	0.60	0.60	0.45	V			
Output voltage LOW	V_{QLmax}	0.8	0.8	0.8	V	5.7 and 6.3	100 ± 1%	$V_{ALmax} = V_{Atd\,min}$
at:								
Output current LOW	I_{QLmax}	2.5	2.9	1.9	mA	5.7		
		2.1	2.5	1.6	mA	6.3		
Output voltage HIGH	V_{QHmin}	5.3	5.3	5.3	V	5.7	0	$I_Q = 0$
at:								
Input voltage HIGH	V_{AHmin}	0.95	0.90	0.80	V			
Input current HIGH	I_{AHmax}	2.2	2.0	2.0	mA	5.7 and 6.3	0	$V_A = 2\,V$
Input current HIGH	I_{AHmax}	1.2	1.1	1.2	mA	5.7 and 6.3	100 ± 1%	$V_A = 2\,V$
Output current LOW	$-I_{QLLmin}$	1.0	0.95	0.75	mA	5.7	0	$V_A = 2\,V$, V_Q externally forced to 0 V.
	$-I_{QLLmax}$	2.5	2.1	2.0	mA	6.3	0	
Supply current								
- output LOW	I_{PLmax}	4.2	3.7	3.5	mA	6.3	0	$V_A = 0\,V$
- output HIGH	I_{PHmax}	2.9	2.6	2.5	mA	6.3	0	$V_A = 2\,V$
DYNAMIC DATA								
Operating frequency	f_{min}	–	1	–	MHz	6.0	100 ± 1%	
	f_{typ}	–	5	–	MHz			

DESIGN CURVES at T_{amb} = 25 °C (dots indicate guaranteed values)

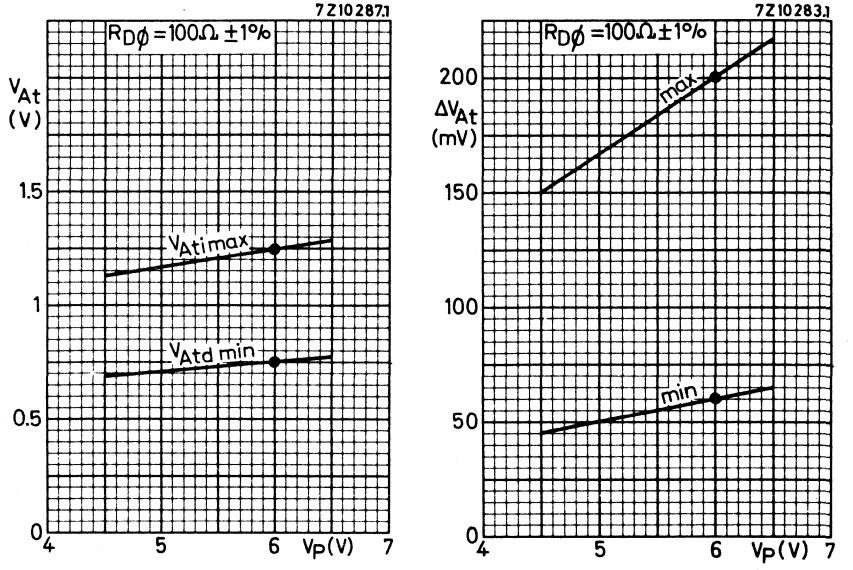


Input tripping levels versus feedback resistance

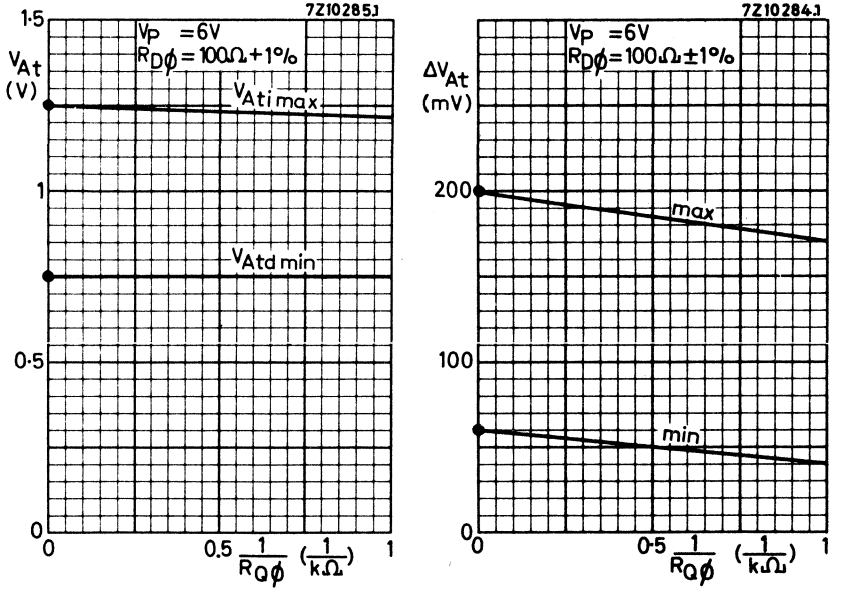


Input hysteresis voltage versus feedback resistance

DESIGN CURVES (continued) at T_{amb} = 25 °C

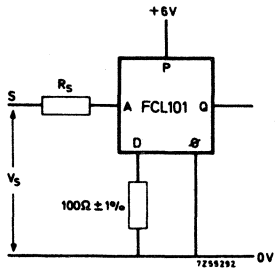


Input tripping levels and hysteresis voltage versus supply voltage

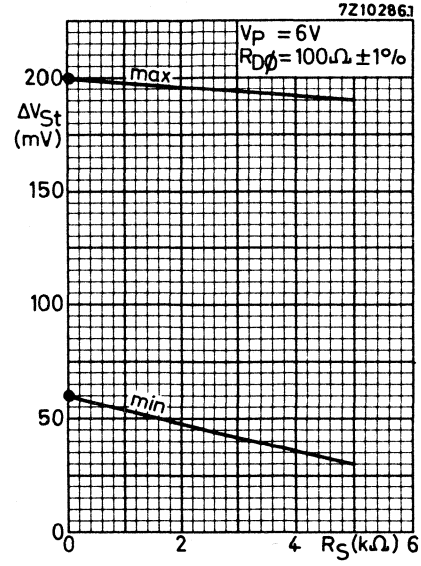


Input tripping levels and hysteresis voltage versus load conductance

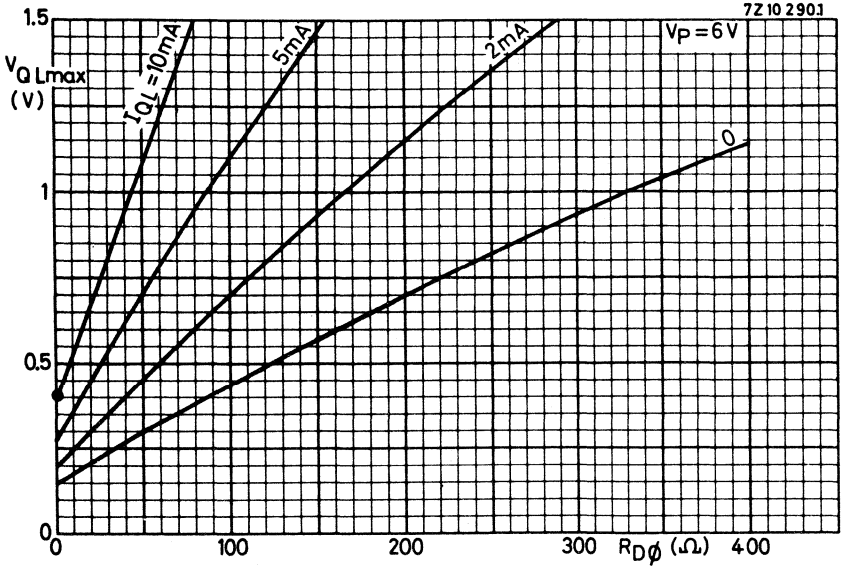
DESIGN CURVES (continued) at T_{amb} = 25 °C



ΔV_{St} = hysteresis at point S.



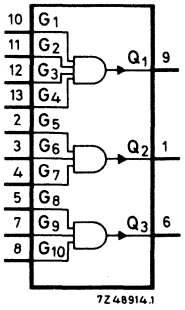
Hysteresis at signal source versus resistance

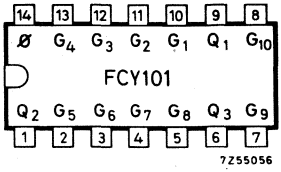


Low output voltage versus feedback resistance

The FC family of DTL silicon monolithic integrated circuits has been designed for medium speed digital applications in computing, office electronics, telecommunication, instrumentation and industrial control.

TRIPLE GATE EXPANDER





CHARACTERISTICS

			T_{amb} (°C) 25	75	
Reverse breakdown voltage at I_R = 50 μA	$V_{(BR)R}$	min.	8.0		V
Reverse leakage current at V_R = 8.0 V	I_R	max.	1.0	25	μA
Forward voltage at I_F = 2.0 mA	V_F	max.	1.0		V
Capacitance at V_R = 0; f = 1 MHz	C_d	max.	11		pF
Reverse recovery time at $I_F = I_R$ = 2.0 mA	t_{rr}	typ.	4		ns
		max.	11		ns

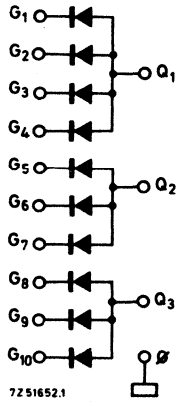
The FCY101 comprises three independent diode arrays. It is intended primarily for expanding the fan-in capability of those FCH gates that have an expansion input terminal.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Reverse voltage	V_R	max.	8.0	V
Forward current	I_F	max.	30	mA
Storage temperature	T_{stg}	−55 to +125		°C
Operating ambient temperature	T_{amb}	0 to +75		°C

PACKAGE OUTLINE: 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAM



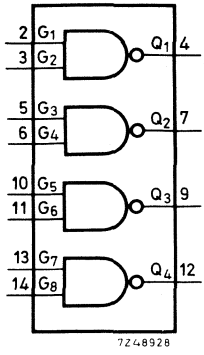
DTL/HNIL

FZ family

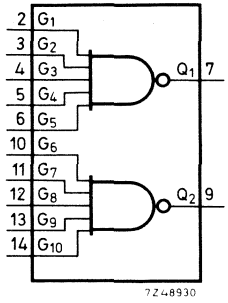
FZH101	quadruple 2-input NAND gate
FZH111	quadruple 2-input NAND gate (with slow-down capability)
FZH121	dual 5-input NAND gate
FZH131	dual 5-input NAND gate (with slow-down capability)
FZH141	dual 5-input power NAND gate (with slow-down capability)
FZH151	AND-OR gate (with slow-down capability)
FZH161	level CONVERTER HNIL to TTL (with slow-down capability)
FZH171	dual 4-input NAND gate (with slow-down capability and expandable inputs
FZH181	level CONVERTER TTL to HNIL
FZJ101	single JK master-slave FLIP-FLOP (with slow-down capability on the slave)
FZJ111	single JK master-slave FLIP-FLOP (with slow-down capability on master and slave)

The FZ family of HNIL silicon monolithic integrated circuits has been designed for high noise immunity low speed digital applications in industrial control and computer periphery equipment.

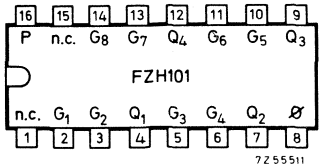
FZH101: QUADRUPLE 2-INPUT NAND GATE
FZH121: DUAL 5-INPUT NAND GATE

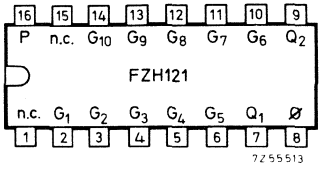


FZH101



FZH121





QUICK REFERENCE DATA

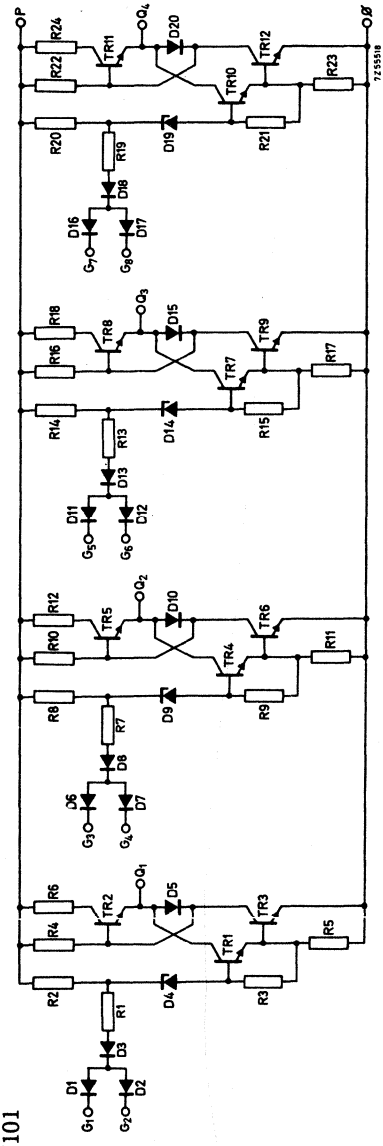
Supply voltage (range I)	V_P	12 $^{+12\frac{1}{2}\%}_{-5\%}$	V
(range II)	V_P	15 $^{+13\%}_{-10\%}$	V
Operating ambient temperature	T_{amb}	0 to +70	°C
Average propagation delay time ($N = 1$; $C_L = 10$ pF; $T_{amb} = 25$ °C; $V_{pd} = 4.5$ V	tpd	typ. 170	ns
Available d.c. fan-out (LOW state)	N_{aL}	max. 10	
($T_{amb} = 0$ to +70 °C) HIGH state	N_{aH}	max. 100	
D.C. noise margin at $T_{amb} = 25$ °C			
range I : $V_P = 12$ V	$M_L = M_H$	typ. 5	V
range II: $V_P = 15$ V	M_L	typ. 5	V
	M_H	typ. 8	V
Power consumption per gate at $T_{amb} = 25$ °C			
(50% duty cycle) range I : $V_P = 12$ V	P_{av}	typ. 16	mW
range II : $V_P = 15$ V	P_{av}	typ. 27	mW

The FZH101 and FZH121 consists of a number of independent NAND gates without slow-down capability.

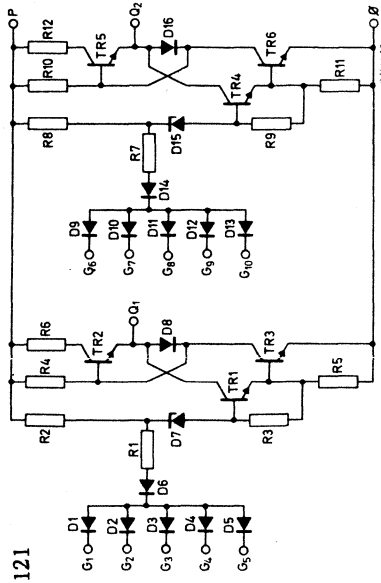
PACKAGE OUTLINE 16 lead plastic dual in-line (type B) (See General Section).

CIRCUIT DIAGRAMS

FZH101



FZH121

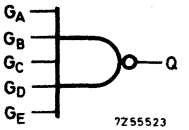


LOGIC FUNCTION

FZH101

$Q = \overline{G_A \cdot G_B}$ (positive logic)

FZH121



$Q = \overline{G_A \cdot G_B \cdot G_C \cdot G_D \cdot G_E}$

(positive logic)

Function tables

G_A	G_B	Q
L	X	H
X	L	H
H	H	L

G_A	G_B	G_C	G_D	G_E	Q
L	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H
H	H	H	H	H	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18	V
Output voltage	V_Q	max.	12	V
Input voltage	V_G	max.	18	V
Input current at V_P = 17 V; $-V_{Gtyp}$ = 5 V	$-I_{GL}$	max.	25	mA
Voltage difference between any two inputs		max	18	V
Storage temperature	T_{stg}	−65 to +150		°C
Operating ambient temperature	T_{amb}	0 to +70		°C
Output short circuit duration duty cycle 10 %	t_{Qsc}	max.	2	s

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to	+70	°C
Uniform system supply voltage (range I)	V_P	11.4 to	13.5	V
(range II)	V_P	13.5 to	17	V
Available d.c. fan-out	N_{aL}	max.	10	
	N_{aH}	max.	100	
D.C. noise margin; range I at V_{Pmin}	M_L	min.	2.8	V
	M_H	min.	2.5	V
range II at V_{Pmin}	M_L	min.	2.8	V
	M_H	min.	4.5	V
Supply current at range I ; output HIGH	I_{Pav}	typ.	0.9	mA
output LOW	I_{Pav}	typ.	1.7	mA
at range II; output HIGH	I_{Pav}	typ.	1.2	mA
output LOW	I_{Pav}	typ.	2.3	mA
Power consumption per gate (50% duty cycle) at range I ; V_{Pmax}	P_{tot}	max.	28	mW
at range II; V_{Pmax}	P_{tot}	max.	46	mW
Thermal resistance from system to ambient	R_{th}	max.	150	°C/W

CHARACTERISTICS Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Sym-bol	min.	typ. [1]	max.	Conditions and references: V_P (V)	Conditions and references
STATIC DATA						
Voltages						
Input HIGH	V_{GH}	7.5	–	– V	11.4	$V_{QL} \leq 1.7$ V; I_{QL} = 15 mA
Input LOW	V_{GL}	–	–	4.5 V	11.4 and 13.5	$V_{QH} \geq 10$ V; $-I_{QH}$ = 15 mA
Output HIGH	V_{QH}	10.0	11.3	– V	11.4 and 13.5	V_{GL} = 4.5 V; $-I_{QH}$ = 0.1 mA
Output LOW	V_{QL}	–	0.9	1.7 V	11.4	V_{GH} = 7.5 V; I_{QL} = 15 mA
D.C. noise margin: HIGH	M_H	2.5	5.0	– V	11.4	
LOW	M_L	2.8	5.0	– V	11.4	
Currents (per gate)						
Input HIGH	I_{GH}	–	–	1.0 µA	13.5	V_{GH} = 13.5 V; other inputs 0 V
Input LOW	$-I_{GL}$	–	0.8	1.5 mA	13.5	V_{GL} = 1.7 V; other inputs 13.5 V
Output HIGH	$-I_{QH}$	0.1	–	– mA	11.4 and 13.5	V_{GL} = 4.5 V; V_{QH} = 10 V
Output LOW	I_{QL}	15	–	– mA	11.4	V_{GH} = 7.5 V; V_{QL} = 1.7 V
Output short circuited [2]	$-I_{Qsc}$	10	30	50 mA	13.5	V_G = 0 V; V_Q = 0 V
SUPPLY DATA						
Currents (per gate)						
at V_{QH}	I_P	–	0.9	1.6 mA	13.5	V_G = 0 V
at V_{QL}	I_P	–	1.7	3.0 mA	13.5	V_G = 13.5 V
DYNAMIC DATA						
Times						
Propagation delay:						
fall time	t_{pdf}	90	175	310 ns	12	C_L = 10 pF; N = 1; T_{amb} = 25 °C; V_{pd} = 4.5 V
rise time	t_{pdr}	90	175	310 ns	12	
output rise time	t_r	200	340	570 ns	12	
output fall time	t_f	70	120	210 ns	12	

[1] All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V

[2] Non-repetitive short circuit duration max. 2 s (duty cycle 10%)

CHARACTERISTICS Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

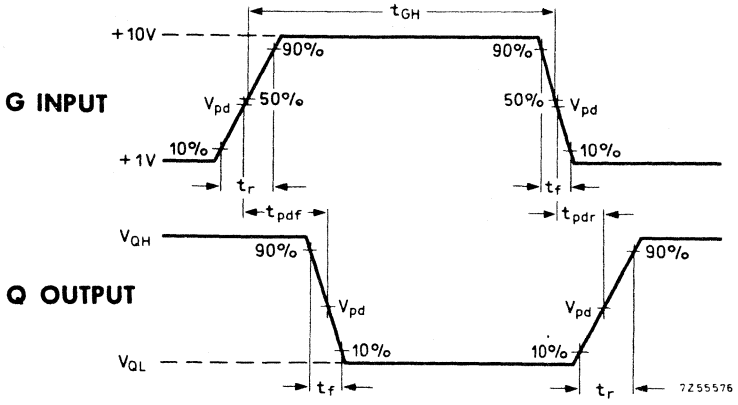
	Symbol	min.	typ.[1]	max.		Conditions and references: V_P (V)	Conditions and references
STATIC DATA							
Voltages							
Input HIGH	V_{GH}	7.5	–	– V		13.5	$V_{QL} \leq 1.7$ V; I_{QL} = 18 mA
Input LOW	V_{GL}	–	–	4.5 V		13.5 and 17	$V_{QH} \geq 12$ V; $-I_{QH}$ = 0.1 mA
Output HIGH	V_{QH}	12.0	14.3	– V		13.5 and 17	V_{GL} = 4.5 V; $-I_{QH}$ = 0.1 mA
Output LOW	V_{QL}	–	1.0	1.7 V		13.5	V_{GH} = 7.5 V; I_{QL} = 18 mA
D.C. noise margin: HIGH	M_H	4.5	8.0	– V		13.5	
LOW	M_L	2.8	5.0	– V		13.5	
Currents (per gate)							
Input HIGH	I_{GH}	–	–	1.0 µA		17	V_{GH} = 17 V; other inputs 0 V
Input LOW	$-I_{GL}$	–	1.0	1.8 mA		17	V_{GL} = 1.7 V; other inputs 17 V
Output HIGH	$-I_{QH}$	0.1	–	– mA		13.5 and 17	V_{GL} = 4.5 V; V_{QH} = 12 V
Output LOW	$-I_{QL}$	18	–	– mA		13.5	V_{GH} = 7.5 V; V_{QL} = 1.7 V
Output short circuited [2]	$-I_{Qsc}$	15	37	60 mA		17	V_G = 0 V; V_Q = 0 V
SUPPLY DATA							
Currents (per gate)							
at V_{QH}	I_P	–	1.2	2.1 mA		13.5	V_G = 0 V
at V_{QL}	I_P	–	2.3	4.0 mA		17	V_G = 17 V
DYNAMIC DATA							
Times							
Propagation delay:							
fall time	t_{pdf}	–	140	– ns		15	C_L = 10 pF; N = 1; T_{amb} = 25 °C; V_{pd} = 4.5 V
rise time	t_{pdr}	–	195	– ns		15	
output rise time	t_r	–	410	– ns		15	
output fall time	t_f	–	75	– ns		15	

[1]) All typical values under test conditions : T_{amb} = 25 °C and V_P = 15 V

[2]) Non-repetitive short circuit duration max. 2 s (duty cycle 10%)

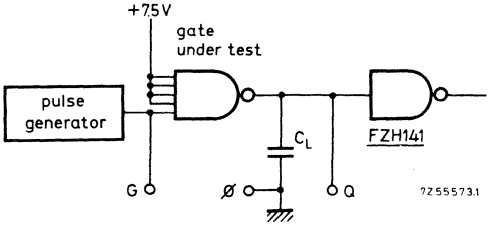
CHARACTERISTICS (continued)

DYNAMIC DATA



Pulse generator (G-input): t_r = 350 ns
t_f = 120 ns
t_{GH} = 1 µs

V_{pd} = + 4.5 V



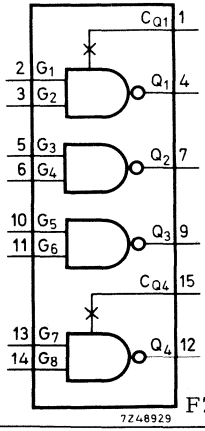
Measuring conditions: V_P = + 12 V; + 15 V
C_L = 10 pF (including probe and jig capacitance)
T_{amb} = 25 °C

Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf}

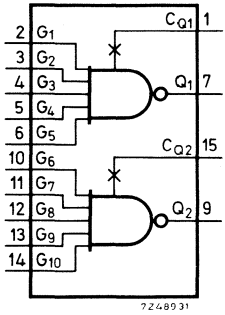
The FZfamily of HNIL silicon monolithic integrated circuits has been designed for high noise immunity low speed digital applications in industrial control and computer periphery equipment.

FZH111: QUADRUPLE 2-INPUT NAND GATE with slow-down capability

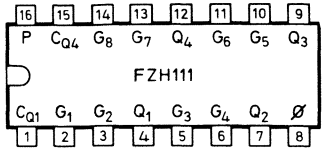
FZH131: DUAL 5-INPUT NAND GATE with slow-down capability

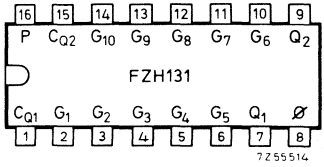


FZH111



FZH131





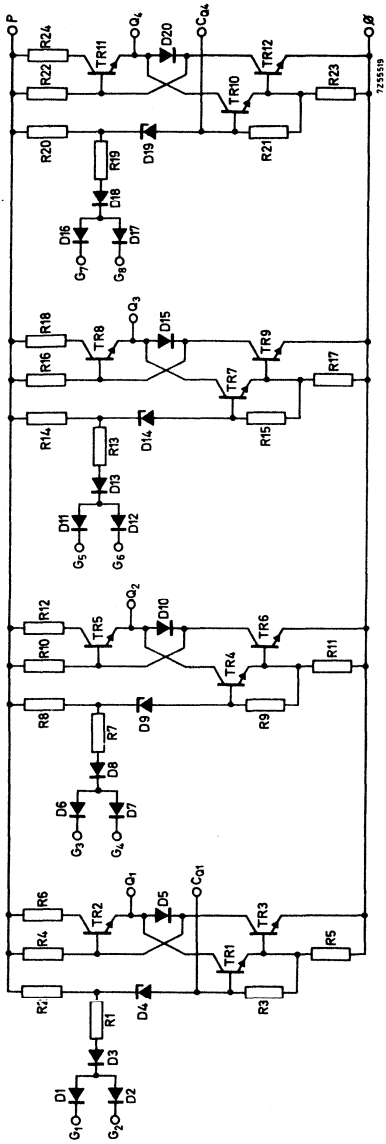
QUICK REFERENCE DATA				
Supply voltage (range I)	V_P	12	$+12\frac{1}{2}\%$ -5%	V
(range II)	V_P	15	$+13\%$ -10%	V
Operating ambient temperature	T_{amb}	0	to +70	°C
Average propagation delay time (N = 1; C_L = 10 pF; T_{amb} = 25 °C; V_{pd} = 4.5 V	t_{pd}	typ.	170	ns
Available d.c. fan-out LOW state (T_{amb} = 0 to +70 °C)	N_{aL}	max.	10	
Available d.c. fan-out HIGH state (T_{amb} = 0 to +70 °C)	N_{aH}	max.	100	
D.C. noise margin at T_{amb} = 25 °C range I : V_P = 12 V	$M_L = M_H$	typ.	5	V
range II: V_P = 15 V	M_L	typ.	5	V
	M_H	typ.	8	V
Power consumption per gate at T_{amb} = 25 °C (50% duty cycle) range I : V_P = 12 V	P_{av}	typ.	16	mW
range II: V_P = 15 V	P_{av}	typ.	27	mW

The FZH111 and FZH131 consist of a number of independent NAND gates at which two NAND gates per type have a special terminal (C_Q). It is possible to connect a capacitor between the output (Q) and the corresponding slow-down terminal C_Q to increase the propagation delay time.

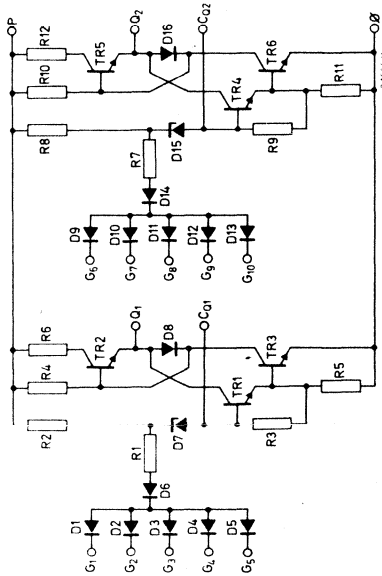
PACKAGE OUTLINE 16 lead plastic dual in-line (type B) (See General Section).

CIRCUIT DIAGRAMS

FZH111

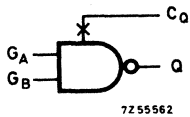


FZH131



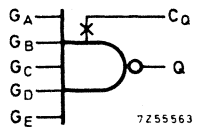
LOGIC FUNCTION

FZH111



$Q = \overline{G_A \cdot G_B}$ (positive logic)

FZH131



$Q = \overline{G_A \cdot G_B \cdot G_C \cdot G_D \cdot G_E}$ (positive logic)

Function tables

G_A	G_B	Q
L	X	H
X	L	H
H	H	L

G_A	G_B	G_C	G_D	G_E	Q
L	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H
H	H	H	H	H	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is inmaterial

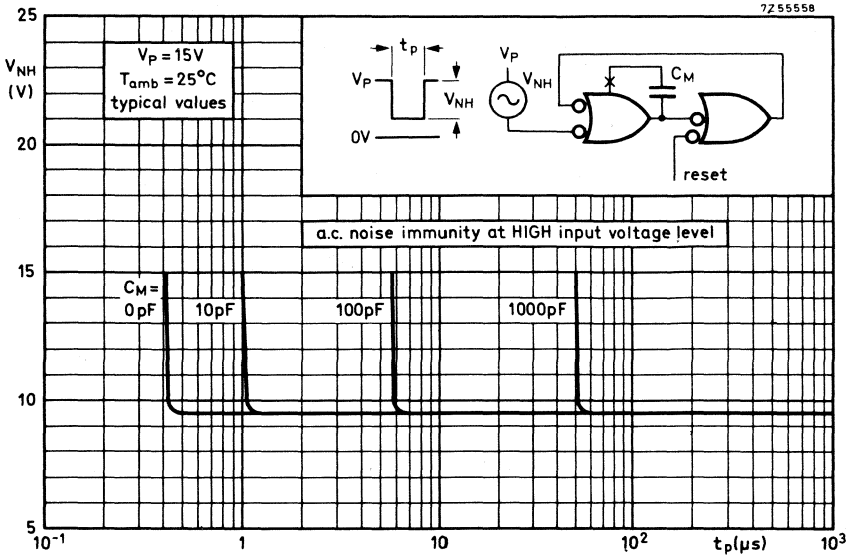
RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18	V
Output voltage	V_Q	max.	12	V
Input voltage	V_G	max.	18	V
Input current at V_P = 17 V; $-V_{Gtyp}$ = 5 V	$-I_{GL}$	max.	25	mA
Voltage difference between any two inputs		max.	18	V
Storage temperature	T_{stg}		−65 to +150	°C
Operating ambient temperature	T_{amb}		0 to +70	°C
Output short circuit duration duty cycle 10 %	t_{Qsc}	max.	2	s
Slow-down input voltage	$+V_{CQ}$	max.	0.6	V
	$-V_{CQ}$	max.	1.0	V
Slow-down input current	$+I_{CQ}$	max.	2.0	mA
	$-I_{CQ}$	max.	10.0	mA

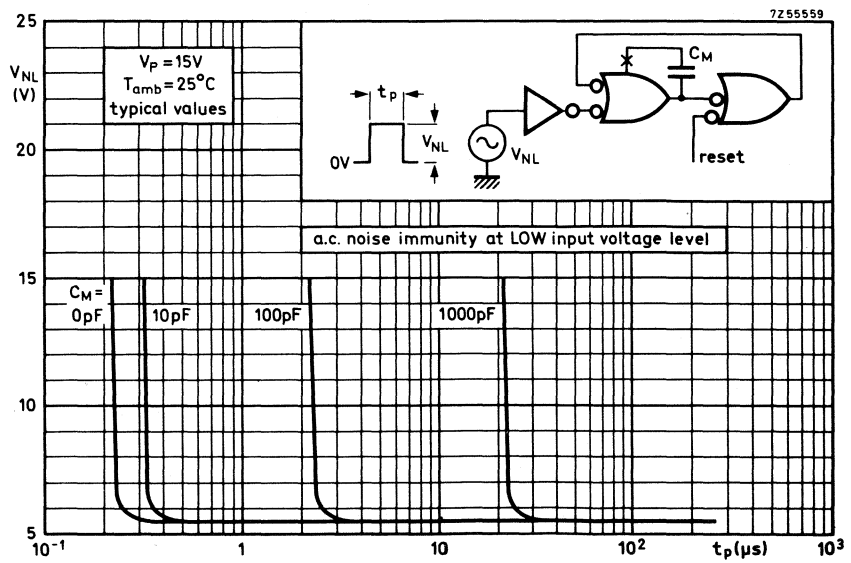
SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to +70		°C
Uniform system supply voltage (range I)	V_P	11.4 to 13.5		V
(range II)	V_P	13.5 to 17		V
Available d.c. fan-out	N_{aL}	max.	10	
	N_{aH}	max.	100	
D.C. noise margin; range I at V_{Pmin}	M_L	min.	2.8	V
	M_H	min.	2.5	V
range II at V_{Pmin}	M_L	min.	2.8	V
	M_H	min.	4.5	V
Supply current at range I ; output HIGH	I_{Pav}	typ.	0.9	mA
output LOW	I_{Pav}	typ.	1.7	mA
at range II; output HIGH	I_{Pav}	typ.	1.2	mA
output LOW	I_{Pav}	typ.	2.3	mA
Power consumption per gate (50% duty cycle) at range I ; V_{Pmax}	P_{tot}	max.	28	mW
at range II ; V_{Pmax}	P_{tot}	max.	46	mW
Thermal resistance from system to ambient	R_{th}	max.	150	°C/W

SYSTEM DESIGN DATA (continued)



Typical curves for HIGH-input voltage level



Typical curves for LOW-input voltage level

CHARACTERISTICS Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Sym-bol	min.	typ.[1]	max.	Conditions and references: V_P (V)	Conditions and references
STATIC DATA						
Voltages						
Input HIGH	V_{GH}	7.5	–	– V	11.4	$V_{QL} \leqslant 1.7$ V; I_{QL} = 15 mA
Input LOW	V_{GL}	–	–	4.5 V	11.4 and 13.5	$V_{QH} \geqslant 10$ V; $-I_{QH}$ = 0.1 mA
Output HIGH	V_{QH}	10.0	11.3	– V	11.4 and 13.5	V_{GL} = 4.5 V; $-I_{QH}$ = 0.1 mA
Output LOW	V_{QL}	–	0.9	1.7 V	11.4	V_{GH} = 7.5 V; I_{QL} = 15 mA
D.C. noise margin: HIGH	M_H	2.5	5.0	– V	11.4	
LOW	M_L	2.8	5.0	– V	11.4	
Currents (per gate)						
Input HIGH	I_{GH}	–	–	1.0 μA	13.5	V_{GH} = 13.5 V; other inputs 0 V
Input LOW	$-I_{GL}$	–	0.8	1.5 mA	13.5	V_{GL} = 1.7 V; other inputs 13.5 V
Output HIGH	$-I_{QH}$	0.1	–	– mA	11.4 and 13.5	V_{GL} = 4.5 V; V_{QH} = 10 V
Output LOW	I_{QL}	15	–	– mA	11.4	V_{GH} = 7.5 V; V_{QL} = 1.7 V
Output short circuited[2]	$-I_{Qsc}$	10	30	50 mA	13.5	V_G = 0 V; V_Q = 0 V
SUPPLY DATA						
Currents (per gate)						
at V_{QH}	I_P	–	0.9	1.6 mA	13.5	V_G = 0 V
at V_{QL}	I_P	–	1.7	3.0 mA	13.5	V_G = 13.5 V
DYNAMIC DATA						
Times:						
Propagation delay						
fall time	t_{pdf}	90	175	310 ns	12	C_L = 10 pF; N = 1; T_{amb} = 25 °C; V_{pd} = 4.5 V
rise time	t_{pdr}	90	175	310 ns	12	
output rise time	t_r	200	340	570 ns	12	
output fall time	t_f	70	120	210 ns	12	

[1] All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V

[2] Non-repetitive short circuit duration max. 2 s (duty cycle 10 %)

CHARACTERISTICS Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

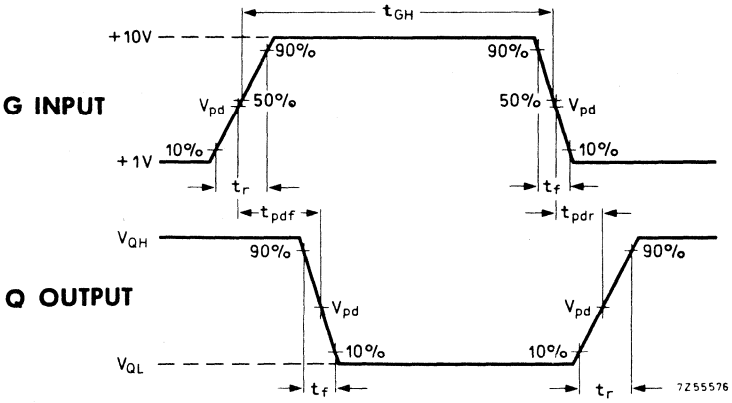
	Symbol	min.	typ.[1]	max.	Conditions and references: V_P (V)	Conditions and references
STATIC DATA						
Voltages						
Input HIGH	V_{GH}	7.5	–	– V	13.5	$V_{QL} \leqslant 1.7$ V; I_{QL} = 18 mA
Input LOW	V_{GL}	–	–	4.5 V	13.5 and 17	$V_{QH} \geqslant 12$ V; $-I_{QH}$ = 0.1 mA
Output HIGH	V_{QH}	12.0	14.3	– V	13.5 and 17	V_{GL} = 4.5 V; $-I_{QH}$ = 0.1 mA
Output LOW	V_{QL}	–	1.0	1.7 V	13.5	V_{GH} = 7.5 V; I_{QL} = 18 mA
D.C. noise margin: HIGH	M_H	4.5	8.0	– V	13.5	
LOW	M_L	2.8	5.0	– V	13.5	
Currents (per gate)						
Input HIGH	I_{GH}	–	–	1.0 μA	17	V_{GH} = 17 V; other inputs 0 V
Input LOW	$-I_{GL}$	–	1.0	1.8 mA	17	V_{GL} = 1.7 V; other inputs 17 V
Output HIGH	$-I_{QH}$	0.1	–	– mA	13.5 and 17	V_{GL} = 4.5 V; V_{QH} = 12 V
Output LOW	I_{QL}	18	–	– mA	13.5	V_{GH} = 7.5 V; V_{QL} = 1.7 V
Output short circuited [2]	$-I_{Qsc}$	15	37	60 mA	17	V_G = 0 V; V_Q = 0 V
SUPPLY DATA						
Currents (per gate)						
at V_{QH}	I_P	–	1.2	2.1 mA	17	V_G = 0 V
at V_{QL}	I_P	–	2.3	4.0 mA	17	V_G = 17 V
DYNAMIC DATA						
Times:						
Propagation delay						
fall time	t_{pdf}	–	140	– ns	15	C_L = 10 pF; N = 1; T_{amb} = 25 °C; V_{dp} = 4.5 V
rise time	t_{pdr}	–	195	– ns	15	
output rise time	t_r	–	410	– ns	15	
output fall time	t_f	–	75	– ns	15	

[1] All typical values under test conditions: T_{amb} = 25 °C and V_P = 15 V

[2] Non-repetitive short circuit duration max. 2 s (duty cycle 10 %)

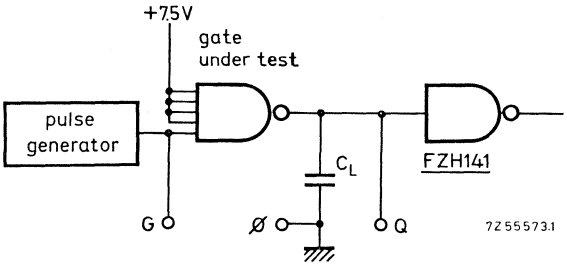
CHARACTERISTICS (continued)

DYNAMIC DATA



Pulse generator (G-input): t_r = 350 ns
t_f = 120 ns
tGH = 1 µs

V_{pd} = + 4.5 V

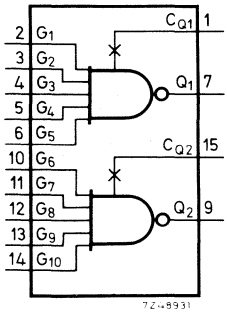


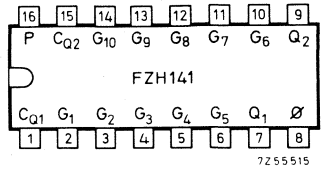
Measuring conditions: V_P = + 12 V; + 15 V
C_L = 10 pF (including probe and jig capacitance)
T_{amb} = 25 °C
Slow-down terminals are not connected

Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf}

The FZ family of HNiL silicon monolithic integrated circuits has been designed for high noise immunity low speed digital applications in industrial control and computer periphery equipment.

DUAL 5-INPUT POWER NAND GATE
with slow-down capability





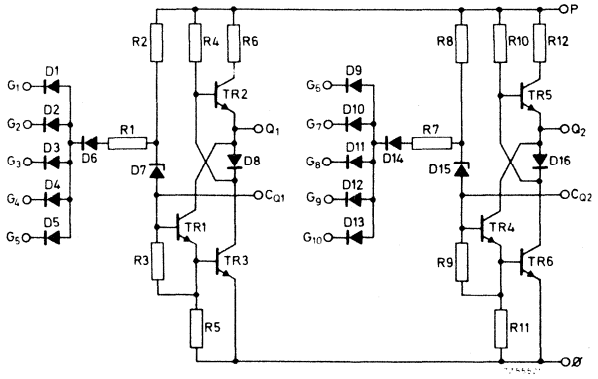
QUICK REFERENCE DATA

Supply voltage (range I)	V_P	$12 \begin{smallmatrix}+12\frac{1}{2}\% \\ -5\ \%\end{smallmatrix}$	V
(range II)	V_P	$15 \begin{smallmatrix}+13\ \% \\ -10\ \%\end{smallmatrix}$	V
Operating ambient temperature	T_{amb}	0 to +70	°C
Average propagation delay time ($N = 1$; $C_L = 10$ pF; $T_{amb} = 25$ °C; $V_{pd} = 4.5$ V	t_{pd}	typ. 170	ns
Available d.c. fan-out (LOW state ($T_{amb} = 0$ to +70 °C)	N_{aL}	max. 30	
Available d.c. fan-out (HIGH state ($T_{amb} = 0$ to +70 °C)	N_{aH}	max. 100	
D.C. noise margin at $T_{amb} = 25$ °C range I : $V_P = 12$ V	$M_L = M_H$	typ. 5	V
	M_L	typ. 5	V
range II : $V_P = 15$ V	M_H	typ. 8	V
Power consumption per gate at $T_{amb} = 25$ °C (50% duty cycle) range I : $V_P = 12$ V	P_{av}	typ. 16	mW
range II : $V_P = 15$ V	P_{av}	typ. 27	mW

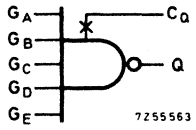
The FZH141 is a dual 5 input power NAND gate with on each gate a special base connection. It is possible to connect a capacitor between the output (Q) and the corresponding slow-down terminal CQ to increase the propagation delay time.

PACKAGE OUTLINE 16 lead plastic dual in-line (type B) (See General Section).

CIRCUIT DIAGRAM



LOGIC FUNCTION



$$Q = \overline{G_A \cdot G_B \cdot G_C \cdot G_D \cdot G_E}$$
(positive logic)

Function table

G_A	G_B	G_C	G_D	G_E	Q
L	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H
H	H	H	H	H	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

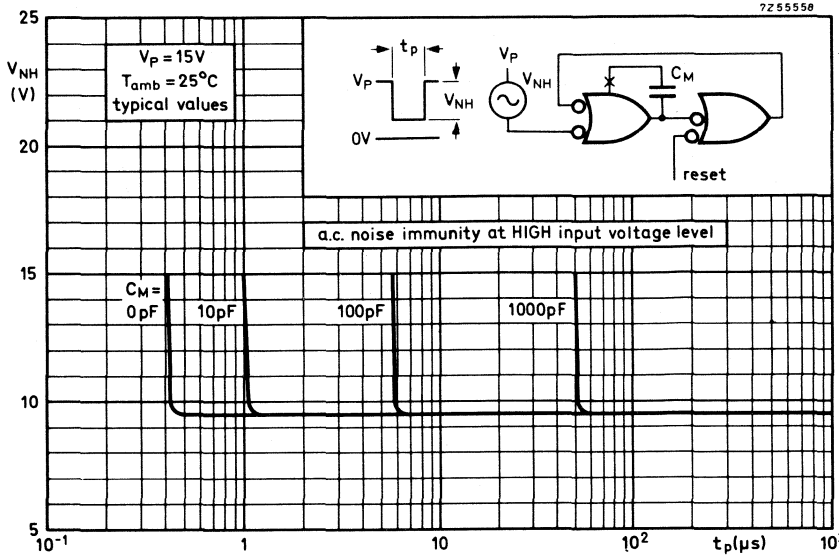
RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18	V
Output voltage	V_Q	max.	12	V
Input voltage	V_G	max.	18	V
Input current at V_P = 17 V; $-V_{Gtyp}$ = 5 V	$-I_{GL}$	max.	25	mA
Voltage difference between any two inputs		max.	18	V
Storage temperature	T_{stg}	−65 to +150		°C
Operating ambient temperature	T_{amb}	0 to +70		°C
Output short circuit duration duty cycle 10 %	t_{Qsc}	max.	2	s
Slow-down input voltage	$+V_{CQ}$	max.	0.6	V
	$-V_{CQ}$	max.	1.0	V
Slow-down input current	$+I_{CQ}$	max.	2.0	mA
	$-I_{CQ}$	max.	10.0	mA

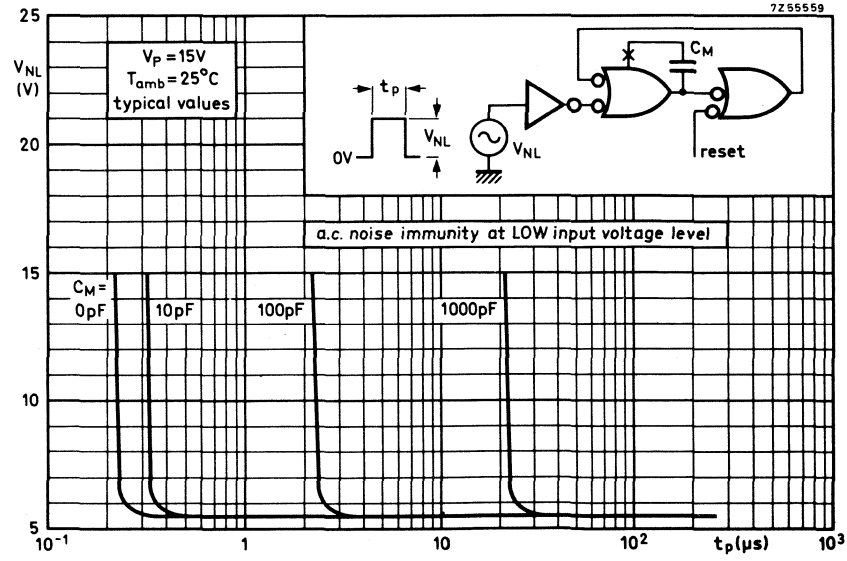
SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to +70		°C
Uniform system supply voltage (range I)	V_P	11.4 to 13.5		V
(range II)	V_P	13.5 to 17		V
Available d.c. fan-out	N_{aL}	max.	30	
	N_{aH}	max.	100	
D.C. noise margin; range I at V_{Pmin}	M_L	min.	2.8	V
	M_H	min.	2.5	V
range II at V_{Pmin}	M_L	min.	2.8	V
	M_H	min.	4.5	V
Supply current at range I; output HIGH	I_{Pav}	typ.	0.9	mA
output LOW	I_{Pav}	typ.	1.7	mA
at range II; output HIGH	I_{Pav}	typ.	1.2	mA
output LOW	I_{Pav}	typ.	2.3	mA
Power consumption per gate (50% duty cycle) at range I ; V_{Pmax}	P_{tot}	max.	28	mW
at range II ; V_{Pmax}	P_{tot}	max.	46	mW
Thermal resistance from system to ambient	R_{th}	max.	150	°C/W

SYSTEM DESIGN DATA (continued)



Typical curves for HIGH-input voltage level



Typical curves for LOW-input voltage level

CHARACTERISTICS Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Sym-bol	min.	typ. [1]	max.	Conditions and references: V_P (V)	Conditions and references:
STATIC DATA						
Voltages						
Input HIGH	V_{GH}	7.5	-	- V	11.4	$V_{QL} \leqslant 1.7$ V; I_{QL} = 45 mA
Input LOW	V_{GL}	-	-	4.5 V	11.4 and 13.5	$V_{QH} \geqslant 10$ V; $-I_{QH}$ = 0.1 mA
Output HIGH	V_{QH}	10.0	11.3	- V	11.4 and 13.5	V_{GL} = 4.5 V; $-I_{QH}$ = 0.1 mA
Output LOW	V_{QL}	-	1.3	1.7 V	11.4	V_{GH} = 7.5 V; I_{QL} = 45 mA
D. C. noise margin: HIGH	M_H	2.5	5.0	- V	11.4	
LOW	M_L	2.8	5.0	- V	11.4	
Currents (per gate)						
Input HIGH	I_{GH}	-	-	1.0 µA	13.5	V_{GH} = 13.5 V; other inputs 0 V
Input LOW	$-I_{GL}$	-	0.8	1.5 mA	13.5	V_{GL} = 1.7 V; other inputs 13.5 V
Output HIGH	$-I_{QH}$	0.1	-	- mA	11.4 and 13.5	V_{GL} = 4.5 V; V_{QH} = 10 V
Output LOW	I_{QL}	45	-	- mA	11.4	V_{GH} = 7.5 V; V_{QL} = 1.7 V
Output short circuited [2]	$-I_{Qsc}$	10	30	50 mA	13.5	V_G = 0 V; V_Q = 0 V
SUPPLY DATA						
Currents (per gate)						
at V_{QH}	I_P	-	0.9	1.6 mA	13.5	V_G = 0 V
at V_{QL}	I_P	-	1.7	3.0 mA	13.5	V_G = 13.5 V
DYNAMIC DATA						
Times						
Propagation delay						
fall time	t_{pdf}	90	175	310 ns	12	
rise time	t_{pdr}	90	175	310 ns	12	C_L = 10 pF; N = 1; T_{amb} = 25 °C
output rise rime	t_r	200	340	570 ns	12	
output fall time	t_f	70	120	210 ns	12	V_{pd} = 4.5 V

[1] All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V

[2] Non-repetitive short circuit duration max. 2 s (duty cycle 10%)

CHARACTERISTICS Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

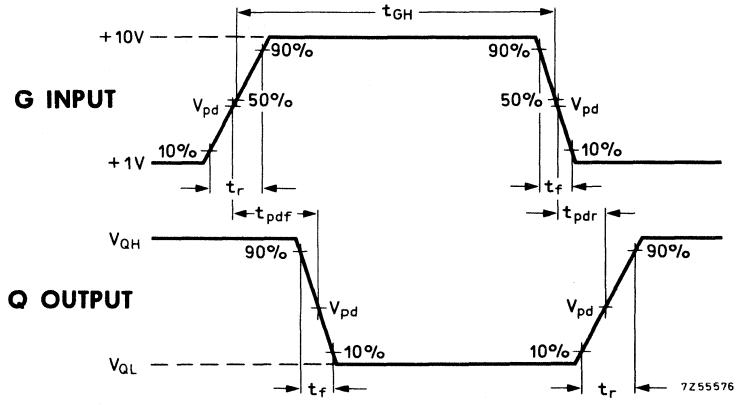
	Sym-bol	min.	typ. [1]	max.	Conditions and references: V_P (V)	
STATIC DATA						
Voltages						
Input HIGH	V_{GH}	7.5	-	- V	13.5	$V_{QL} \leqslant 1.7$ V; I_{QL} = 54 mA
Input LOW	V_{GL}	-	-	4.5 V	13.5 and 17	$V_{QH} \geqslant 12$ V; $-I_{QH}$ = 0.1 mA
Output HIGH	V_{QH}	12.0	14.3	- V	13.5 and 17	V_{GL} = 4.5 V; $-I_{QH}$ = 0.1 mA
Output LOW	V_{QL}	-	1.4	1.7 V	13.5	V_{GH} = 7.5 V; I_{QL} = 54 mA
D.C. noise margin: HIGH	M_H	4.5	8.0	- V	13.5	
LOW	M_L	2.8	5.0	- V	13.5	
Currents (per gate)						
Input HIGH	I_{GH}	-	-	1.0 µA	17	V_{GH} = 17 V; other inputs 0 V
Input LOW	$-I_{GL}$	-	-	1.8 mA	17	V_{GL} = 1.7 V; other inputs 17 V
Output HIGH	$-I_{QH}$	0.1	-	- mA	13.5 and 17	V_{GL} = 4.5 V; V_{QH} = 12 V
Output LOW	I_{QL}	54	-	- mA	13.5	V_{GH} = 7.5 V; V_{QL} = 1.7 V
Output short circuited [2]	$-I_{Qsc}$	15	37	60 mA	17	V_G = 0 V; V_Q = 0 V
SUPPLY DATA						
Currents (per gate)						
at V_{QH}	I_P	-	1.2	2.1 mA	13.5	V_G = 0 V
at V_{QL}	I_P	-	2.3	4.0 mA	17	V_G = 17 V
DYNAMIC DATA						
Times						
Propagation delay						
fall time	t_{pdf}	-	140	- ns	15	C_L = 10 pF; N = 1; T_{amb} = 25 °C; V_{dp} = 4.5 V
rise time	t_{pdr}	-	195	- ns	15	
output rise time	t_r	-	410	- ns	15	
output fall time	t_f	-	75	- ns	15	

[1]) All typical values under test conditions: T_{amb} = 25 °C and V_P = 15 V

[2]) Non-repetitive short circuit duration max. 2 s (duty cycle 10 %)

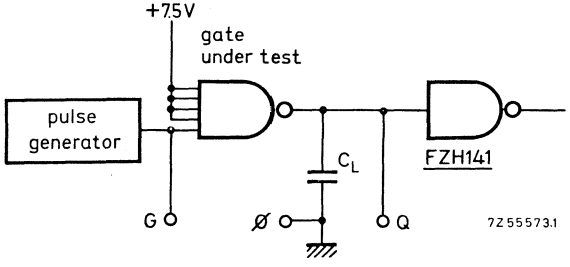
CHARACTERISTICS (continued)

DYNAMIC DATA



Pulse generator (G-input): t_r = 350 ns
t_f = 120 ns
t_{GH} = 1 µs

V_{pd} = +4.5 V

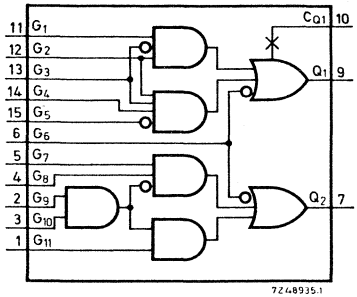


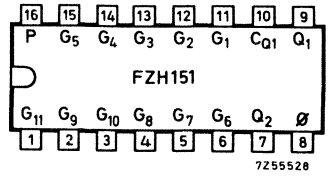
Measuring conditions: V_P = + 12 V; + 15 V
C_L = 10 pF (including probe and jig capacitance)
T_{amb} = 25 °C
Slow-down terminals are not connected

Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf}

The FZ family of HNIL silicon monolithic integrated circuits has been designed for high noise immunity low speed digital applications in industrial control and computer periphery equipment.

AND - OR gate with slow-down capability

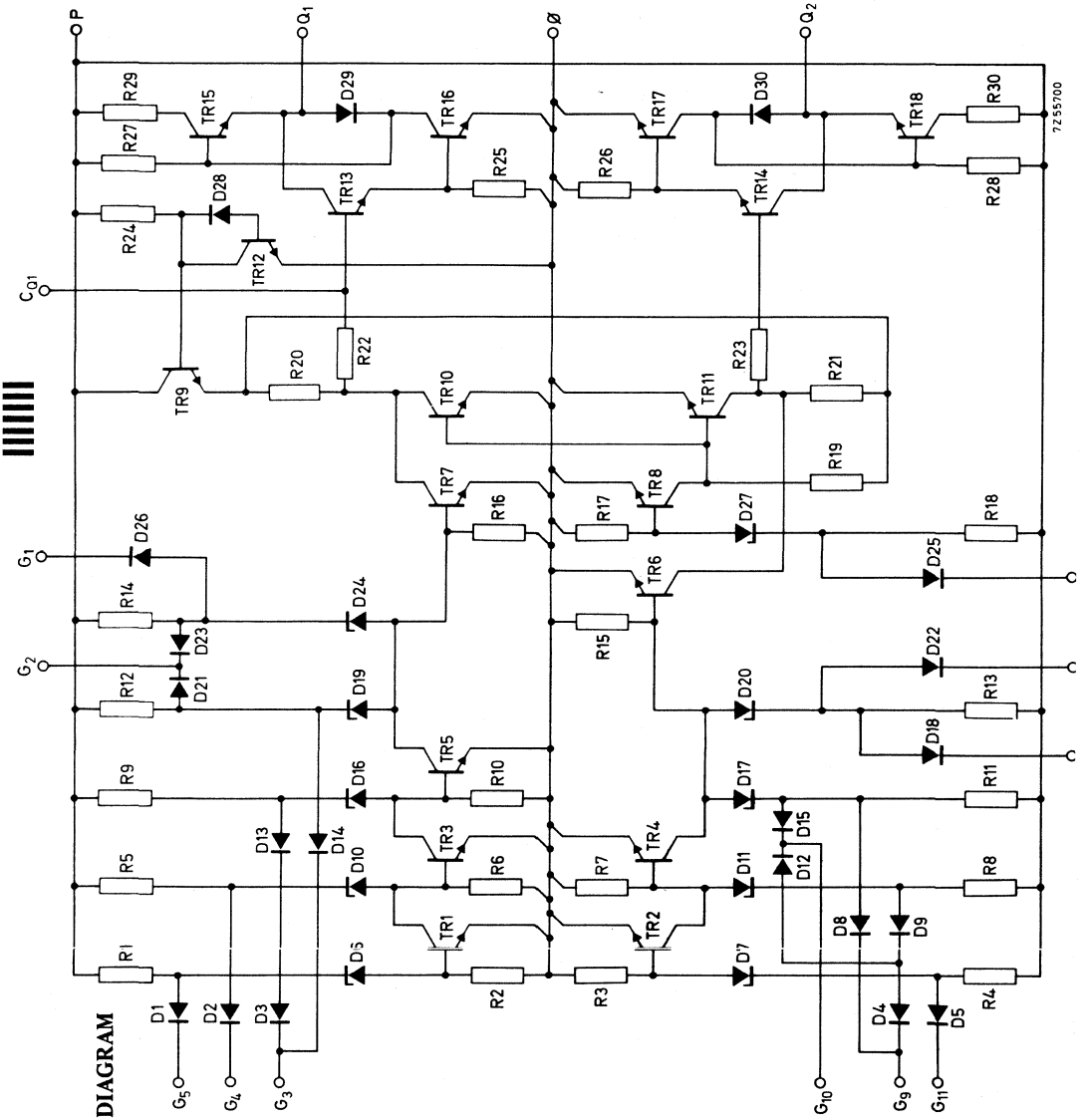




QUICK REFERENCE DATA				
Supply voltage (range I)	V_P	12 $^{+12\frac{1}{2}\,\%}_{-5\,\%}$		V
(range II)	V_P	15 $^{+13\,\%}_{-10\,\%}$		V
Operating ambient temperature	T_{amb}	0 to +70		°C
Average propagation delay time ($N = 1$; $C_L = 10$ pF; $T_{amb} = 25$ °C; $V_{pd} = 4.5$ V)	tpd	typ.	380	ns
Available d.c. fan-out ($T_{amb} = 0$ to +70 °C) LOW state at FZH151 load	N_{aL}	max.	24	
Available d.c. fan-out ($T_{amb} = 0$ to +70 °C) LOW state at HNIL load	N_{aL}	max.	20	
Available d.c. fan-out ($T_{amb} = 0$ to +70 °C) HIGH state	N_{aH}	max.	100	
D.C. noise margin at T_{amb} = 25 °C; range I: V_P = 12 V	$M_L = M_H$	typ.	5	V
range II: V_P = 15 V	M_L	typ.	5	V
	M_H	typ.	8	V
Power consumption per gate at T_{amb} = 25 °C (50 % duty cycle) range I: V_P = 12 V	P_{av}	typ.	132	mW
range II: V_P = 15 V	P_{av}	typ.	225	mW

The FZH151 consists of two combinations of AND and OR gates with some common inputs to the AND gates and a common override input to the OR gates. One of the OR gates has a special terminal to provide slow-down capability.

PACKAGE OUTLINE 16 lead plastic dual in-line (type B) (See General Section).



CIRCUIT DIAGRAM

LOGIC FUNCTION

$$Q_1 = G_1 \cdot G_2 \cdot \overline{G_3} + G_2 \cdot G_3 \cdot G_4 \cdot \overline{G_5} + \overline{G_6}$$

$$Q_2 = G_7 \cdot G_8 \cdot \overline{G_9 \cdot G_{10}} + G_9 \cdot G_{10} \cdot G_{11} + \overline{G_6}$$

} for positive logic

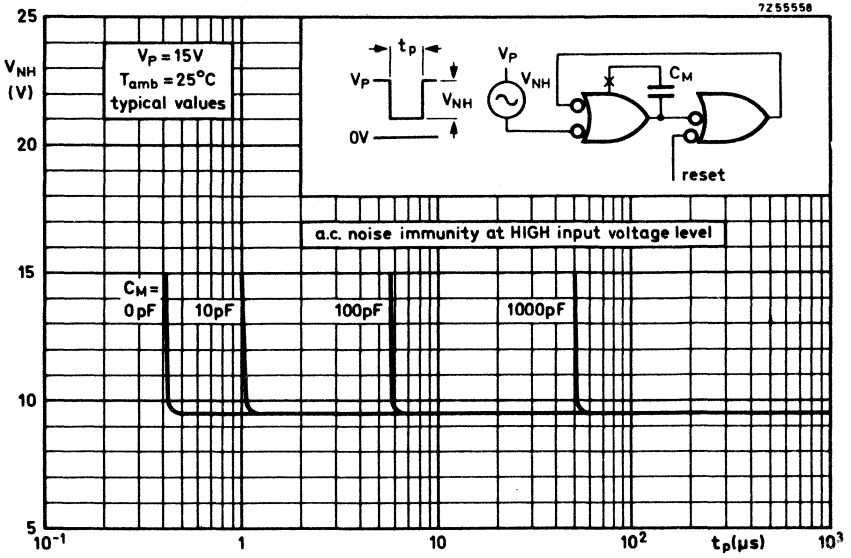
RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18	V
Output voltage	V_Q	max.	12	V
Input voltage	V_G	max.	18	V
Input current at V_P = 17 V; $-V_{Gtyp}$ = 0.7 V	$-I_G$	max.	6	mA
Input current	$-I_{GL}$	max.	25	mA
Voltage difference between any two inputs		max.	18	V
Slow-down input voltage	$+V_{CQ}$	max.	0.6	V
	$-V_{CQ}$	max.	1.0	V
Slow-down input current	$+I_{CQ}$	max.	2.0	mA
	$-I_{CQ}$	max.	10.0	mA
Storage temperature	T_{stg}		−65 to +150	°C
Operating ambient temperature	T_{amb}		0 to +70	°C
Output short circuit duration duty cycle 10 %	t_{Qsc}	max.	2	s

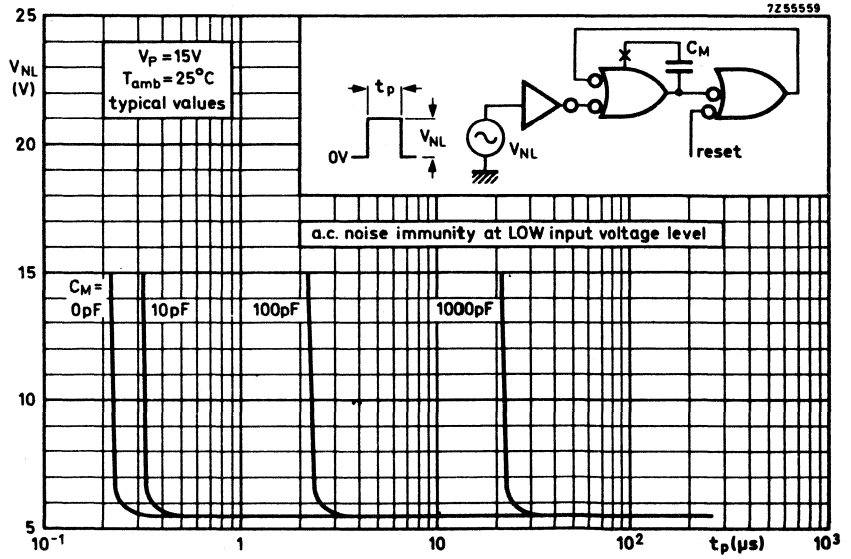
SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to	70	°C
Uniform system supply voltage (range I)	V_P	11.4 to	13.5	V
(range II)	V_P	13.5 to	17	V
Available d.c. fan-out: at FZH151 load	N_{aL}	max.	24	
at HNIL gate load	N_{aL}	max.	20	
	N_{aH}	max.	100	
D.C. noise margin; range I at V_{Pmin}	M_L	min.	2.8	V
	M_H	min.	2.5	V
range II at V_{Pmin}	M_L	min.	2.8	V
	M_H	min.	4.5	V
Supply current at range I ; output HIGH	I_{Pav}	typ.	14	mA
output LOW	I_{Pav}	typ.	8.0	mA
at range II; output HIGH	I_{Pav}	typ.	18	mA
output LOW	I_{Pav}	typ.	12	mA
Power consumption per gate (50% duty cycle) at range I , V_{Pmax}	P_{tot}	max.	236	mW
at range II, V_{Pmax}	P_{tot}	max.	388	mW
Thermal resistance from system to ambient	R_{th}	max.	150	°C/W

SYSTEM DESIGN DATA (continued)



Typical curves for HIGH-input voltage level



Typical curves for LOW-input voltage level

CHARACTERISTICS Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Sym-bol	min.	typ.[1]	max.		Conditions and references	
						V_P (V)	
STATIC DATA							
Voltages							
Input HIGH	V_{GH}	7.5	–	–	V	11.4	V_{QL} = max 1.7 V; I_{QL} = 30 mA
Input LOW	V_{GL}	–	–	4.5	V	11.4	V_{QH} = min 10 V; $-I_{GH}$ = 0.1 mA
Output HIGH	V_{QH}	10.0	11.3	–	V	11.4	V_{GL} = 4.5 V; $-I_{QH}$ = 0.1 mA
Output LOW	V_{QL}	–	0.9	1.7	V	11.4	V_{GH} = 7.5 V; I_{QL} = 30 mA
D.C. noise margin: HIGH	M_H	2.5	5.0	–	V		
LOW	M_L	2.8	5.0	–	V		
Currents							
Input HIGH: G_2;G_3;G_9;G_{10}	I_{GH}	–	–	2	μA	13.5	V_{GH} = 13.5 V; other inputs 0 V
at other G inputs	I_{GH}	–	–	1	μA		
Input LOW: G_2;G_3;G_9;G_{10}	$-I_{GL}$	–	1.0	2.5	mA	13.5	V_{GL} = 1.7 V; other inputs 13.5V
at other G inputs	$-I_{GL}$	–	0.5	1.25	mA		
Output HIGH	$-I_{QH}$	0.1	–	–	mA	11.4	V_{GL} = 4.5 V; V_{QH} = 10 V
Output LOW	I_{QL}	30	–	–	mA	11.4	V_{GH} = 7.5 V; V_{QL} = 1.7 V
Output short circuited[2]	$-I_{Qsc}$	10	30	50	mA	13.5	V_G = 0 V; V_Q = 0 V
SUPPLY DATA							
Currents							
at V_{QH}	I_P	–	14.0	22.0	mA	13.5	V_G = 0 V
at V_{QL}	I_P	–	8.0	15.0	mA	13.5	V_{G11} = V_{GL}; other G inputs: V_{GH}

[1]) All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V
[2]) Non-repetitive short circuit duration max. 2 s (duty cycle 10 %)

CHARACTERISTICS (continued from page 6)

	Sym-bol	min.	typ.[1]	max.		Conditions and references	
						V_P (V)	
DYNAMIC DATA							
Times							
Propagation delay							
fall times at output Q	t_{pdf1}	–	230	–	ns	12	C_L = 10 pF N = 1 T_{amb} = 25 °C V_{pd} = 4.5 V
at output $\overline{Q}$	t_{pdf2}	–	300	–	ns	12	
at input G_5	t_{pdf3}	–	400	–	ns	12	
rise times at output Q	t_{pdr1}	–	340	–	ns	12	
at output $\overline{Q}$	t_{pdr2}	–	340	–	ns	12	
at input G_5	t_{pdr3}	–	270	–	ns	12	
Output rise time	t_r	–	330	–	ns	12	
Output fall time	t_f	–	200	–	ns	12	

[1]) All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V

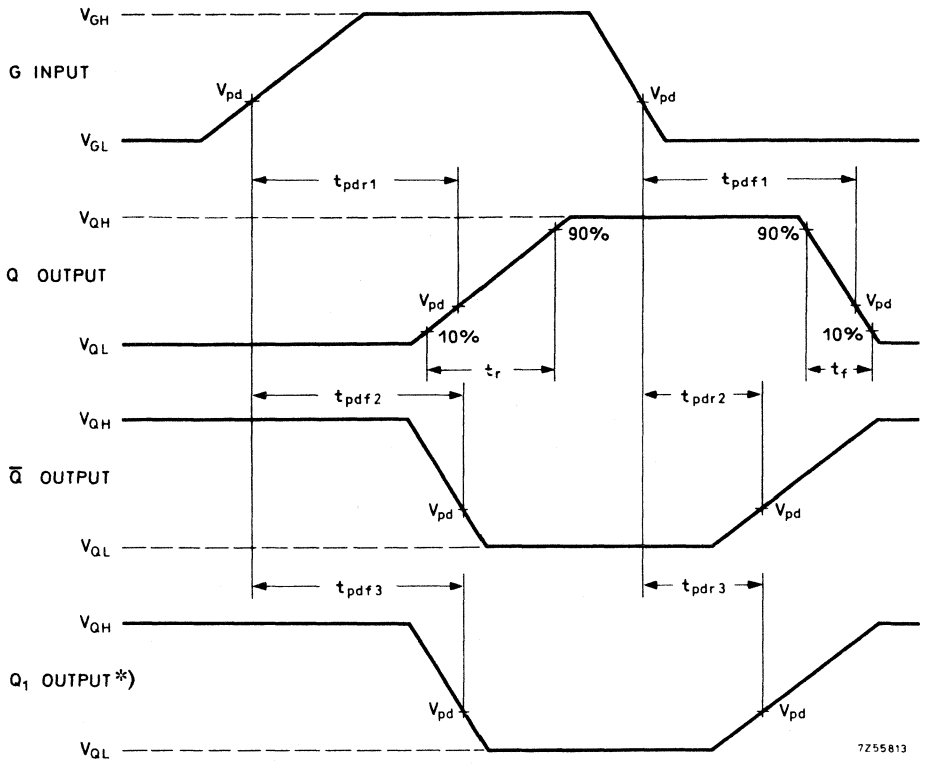
CHARACTERISTICS Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

	Sym-bol	min.	typ.[1]	max.	Conditions and references: V_P (V)	Conditions and references
STATIC DATA						
Voltages						
Input HIGH	V_{GH}	7.5	–	– V	13.5	V_{QL} = max. 1.7 V; I_{QL} = 36 mA
Input LOW	V_{GL}	–	–	4.5 V	13.5	V_{QH} = min. 12 V; $-I_{QH}$ = 0.1 mA
Output HIGH	V_{QH}	12.0	14.3	– V	13.5	V_{GL} = 4.5 V; $-I_{QH}$ = 0.1 mA
Output LOW	V_{QL}	–	1.0	1.7 V	13.5	V_{GH} = 7.5 V; I_{QL} = 36 mA
D.C. noise margin: HIGH	M_H	4.5	8.0	– V	13.5	
LOW	M_L	2.8	5.0	– V	13.5	
Currents						
Input HIGH: $G_2;G_3;G_9;G_{10}$	I_{GH}	–	–	2.0 μA	17	V_{GH} = 17 V; other inputs 0 V
at other G inputs	I_{GH}	–	–	1.0 μA		
Input LOW: $G_2;G_3;G_9;G_{10}$	$-I_{GL}$	–	1.2	3.0 mA	17	V_{GL} = 1.7 V; other inputs 17 V
at other G inputs	$-I_{GL}$	–	0.6	1.5 mA		
Output HIGH	$-I_{QH}$	0.1	–	– mA	13.5	V_{GL} = 4.5 V; V_{QH} = 12 V
Output LOW	I_{QL}	36	–	– mA	13.5	V_{GH} = 7.5 V; V_{QL} = 1.7 V
Output short circuited[2]	$-I_{Qsc}$	15	37	60 mA	17	V_G = 0 V; V_Q = 0 V
SUPPLY DATA						
Currents						
at V_{QH}	I_P	–	18	29 mA	17	V_G = 0 V
at V_{QL}	I_P	–	12	21 mA	17	$V_{G11} = V_{GL}$; other G inputs: V_{GH}

[1] All typical values under test condiotions: T_{amb} = 25 °C and V_P = 15 V
[2] Non- repetitive short circuit duration max. 2 s (duty cycle 10 %)

CHARACTERISTICS (continued)

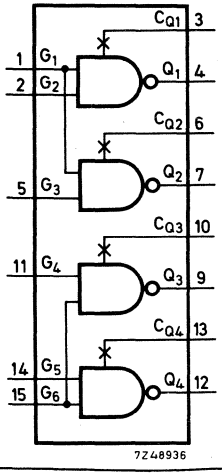
DYNAMIC DATA



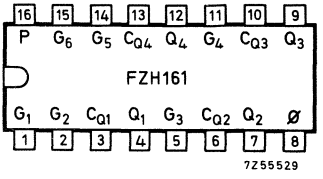
Waveforms illustrating measurement of t_{pdr} and t_{pdf}

*) If G input = G_5

The FZ family of HNIL silicon monolithic integrated circuits has been designed for high noise immunity low speed digital applications in industrial control and computer periphery equipment.



LEVEL CONVERTER HNIL to TTL with slow-down capabilities

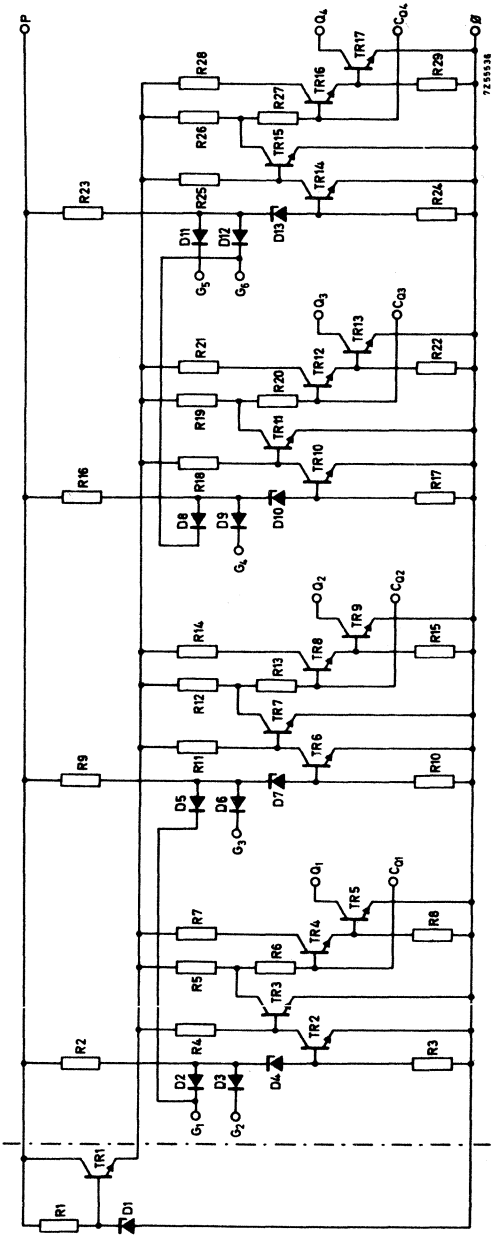


QUICK REFERENCE DATA			
Supply voltage (range I)	V_P	12 $^{+12\frac{1}{2}\ \%}_{-5\ \%}$	V
(range II)	V_P	15 $^{+13\ \%}_{-10\ \%}$	V
Operating ambient temperature	T_{amb}	0 to +70	°C
Average propagation delay			
V_P = 12 V ; N_a = 1 } V_Q = 12 V	t_{pd1}	typ. 115	ns
V_{pd} = 4.5 V; T_{amb} = 25 °C } V_Q = 5 V	t_{pd2}	typ. 105	ns
D.C. noise margin at T_{amb} = 25 °C			
range I : V_P = 12 V	$M_L = M_H$	typ. 5	V
range II : V_P = 15 V	M_L	typ. 5	V
	M_H	typ. 8	V
Power consumption per gate at T_{amb} = 25 °C			
(50 % duty cycle) range I : V_P = 12 V	P_{av}	typ. 39	mW
range II: V_P = 15 V	P_{av}	typ. 55	mW

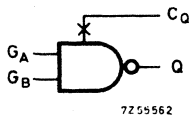
The FZH161 is a level converter with open collector output for HNIL to TTL and consists of 4 gates and some common inputs.
Each gate has a slow-down capability.

PACKAGE OUTLINE 16 lead plastic dual in-line (type B) (See General Section).

CIRCUIT DIAGRAM



LOGIC FUNCTION



$Q = \overline{G_A \cdot G_B}$

(for positive logic)

Function table

G_A	G_B	Q
L	X	H
X	L	H
H	H	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is inmaterial

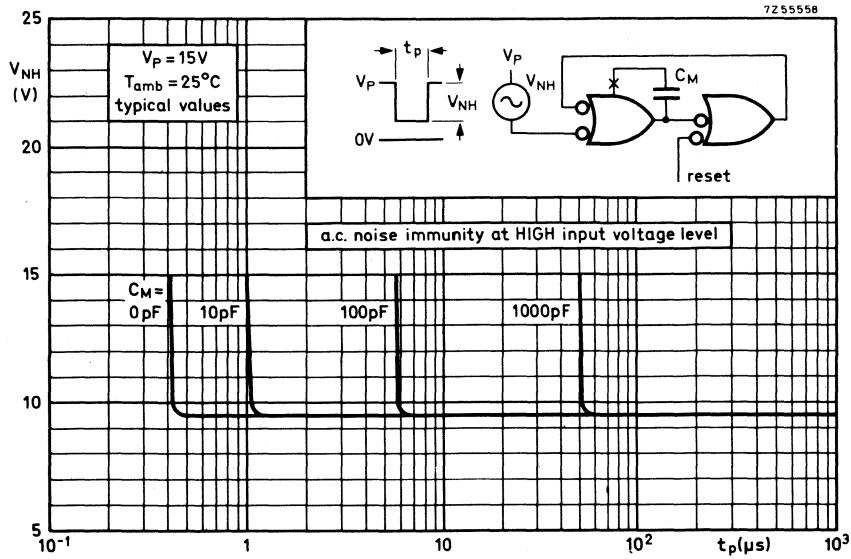
RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18	V
Output voltage (HIGH state)	V_Q	max.	18	V
Input voltage	V_G	max.	18	V
Input current ($-V_{Gtyp}$ = 5 V; V_P = 17 V; T_{amb} = 70 °C)	$-I_{GL}$	max.	25	mA
Voltage difference between any two inputs		max.	18	V
Slow-down input voltage	$+V_{CQ}$	max.	0.6	V
	$-V_{CQ}$	max.	1.0	V
Slow-down input current	$+I_{CQ}$	max.	2.0	mA
	$-I_{CQ}$	max.	10.0	mA
Storage temperature	T_{stg}	-65 to +150		°C
Operating ambient temperature	T_{amb}	0 to + 70		°C

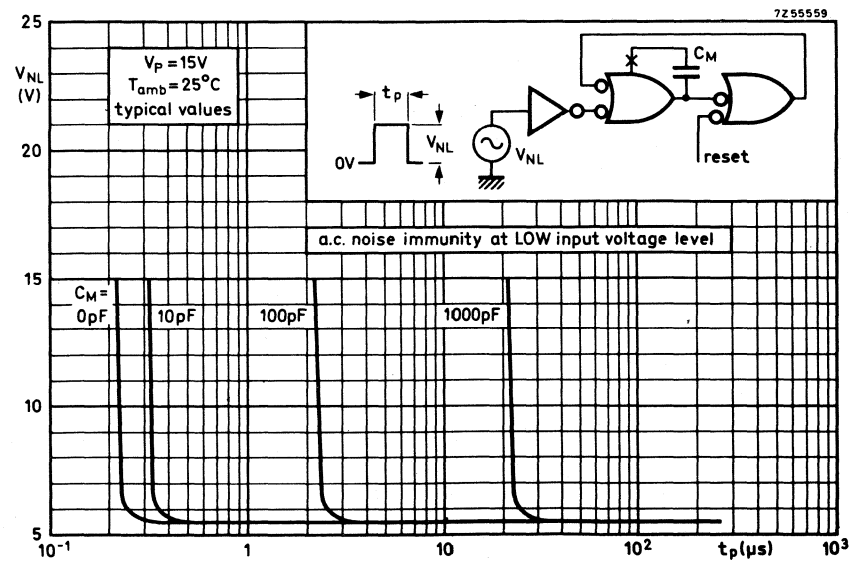
SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}		0 to +70	°C
Uniform system supply voltage (range I)	V_P		11.4 to 13.5	V
(range II)	V_P		13.5 to 17	V
Available output current	I_{QL}	min.	20	mA
	I_{QH}	max.	50	µA
D.C. noise margin; range I at V_{Pmin}	M_L	min.	2.8	V
	M_H	min.	2.5	V
range II at V_{Pmin}	M_L	min.	2.8	V
	M_H	min.	4.5	V
Supply current at range I ; output HIGH	I_{Pav}	typ.	2.5	mA
output LOW	I_{Pav}	typ.	4.0	mA
at range II; output HIGH	I_{Pav}	typ.	2.8	mA
output LOW	I_{Pav}	typ.	4.5	mA
Power consumption per gate (50 % duty cycle) at range I ; V_{Pmax}	P_{tot}	max.	77.5	mW
at range II; V_{Pmax}	P_{tot}	max.	110	mW
Average propagation delay				
at V_{pd1} = 4.5 V; (V_Q = 12 V)	t_{pd1}	max.	275	ns
at V_{pd2} = 1.5 V; (V_Q = 5 V)	t_{pd2}	max.	275	ns
Thermal resistance from system to ambient	R_{th}	max.	150	°C/W

SYSTEM DESIGN DATA (continued)



Typical curves for HIGH-input voltage level



Typical curves for LOW-input voltage level

CHARACTERISTICS

Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to + 70 °C.

	Sym-bol	min.	typ. [1]	max.	Conditions and references: V_P (V)	Conditions and references
STATIC DATA						
Voltages						
Input HIGH	V_{GH}	7.5	–	– V	11.4	V_{QL} = 0.4 V; I_{QL} = 20 mA
Input LOW	V_{GL}	–	–	4.5 V	11.4	V_{QH} = 13.5 V; I_{QH} = 40 µA
Output LOW	V_{QL}	–	–	0.4 V	11.4	V_{GH} = 7.5 V; I_{QL} = 20 mA
D.C. noise margin: HIGH	M_H	2.5	5.0	–	11.4	
LOW	M_L	2.8	5.0	–	11.4	
Currents (per gate)						
Input HIGH; G_2; G_3; G_4; G_5	I_{GH}	–	–	1.0 µA	13.5	V_{GH} = 13.5 V; other inputs 0V
G_1; G_6	I_{GH}	–	–	2.0 µA		
Input LOW; G_2;G_3; G_4; G_5	$-I_{GL}$	–	0.8	1.5 mA	13.5	V_{GL} = 1.7 V; other inputs 13.5V
G_1; G_6	$-I_{GL}$	–	1.6	3.0 mA		
Output HIGH	I_{QH}	–	–	40 µA	11.4	V_{QH} = 13.5 V; V_{GH} = 4.5 V
Output LOW	I_{QL}	20	–	– mA	11.4	V_{QL} = 0.4 V; V_{GH} = 7.5 V
SUPPLY DATA						
Currents (per gate)						
at V_{QH}	I_P	–	2.5	4.5 mA	13.5	V_G = 0 V
at V_{QL}	I_P	–	4.0	6.0 mA	13.5	V_G = 13.5 V
DYNAMIC DATA						
Times						
Propagation delay						
fall time: V_Q = 12 V	t_{pdf1}	–	100	250 ns		R_L =390 Ω;N_a = 1; T_{amb} = 25 °C
V_Q = 5 V	t_{pdf2}	–	90	250 ns		
rise time: V_Q = 12 V	t_{pdr1}	–	130	300 ns		R_L =3.9kΩ;N_a= 1; T_{amb} = 25 °C
V_Q = 5 V	t_{pdr2}	–	120	300 ns		

1) All typ. values under test conditions: T_{amb} = 25 °C and V_P = 12 V

CHARACTERISTICS

Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to 70 °C

	Symbol	min.	typ. [1]	max.		Conditions and references: V_P (V)	
STATIC DATA							
Input HIGH	V_{GH}	7.5	–	–	V	13.5	V_{QL} = 0.4 V; I_{QL} = 20 mA
Input LOW	V_{GL}	–	–	4.5	V	13.5	V_{QH} = 17 V; I_{QH} = 40 µA
Output LOW	V_{QL}	–	–	0.4	V	13.5	V_{GH} = 7.5 V; I_{QL} = 20 mA
D.C. noise margin: HIGH	M_H	4.5	8.0	–	V	13.5	
LOW	M_L	2.8	5.0	–	V	13.5	
Currents (per gate)							
Input HIGH: G_2;G_3;G_4;G_5	I_{GH}	–	–	1.0	µA	17	V_{GH} = 17 V; other inputs 0 V
G_1;G_6	I_{GH}	–	–	2.0	µA		
Input LOW: G_2;G_3;G_4;G_5	$-I_{GL}$	–	1.0	1.8	mA	17	V_{GL} = 1.7 V; other inputs 17V
G_1;G_6	$-I_{GL}$	–	2.0	3.6	mA		
Output HIGH	I_{QH}	–	–	40	µA	13.5	V_{QH} = 17 V; V_{GL} = 4.5 V
Output LOW	I_{QL}	20	–	–	mA	13.5	V_{QL} = 0.4 V; V_{GL} = 7.5 V
SUPPLY DATA							
Currents (per gate)							
at V_{QH}	I_P	–	2.8	4.5	mA	17	V_G = 0 V
at V_{QL}	I_P	–	4.5	7.0	mA	17	V_G = 17 V

[1]) All typ. values under test conditions: T_{amb} = 25 °C and V_P = 15 V.

CHARACTERISTICS (continued)

Calculation of collector resistor R_A

The collector resistor R_A has to be calculated out of voltages and input- and output currents of the gates.

$$R_{Amax} = \frac{V_P - V_{QH} \quad (V)}{n \cdot I_{QH} + N \cdot I_{GH} \quad (\mu A)} \qquad R_{Amin} = \frac{V_P - V_{QL} \quad (V)}{I_{QLmax} - N \cdot I_{GL} \quad (mA)}$$

n = number of AND combinations
N = number of used inputs
V_P = supply voltage of TTL-inputs
V_{QH} = output voltage HIGH of TTL-circuit
V_{QL} = output voltage LOW of TTL-circuit
I_{GH} = input current HIGH of TTL-circuit
I_{GL} = input current LOW of TTL-circuit

for interfacing HNIL to TTL:

$$R_{Amax} = \frac{5 - 2.4 \quad (V)}{n \cdot 40 + N \cdot 40 \ (\mu A)} \qquad R_{Amin} = \frac{5 - 0.4 \quad (V)}{20 - N \cdot 1.6 \quad (mA)}$$

of which $n_{max} = 2$ at $N_{max} = 10$

If FZH161 is used as wired-AND combination

for range I: $V_P = 12$ V

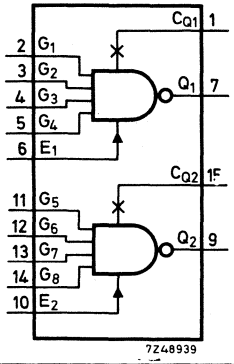
$$R_{Amax} = \frac{12 - 10 \quad (V)}{n \cdot 40 + N \cdot 1 \ (\mu A)} \qquad R_{Amin} = \frac{12 - 0.4 \quad (V)}{20 - N \cdot 1.5 \quad (mA)}$$

for range II: $V_P = 15$ V

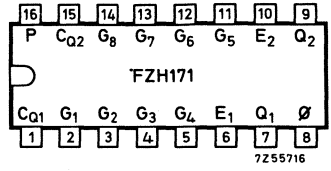
$$R_{Amax} = \frac{15 - 12 \quad (V)}{n \cdot 40 + N \cdot 1 \ (\mu A)} \qquad R_{Amin} = \frac{15 - 0.4 \quad (V)}{20 - N \cdot 1.8 \quad (mA)}$$

of which $n_{max} = 9$ at $N_{max} = 10$

The FZ family of HNIL silicon monolithic integrated circuits has been designed for high noise immunity low speed digital applications in industrial control and computer periphery equipment.



DUAL 4-INPUT NAND GATE with slow-down capability and expandable inputs

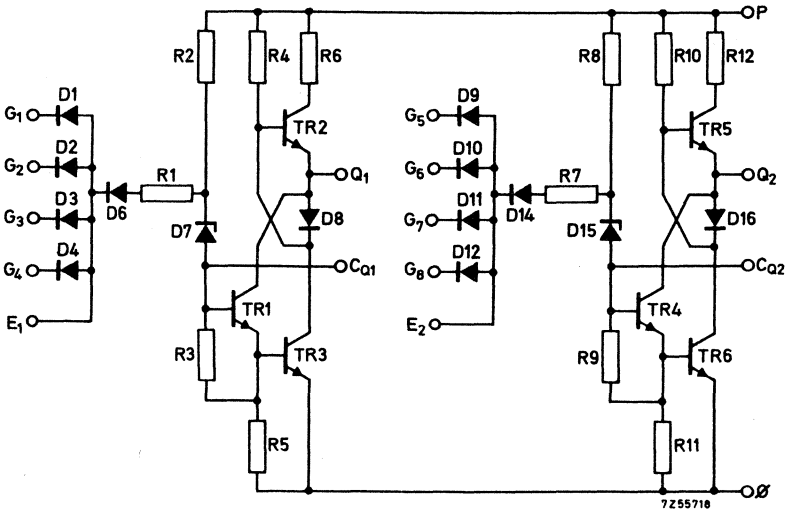


QUICK REFERENCE DATA				
Supply voltage (range I)	V_P	12	$+12\frac{1}{2}$ % -5 %	V
(range II)	V_P	15	$+13$ % -10 %	V
Operating ambient temperature	T_{amb}	0 to +70		°C
Average propagation delay time ($N = 1$; $C_L = 10$ pF; $T_{amb} = 25$ °C; $V_{pd} = 4.5$ V	t_{pd}	typ.	170	ns
Available d.c. fan-out LOW state	N_{aL}	max.	10	
$T_{amb} = 0$ to +70 °C HIGH state	N_{aH}	max.	100	
D.C. noise margin at T_{amb} = 25 °C				
range I: V_P = 12 V	$M_L = M_H$	typ.	5	V
range II: V_P = 15 V	M_L	typ.	5	V
	M_H	typ.	8	V
Power consumption per gate at T_{amb} = 25 °C (50% duty cycle) range I : V_P = 12 V	P_{av}	typ.	16	mW
range II: V_P = 15 V	P_{av}	typ.	27	mW

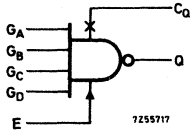
The FZH171 consists of two independent NAND gates and each gate has a special terminal (C_Q). It is possible to connect a capacitor between the output (Q) and the corresponding slow-down terminal C_Q to increase the propagation delay time.
The expandable inputs (E_1 and E_2) are floating.

PACKAGE OUTLINE 16 lead plastic dual in-line (type B) (See General Section).

CIRCUIT DIAGRAM



LOGIC FUNCTION



$$Q = \overline{G_A \cdot G_B \cdot G_C \cdot G_D \cdot E}\ ^{*})$$

(positive logic)

*) When provided with a diode

G_A	G_B	G_C	G_D	Q
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

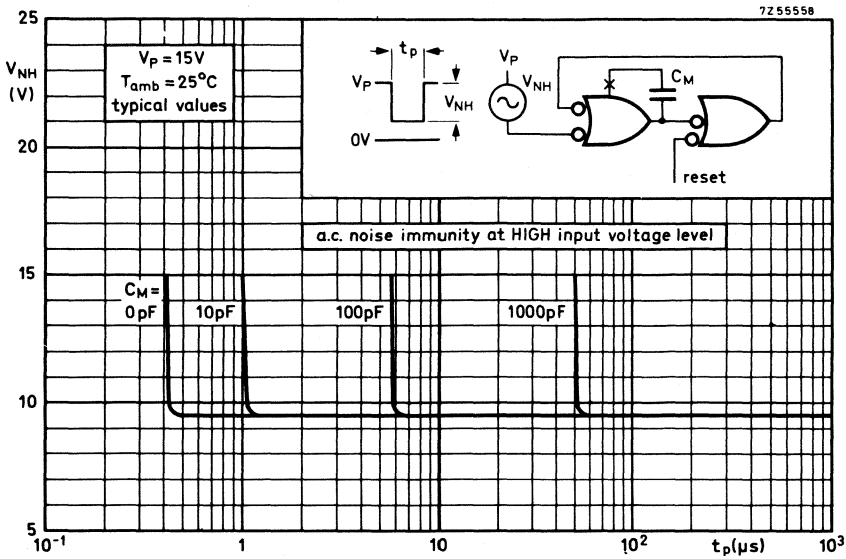
RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18	V
Output voltage	V_Q	max.	12	V
Input voltage	V_G	max.	18	V
Input current at V_P = 17 V; $-V_{Gtyp}$ = 5 V	$-I_{GL}$	max.	25	mA
Voltage difference between any two inputs		max.	18	V
Storage temperature	T_{stg}	−65	to +150	°C
Operating ambient temperature	T_{amb}	0	to + 70	°C
Output short circuit duration duty cycle 10 %	t_{Qsc}	max.	2	s
Slow-down input voltage	$+V_{CQ}$	max.	0.6	V
	$-V_{CQ}$	max.	1.0	V
Slow-down input current	$+I_{CQ}$	max.	2.0	mA
	$-I_{CQ}$	max.	10.0	mA
Expandable input voltage	V_E	min.	0	V
Expandable input current	I_E	max.	25	mA

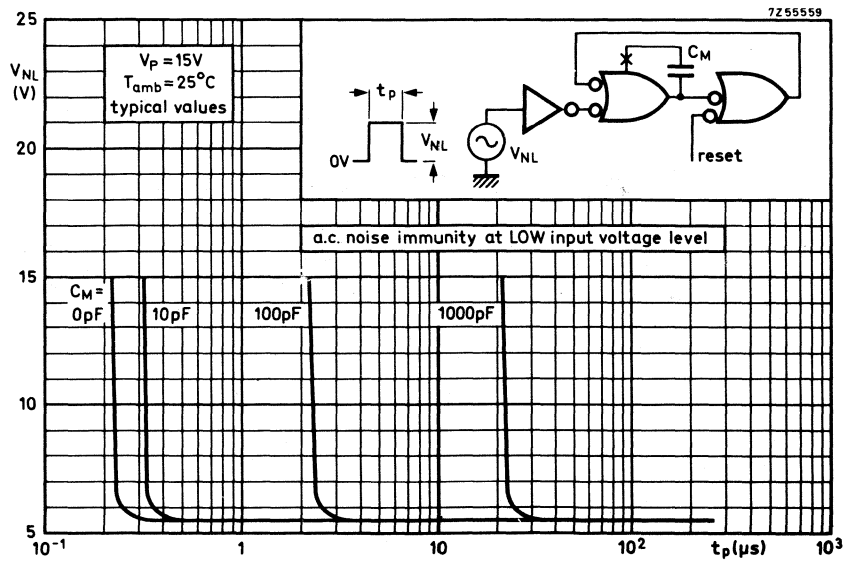
SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to	+70	°C
Uniform system supply voltage (range I)	V_P	11.4 to	13.5	V
(range II)	V_P	13.5 to	17	V
Available d.c. fan-out	N_{aL}	max.	10	
	N_{aH}	max.	100	
D.C. noise margin; range I at V_{Pmin}	M_L	min.	2.8	V
	M_H	min.	2.5	V
range II at V_{Pmin}	M_L	min.	2.8	V
	M_H	min.	4.5	V
Supply current at range I; output HIGH	I_{Pav}	typ.	0.9	mA
output LOW	I_{Pav}	typ.	1.7	mA
at range II; output HIGH	I_{Pav}	typ.	1.2	mA
output LOW	I_{Pav}	typ.	2.3	mA
Power consumption per gate (50% duty cycle) at range I; V_{Pmax}	P_{tot}	max.	28	mW
at range II; V_{Pmax}	P_{tot}	max.	46	mW
Thermal resistance from system to ambient	R_{th}	max.	150	°C/W

SYSTEM DESIGN DATA (continued)



Typical curves for HIGH-input voltage level



Typical curves for LOW-input voltage level

CHARACTERISTICS Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Sym-bol	min.	typ.[1]	max.		Conditions and references	
						V_P (V)	
STATIC DATA							
Voltages							
Input HIGH	V_{GH}	7.5	–	–	V	11.4	$V_{QL} \leq 1.7$ V; I_{QL} = 15 mA
Input LOW	V_{GL}	–	–	4.5	V	11.4 and 13.5	$V_{QH} \geq 10$ V; $-I_{QH}$ = 0.1 mA
Output HIGH	V_{QH}	10.0	11.3	–	V	11.4 and 13.5	V_{GL} = 4.5 V; $-I_{QH}$ = 0.1 mA
Output LOW	V_{QL}	–	0.9	1.7	V	11.4	V_{GH} = 7.5 V; I_{QL} = 15 mA
D.C. noise margin: HIGH	M_H	2.5	5.0	–	V	11.4	
LOW	M_L	2.8	5.0	–	V	11.4	
Currents (per gate)							
Input HIGH	I_{GH}	–	–	1.0	µA	13.5	V_{GH} = 13.5 V; other inputs 0 V
Input LOW	$-I_{GL}$	–	0.8	1.5	mA	13.5	V_{GL} = 1.7 V; other inputs 13.5 V
Output HIGH	$-I_{QH}$	0.1	–	–	mA	11.4 and 13.5	V_{GL} = 4.5 V; V_{QH} = 10 V
Output LOW	I_{QL}	15	–	–	mA	11.4	V_{GH} = 7.5 V; V_{QL} = 1.7 V
Output short circuited [2]	$-I_{Qsc}$	10	30	50	mA	13.5	V_G = 0 V; V_Q = 0 V
SUPPLY DATA							
Currents (per gate)							
at V_{QH}	I_P	–	0.9	1.6	mA	13.5	V_G = 0 V
at V_{QL}	I_P	–	1.7	3.0	mA	13.5	V_G = 13.5 V
DYNAMIC DATA							
Times:							
Propagation delay							
fall time	t_{pdf}	90	175	310	ns	12	C_L = 10 pF; N = 1; T_{amb} = 25 °C; V_{pd} = 4.5 V
rise time	t_{pdr}	90	175	310	ns	12	
output rise time	t_r	200	340	570	ns	12	
output fall time	t_f	70	120	210	ns	12	

[1]) All typ. values under test conditions: T_{amb} = 25 °C and V_P = 12 V

[2]) Non-repetitive short circuit duration max. 2 s (duty cycle 10 %)

CHARACTERISTICS Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

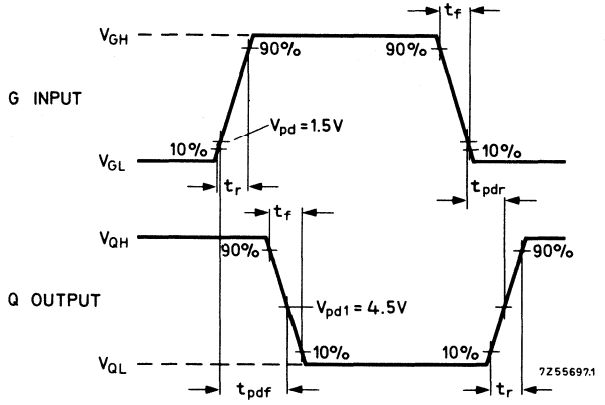
	Symbol	min.	typ.[1]	max.		Conditions and references: V_P (V)	Conditions and references
STATIC DATA							
Voltages							
Input HIGH	V_{GH}	7.5	–	–	V	13.5	$V_{QL} \leq 1.7$ V; I_{QL} = 18 mA
Input LOW	V_{GL}	–	–	4.5	V	13.5 and 17	$V_{QH} \geq 12$ V; $-I_{QH}$ = 0.1 mA
Output HIGH	V_{QH}	12.0	14.3	–	V	13.5 and 17	V_{GL} = 4.5 V; $-I_{QH}$ = 0.1 mA
Output LOW	V_{QL}	–	1.0	1.7	V	13.5	V_{GH} = 7.5 V; I_{QL} = 18 mA
D.C. noise margin: HIGH	M_H	4.5	8.0	–	V	13.5	
LOW	M_L	2.8	5.0	–	V	13.5	
Currents (per gate)							
Input HIGH	I_{GH}	–	–	1.0	µA	17	V_{GH} = 17 V; other inputs 0 V
Input LOW	$-I_{GL}$	–	1.0	1.8	mA	17	V_{GL} = 1.7 V; other inputs 17 V
Output HIGH	$-I_{QH}$	0.1	–	–	mA	13.5 and 17	V_{GL} = 4.5 V; V_{QH} = 12 V
Output LOW	I_{QL}	18	–	–	mA	13.5	V_{GH} = 7.5 V; V_{QL} = 1.7 V
Output short circuited [2]	$-I_{Qsc}$	15	37	60	mA	17	V_G = 0 V; V_Q = 0 V
SUPPLY DATA							
Currents (per gate)							
at V_{QH}	I_P	–	1.2	2.1	mA	17	V_G = 0 V
at V_{QL}	I_P	–	2.3	4.0	mA	17	V_G = 17 V
DYNAMIC DATA							
Times:							
Propagation delay							
fall time	t_{pdf}	–	140	–	ns	15	C_L = 10 pF; N = 1; T_{amb} = 25 °C; V_{pd} = 4.5 V
rise time	t_{pdr}	–	195	–	ns	15	
output rise time	t_r	–	410	–	ns	15	
output fall time	t_f	–	75	–	ns	15	

[1] All typical values under test conditions: T_{amb} = 25 °C and V_P = 15 V

[2] Non-repetitive short circuit duration max. 2 s (duty cycle 10 %)

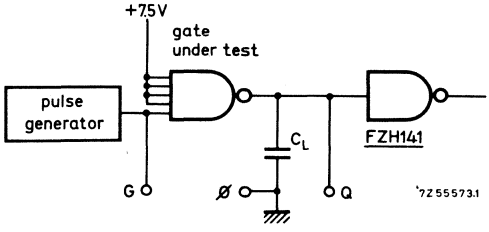
CHARACTERISTICS (continued)

DYNAMIC DATA



Pulse generator (G-input): t_r = 350 ns
t_f = 120 ns
t_{GH} = 1 µs

V_{pd} = +4.5 V

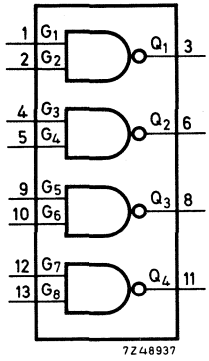


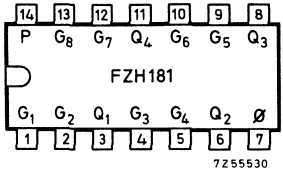
Measuring conditions: V_P = + 12 V; + 15 V
C_L = 10 pF (including probe and jig capacitance)
T_{amb} = 25 °C
Slow-down terminals are not connected

Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf}

The FZ family of HNIL silicon monolithic integrated circuits has been designed for high noise immunity low speed digital applications in industrial control and computer periphery equipment.

LEVEL CONVERTER TTL-HNIL



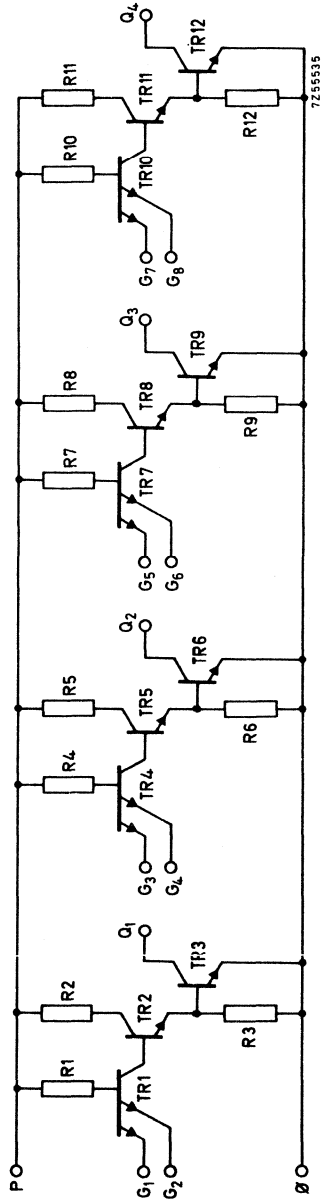


QUICK REFERENCE DATA				
Supply voltage	V_P		5+5%	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Available d.c. fan-out (T_{amb} = 0 to +70 °C) LOW state	N_{aL}	max.	27	
Available d.c. fan-out (T_{amb} = 0 to +70 °C) HIGH state	N_{aH}	max.	100	
Power consumption per gate at T_{amb} = 25 °C (50% duty cycle)	P_{av}	typ.	24	mW

The FZH181 is a level converter with open collector output for interfacing TTL to HNIL and consists of 4 gates.

PACKAGE OUTLINE 14 lead plastic dual in-line (type B) (See General Section).

CIRCUIT DIAGRAM



LOGIC FUNCTION

$Q = \overline{G_A \cdot G_B}$

(for positive logic)

Function table

G_A	G_B	Q
L	X	H
X	L	H
H	H	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is inmaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	7	V
Output voltage	V_Q	max.	18	V
Input voltage	V_G	max.	5.5	V
Input current ($-V_{Gmax} = 0.5$ V; $V_P = 5$ V; $T_{amb} = 70\ ^oC$)	$-I_{GL}$	max.	25	mA
Voltage difference between any two inputs		max.	5.5	V
Storage temperature	T_{stg}	−65 to	+150	^oC
Operating ambient temperature	T_{amb}	0 to	+70	^oC

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to +70		°C
Uniform system supply voltage	V_P	4.75 to 5.25		V
Available d.c. fan-out	N_a	max.	27	
D.C. noise margin	M	min.	0.4	V
Supply current per gate; output HIGH (V_P = 5 V; V_G = 0)	I_{Pav}	max.	2.0	mA
output LOW (V_P = 5 V; V_G = 0)	I_{Pav}	max.	12.0	mA
Power consumption per gate at V_{Pmax} (50% duty cycle)	P_{tot}	typ.	24	mW
Thermal resistance from system to ambient	R_{th}	max.	150	°C/W

CHARACTERISTICS

Test conditions: V_P = 5 V; T_{amb} = 0 to +70 °C

	Symbol	min.	typ. [1]	max.	Conditions and references: V_P (V)	Conditions and references:
STATIC DATA						
Voltages						
Input HIGH	V_{GH}	2.0	–	– V	4.75	V_{QL} = 1.0 V; I_{QL} = 50 mA
Input LOW	V_{GL}	–	–	0.8 V	4.75	V_{QH} = 18.0 V; I_{QH} = 250 µA
Output LOW	V_{QL}	–	–	0.4 V	4.75	V_{GH} = 2 V; I_{QL} = 16 mA
	V_{QL}	–	–	1.0 V	4,75	V_{GH} = 2 V; I_{QL} = 50 mA
D.C. noise margin: HIGH	M_H	0.4	–	– V		
LOW	M_L	0.4	–	– V		
Currents (per gate)						
Input HIGH	I_{GH}	–	–	40 µA	5.25	V_{GH} = 2.4 V
Input LOW	$-I_{GL}$	–	–	1.6 mA	5.25	V_{GL} = 0.4 V
Output HIGH	I_{QH}	–	–	250 µA	4.75	V_{QH} = 18 V; V_{GL} = 0.8 V
Output LOW	I_{QL}	50	–	– mA	4.75	V_{GH} = 2 V; V_{QL} = 1.0 V
SUPPLY DATA						
Currents (per gate)						
at V_{QH}	I_P	–	1.0	2.0 mA	5	V_{GH} = 0 V
at V_{QL}	I_P	–	8.5	12.0 mA	5	V_{GL} = 5 V
DYNAMIC DATA						
Times:						
Propagation						
fall time	t_{pdf}	–	20	60 ns	12	V_Q = 12 V; R_L = 390 Ω
rise time	t_{pdr}	–	130	300 ns	12	V_Q = 12 V; R_L = 3.9 kΩ

1) All typ. values under test conditions: T_{amb} = 25 °C and V_P = 12 V.

CHARACTERISTICS (continued)

Calculation of collector resistor R_A

The collector resistor R_A has to be calculated out of voltages and input- and output currents of the gates.

$$R_{Amax} = \frac{V_P - V_{QH} \quad (V)}{n \cdot I_{QH} + N \cdot I_{GH} \quad (\mu A)} \qquad R_{Amin} = \frac{V_P - V_{QL} \quad (V)}{I_{QLmax} - N \cdot I_{GL} \quad (mA)}$$

n = number of AND combinations
N = number of used inputs
V_P = supply voltage of HNIL inputs
V_{QH} = output voltage HIGH of HNIL-circuit
V_{QL} = output voltage LOW of HNIL-circuit
I_{GH} = input current HIGH of HNIL-circuit
I_{GL} = input current LOW of HNIL-circuit

for interfacing TTL to HNIL (range I; V_P = 12 V)

$$R_{Amax} = \frac{12 - 10 \quad (V)}{n \cdot 250 + N \cdot 1 \quad (\mu A)} \qquad R_{Amin} = \frac{12 - 1.0 \quad (V)}{50 - N \cdot 1.5 \quad (mA)}$$

for interfacing TTL to HNIL (range II; V_P = 15 V)

$$R_{Amax} = \frac{15 - 12 \quad (V)}{n \cdot 250 - N \cdot 1 \ (\mu A)} \qquad R_{Amin} = \frac{15 - 1.0 \quad (V)}{50 - N \cdot 1.8 \quad (mA)}$$

of which n_{max} = 4 at N_{max} = 25

If FZH181 is used as wired-AND combination

HIGH state

$$R_{Amax} = \frac{V_P - 2.4 \quad (V)}{n \cdot 250 - N \cdot 40 \ (\mu A)}$$

LOW state

$$R_{Amin} = \frac{V_P - 0.4 \quad (V)}{16 - N \cdot 1.6 \quad (mA)}$$

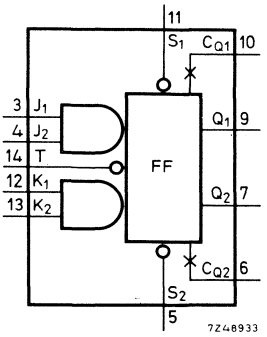
of which n = number of FZH181 AND combinations

N = number of used inputs

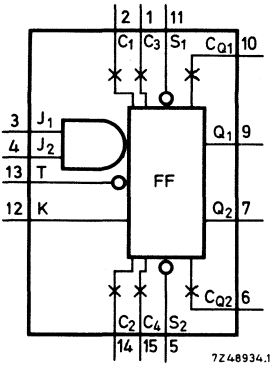
The FZ family of HNIL silicon monolithic integrated circuits has been designed for high noise immunity low speed digital applications in industrial control and computer periphery equipment.

FZJ101: SINGLE JK MASTER SLAVE FLIP-FLOP with slow-down capability on the slave

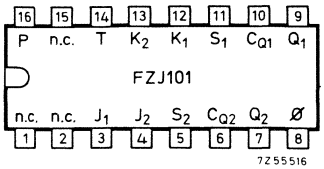
FZJ111: SINGLE JK MASTER SLAVE FLIP-FLOP with slow-down capability on master and slave

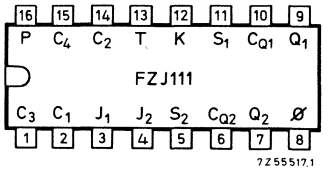


FZJ101



FZJ111



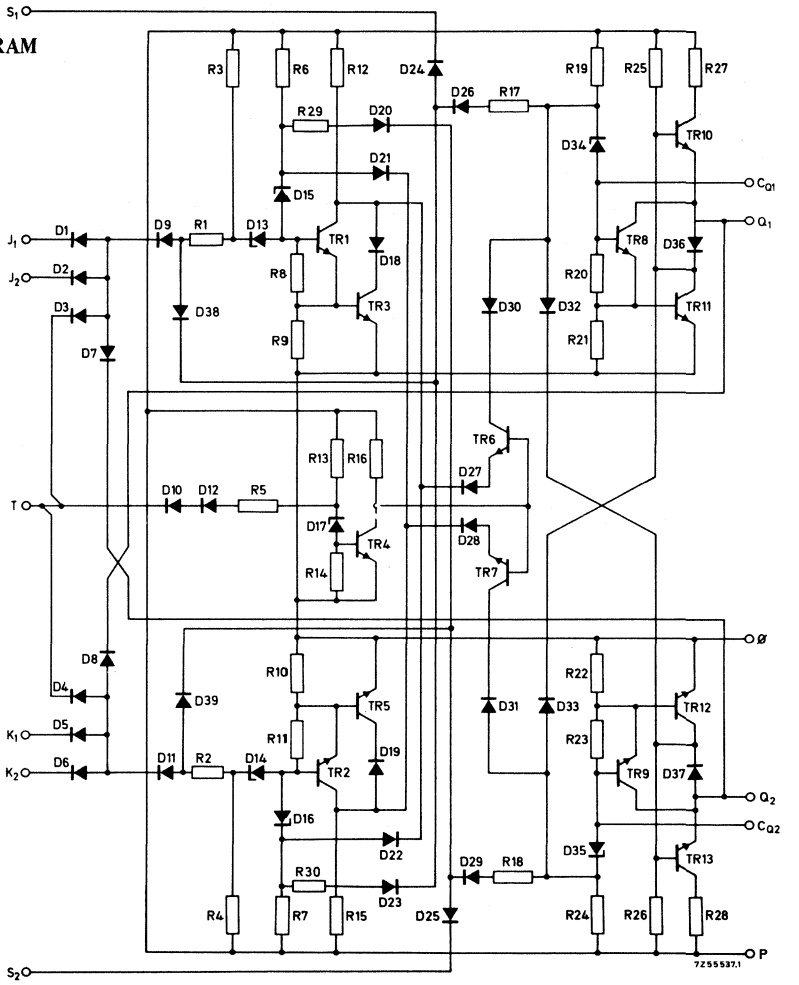


QUICK REFERENCE DATA			
Supply voltage (range I)	V_P	12 $^{+12\frac{1}{2}\%}_{-5\%}$	V
(range II)	V_P	15 $^{+13\%}_{-10\%}$	V
Operating ambient temperature	T_{amb}	0 to +70	°C
Available d.c. fan-out LOW state	N_{aL}	max. 10	
(T_{amb} = 0 to +70 °C) HIGH state	N_{aH}	max. 100	
Maximum operating frequency at T_{amb} = 25 °C			
duty cycle 50%: range I : V_P = 12 V	f_c	max. 0.5	MHz
range II: V_P = 15 V	f_c	max. 0.5	MHz
Average supply current at T_{amb} = 25 °C			
V_P = 13.5 V	I_{Pav}	typ. 8	mA
V_P = 17 V	I_{Pav}	typ. 11	mA
D.C. noise margin at T_{amb} = 25 °C			
range I: V_P = 12 V	$M_L = M_H$	typ. 5	V
range II: V_P = 15 V	M_L	typ. 5	V
	M_H	typ. 8	V

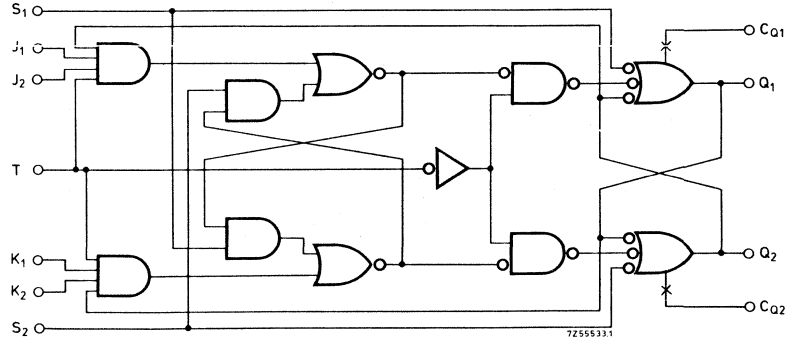
PACKAGE OUTLINE 16-lead plastic dual in-line (type B) (See General Section).

CIRCUIT DIAGRAM

FZJ101

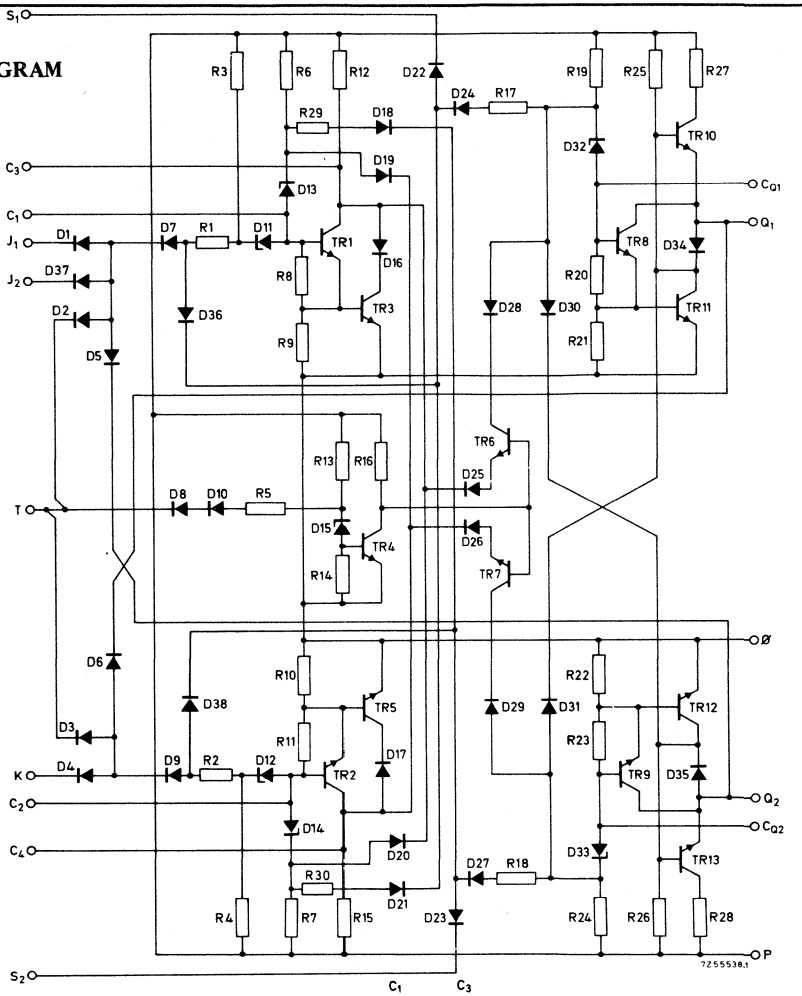


LOGIC DIAGRAM

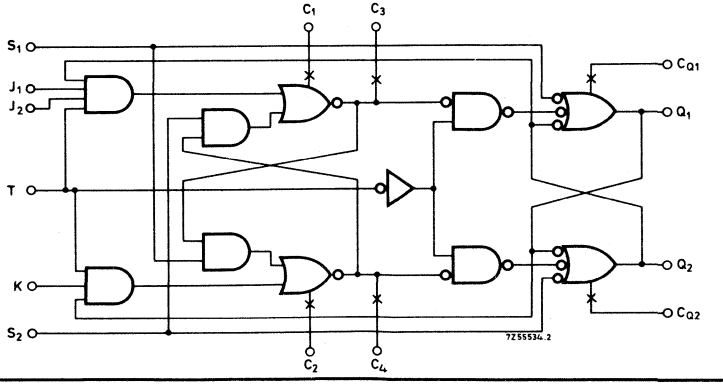


CIRCUIT DIAGRAM

FZJ111



LOGIC DIAGRAM



The FZJ101 consists of a single JK master slave flip-flop with two J and K inputs. This type has also a slow-down capability on the slave of the flip-flop, due to which the propagation delay of the slave being the reaction of the slave on the negative going clock-edge, can increase. This can be achieved by connecting external capacitors between the output terminals and their associated slow down terminals. The FZJ111 consists of a single JK master slave flip-flop with 2 J inputs and one K input. This type has both a slow down capability on the master and the slave of the flip-flop. For slowing down the slave see FZJ101.

The propagation delay of the master, being the reaction of the master to the positive going clock-edge can be increased by connecting external capacitors between the slow down terminals C_1, C_3 and C_2, C_4 respectively.

LOGIC FUNCTIONS

FZJ101: $J = J_1 \cdot J_2$
$K = K_1 \cdot K_2$

FZJ111: $J = J_1 \cdot J_2$
$K = K$

Function tables

t_n		t_{n+1}	
J	K	Q_1	Q_2
L	L	Q_{1n}	Q_{2n}
L	H	L	H
H	L	H	L
H	H	Q_{2n}	Q_{1n}
Q_2 is opposite Q_1			

The set inputs S_1 and S_2 override all the other inputs.

S_1	S_2	Q_1	Q_2
L	H	H	L
H	L	L	H
H	H	Q_1	Q_2 1)
L	L	H	H 2)

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

1) Q_2 is opposite Q_1
2) If S_1 and S_2 return to HIGH simultaneously the Q - states will be indeterminate.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18 V
Output voltage	V_Q	max.	12 V
Input voltage	V_J, V_K, V_T	max.	18 V
Input current at V_P = 17 V; $-V_{Ityp}$ = 5 V	$-I_{IL}$	max.	25 mA [1]
Storage temperature	T_{stg}	−65 to +150	°C
Operating ambient temperature	T_{amb}	0 to +70	°C

1) All inputs except slow-down inputs.

NOTE
The slow-down terminals indicated by crosses are for slow-down purposes only; they are not to be connected to any other terminal.

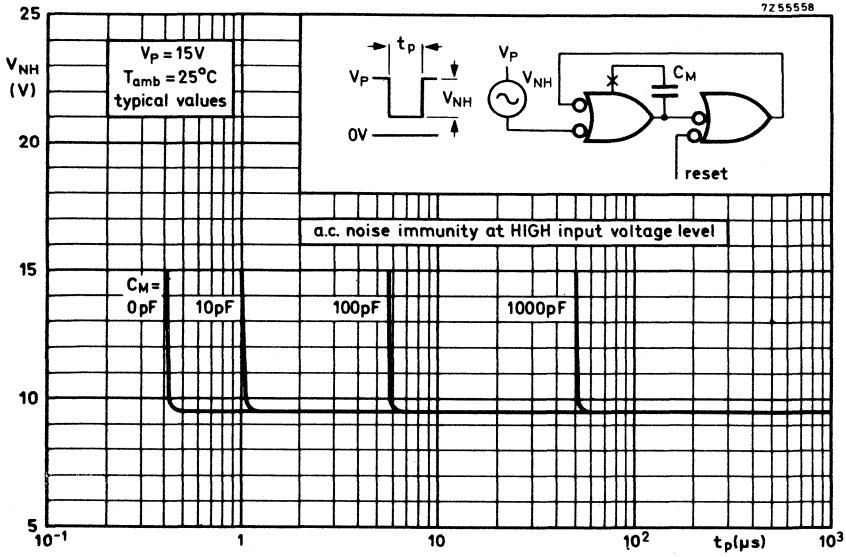
RATINGS (continued)

Output short circuit duration duty cycle 10%	t_{Qsc}	max.	2	s
Slow-down input voltage	$+V_{CQ}$	max.	0.6	V
	$-V_{CQ}$	max.	1.0	V
Slow-down input current	$+I_{CQ}$	max.	2.0	V
	$-I_{CQ}$	max.	10.0	V

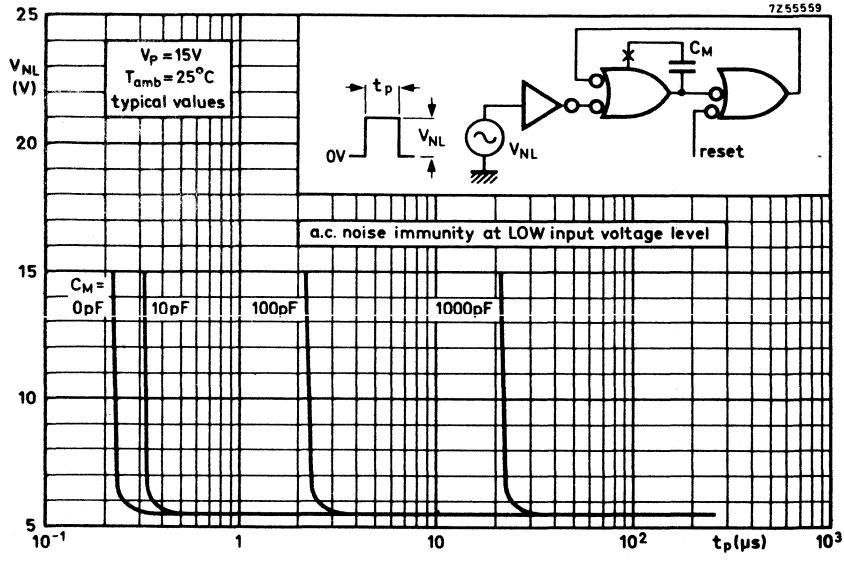
SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to	+70	°C
Uniform system supply voltage (range I)	V_P	11.4 to	13.5	V
(range II)	V_P	13.5 to	17	V
Available d.c. fan-out	N_{aL}	max.	10	
D.C. noise margin to all inputs: range I at V_{Pmin}	M_L	min.	2.8	V
	M_H	min.	2.5	V
range II at V_{Pmin}	M_L	min.	2.8	V
	M_H	min.	4.5	V
Average propagation delay time at V_{pd} = 4.5 V				
T→Q : at range I; V_P = 12 V	t_{pd}	max.	645	ns
at range II; V_P = 15 V	t_{pd}	typ.	400	ns
S→Q : at range I; V_P = 12 V	t_{pd}	max.	455	ns
at range II; V_P = 15 V	t_{pd}	typ.	265	ns
Maximum clock rate at T_{amb} = 25 °C				
duty cycle 50%; range I : V_P = 12 V	f_c	typ.	0.5	MHz
range II : V_P = 15 V	f_c	typ.	0.5	MHz
Supply current at range I : V_P = 12 V	I_P	typ.	8	mA
range II : V_P = 15 V	I_P	typ.	11	mA
Thermal resistance from system to ambient	R_{th}	max.	150	°C/W

SYSTEM DESIGN DATA (continued)



Typical curves for HIGH-input voltage level



Typical curves for LOW-input voltage level

CHARACTERISTICS Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Symbol	min.	typ.[1]	max.	Conditions and references: V_P (V)	Conditions and references
STATIC DATA						
Voltages						
Input HIGH: J, K, T, S	V_{IH}	7.5	–	– V	11.4	$V_{QL} \leq 1.7$ V; I_{QL} = 15 mA
Input LOW: J, K, S	V_{IL}	–	–	4.5 V	11.4 and 13.5	$V_{QH} \geq 10$ V; $-I_{QH} = 0.1$ mA
T	V_{TL}	–	–	4.0 V		
Output HIGH	V_{QH}	10	11.3	– V	11.4 and 13.5	V_{IL} = 4.5 V; $-I_{QH} = 0.1$ mA
Output LOW	V_{QL}	–	0.9	1.7 V	11.4	V_{IH} = 7.5 V; I_{QL} = 15 mA
D.C. noise margin: HIGH	M_H	2.5	5.0	– V	11.4	
LOW	M_L	2.8	5.0	– V	11.4	
Currents						
Input HIGH: J, K, S	I_{IH}	–	–	1 µA	13.5	V_{IH} = 13.5 V (other inputs 0V)
T	I_{TH}	–	–	3 µA		
Input LOW: J, K	$-I_{IL}$	–	0.8	1.5 mA	13.5	$V_{JL} = V_{KL} = 1.7$V
T	$-I_{TL}$	–	1.6	3.0 mA	13.5	V_{TL} = 1.7 V
S[2]	$-I_{SL}$	–	0.8	1.5 mA	13.5	V_{SL} = 1.7 V
Output HIGH	$-I_{QH}$	0.1	–	– mA	11.4 and 13.5	V_{QH} = 10 V
Output LOW	I_{QL}	15	–	– mA	11.4	V_{QL} = 1.7 V
Output short circuited[3]	$-I_{Qsc}$	10	30	50 mA	13.5	V_I=0V; V_Q=0V
SUPPLY DATA						
Supply current	I_P	–	8.0	– mA	13.5	

1) All typ. values under test conditions: T_{amb} = 25 °C and V_P = 12 V.
2) For dynamic: $-I_{SL}$ = 1.5 x specified values.
3) Non-repetitive output short circuited duration max. 2 s (duty cycle 10%).

CHARACTERISTICS (continued)

Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Sym-bol	min.	typ. [1]	max.		Conditions and references	
						V_P (V)	
DYNAMIC DATA							
Times							
Propagation delay:							
T → Q							
fall time	t_{pdf}	270	450	770	ns	12	
rise time	t_{pdr}	160	290	520	ns	12	
S → Q							
fall time	t_{pdf}	180	330	580	ns	12	
rise time	t_{pdr}	70	165	330	ns	12	
output rise time	t_r	200	340	570	ns	12	
output fall time	t_f	70	120	210	ns	12	C_L = 10 pF
Clock rate							N = 1
(duty cycle 50%)	f_c	0.2	0.5	–	MHz	12	T_{amb} = 25 °C
Input times							V_{pd} = 4.5 V
T input	t_{TH}	0.6	–	–	µs	12	
	t_{TL}	0.6	–	–	µs	12	
S input	t_{SH}	1.0	–	–	µs	12	
Hold time	t_{hold}	0	–	–	ns	12	
Input preparation time	t_{prep}	0	–	–	ns	12	
T input slope [2]	$(-dt/dV)_{Tmax}$			1	µs/V	12	

[1] All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V.

[2] For shift register applications $(-dt/dV)_{Tmax}$ = 0.1 µs/V.

CHARACTERISTICS (continued)

Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

	Sym-bol	min.	typ. [1]	max.		Conditions and references: V_P (V)	Conditions and references
STATIC DATA							
Voltages							
Input HIGH: J, K, T, S	V_{IH}	7.5	–	–	V	13.5	$V_{QL} \leq 1.7$ V; I_{QL} = 18 mA
Input LOW: J, K, S	V_{IL}	–	–	4.5	V	13.5 and 17	$V_{QH} \leq 12$ V; $-I_{QH}$ = 0.1 mA
T	V_{TL}	–	–	4.0	V		
Output HIGH	V_{QH}	12	14.3	–	V	13.5 and 17	V_{IL} = 4.5 V; $-I_{QH}$ = 0.1 mA
Output LOW	V_{QL}	–	1.0	1.7	V	13.5	V_{IH} = 7.5 V; I_{QL} = 18 mA
D.C. noise margin: HIGH	M_H	4.5	8.0	–	V	13.5	
LOW	M_L	2.8	5.0	–	V	13.5	
Currents							
Input HIGH: J, K, S	I_{IH}	–	–	1.0	μA	17	V_{IH} = 17 V; (other inputs 0 V)
T	I_{TH}	–	–	3.0	μA		
Input LOW: J, K	$-I_{IL}$	–	1.0	1.8	mA	17	$V_{JL} = V_{KL}$ = 1.7 V
T	$-I_{TL}$	–	2.0	3.6	mA	17	V_{TL} = 1.7 V
S [2]	$-I_{SL}$	–	1.0	1.8	mA	17	V_{SL} = 1.7 V
Output HIGH	$-I_{QH}$	0.1	–	–	mA	13.5 and 17	V_{QH} = 12 V
Output LOW	I_{QL}	18	–	–	mA	13.5	V_{QL} = 1.7 V
Output short circuited	$-I_{Qsc}$ [3]	15	37	60	mA	17	V_I = 0 V; V_Q = 0 V
SUPPLY DATA							
Supply current	I_P	–	11	–	mA	17	

1) All typ. values under test conditions: T_{amb} = 25 °C and V_P = 15 V
2) For dynamic: $-I_{SL}$ = 1.5 x specified values
3) Non-repetitive short circuit duration max. 2 s (duty cycle 10%)

CHARACTERISTICS (continued)

Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

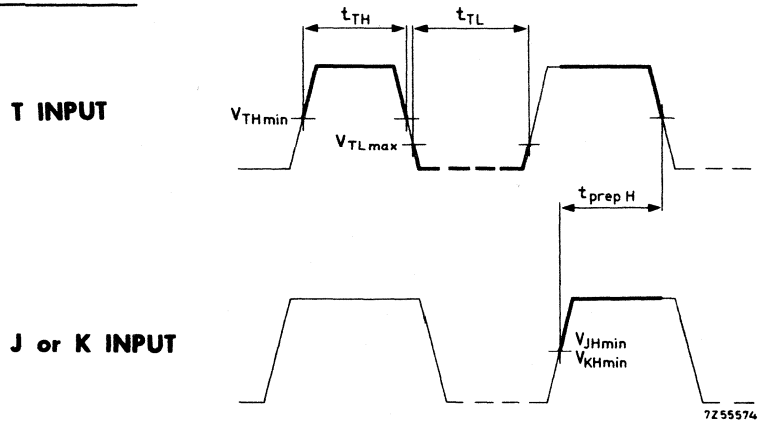
	Sym-bol	min.	typ. [1]	max.		Conditions and references	
						V_P (V)	
DYNAMIC DATA							
Times							
Propagation delay:							
T→Q							
fall time	t_{pdf}	–	470	–	ns	15	
rise time	t_{pdr}	–	330	–	ns	15	
S→Q							
fall time	t_{pdf}	–	340	–	ns	15	
rise time	t_{pdr}	–	195	–	ns	15	
output rise time	t_r	–	410	–	ns	15	
output fall time	t_f	–	75	–	ns	15	C_L = 10 pF
Clock rate							N = 1
(duty cycle 50%)	f_c	–	0.5	–	MHz	15	T_{amb} = 25 °C
Input times							V_{pd} = 4.5 V
T input	t_{TH}	0.6	–	–	µs	15	
	t_{TL}	0.6	–	–	µs	15	
S input	t_{SH}	1.0	–	–	µs	15	
Hold time	t_{hold}	0	–	–	µs	15	
Input preparation time	t_{prep}	0	–	–	µs	15	
T input slope [2]	$(-dt/dV)_{Tmax}$			1	µs/V	15	

[1] All typical values under test conditions: T_{amb} = 25 °C and V_P = 15 V.

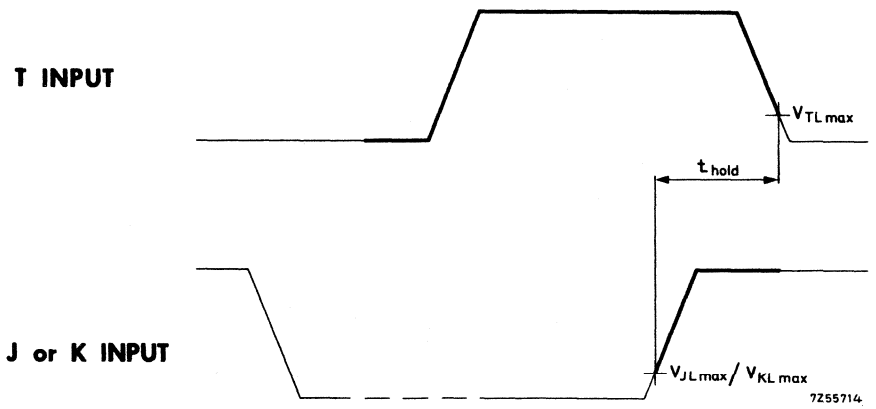
[2] For shift register applications $(-dt/dV)_{Tmax}$ = 0.1 µs/V.

CHARACTERISTICS (continued)

DYNAMIC DATA



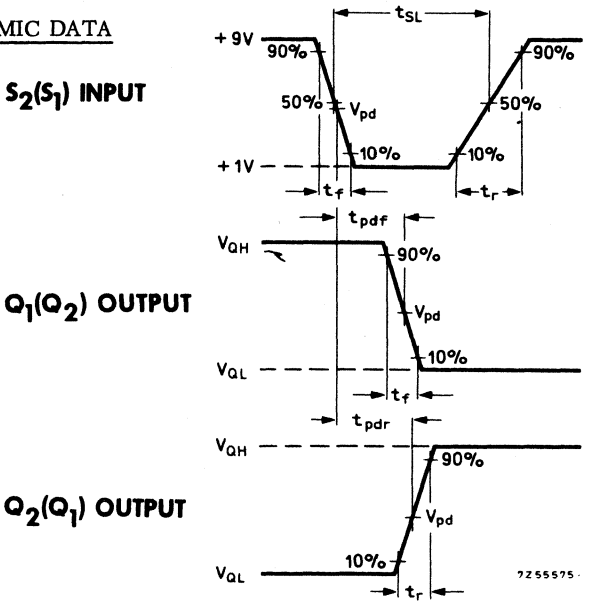
Waveforms illustrating conditions for change of state.



Waveforms illustrating conditions for no change of state.

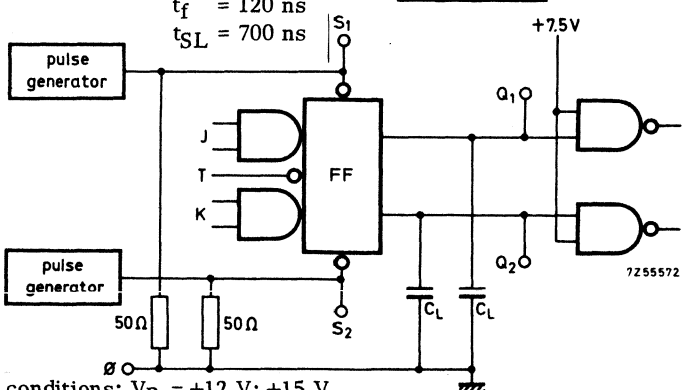
CHARACTERISTICS (continued)

DYNAMIC DATA



Pulse generator (S-input): t_r = 350 ns
t_f = 120 ns
t_{SL} = 700 ns

V_{pd} = +4.5 V



Measuring conditions: V_P = +12 V; +15 V
C_L = 10 pF (including probe and jig capacitance)
T_{amb} = 25 °C
Slow-down terminals are not connected
All other inputs are floating.

Waveforms illustrating conditions for set inputs. Set input signals are not supplied simultaneously.

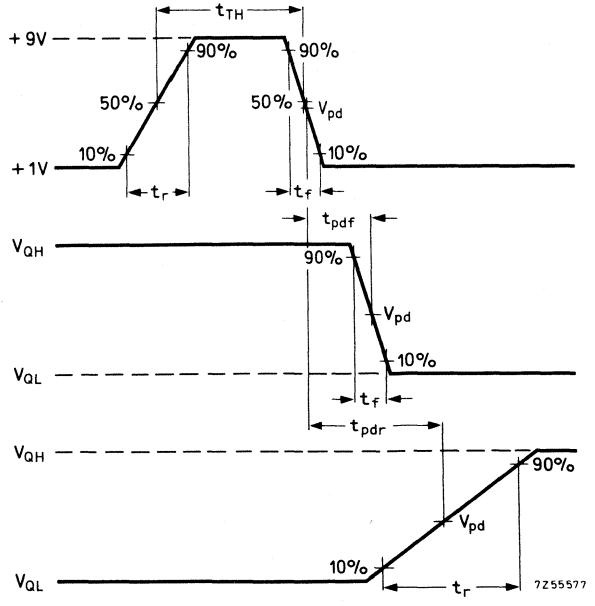
CHARACTERISTICS (continued)

DYNAMIC DATA

T INPUT

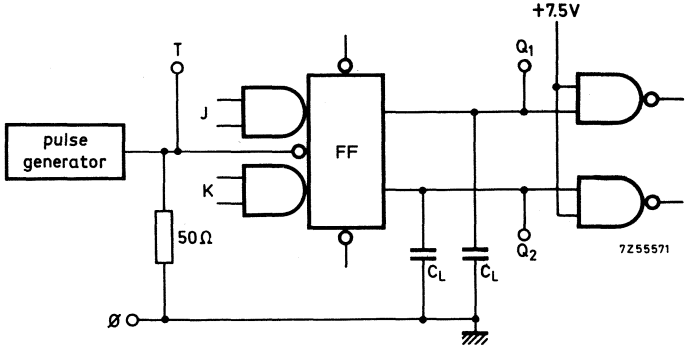
$Q_1(Q_2)$ OUTPUT

$Q_2(Q_1)$ OUTPUT



Pulse generator (T-input): t_r = 350 ns
t_f = 120 ns
t_{TH} = 400 ns

V_{pd} = +4.5 V



Measuring conditions: V_P = +12 V; +15 V
C_L = 10 pF (including probe and jig capacitance)
T_{amb} = 25 °C
Slow-down terminals are not connected
All other inputs are floating.

Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf}.

T T L FJ family

FJH101/7430	single 8-input NAND gate
FJH111/7420	dual 4-input NAND gate
FJH121/7410	triple 3-input NAND gate
FJH131/7400	quadruple 2-input NAND gate
FJH141/7440	dual NAND power gate
FJH151/7450	dual AND-OR-NOT gate (one gate with expander inputs)
FJH161/7451	dual AND-OR-NOT gate
FJH171/7453	expandable 2+2+2+2 input AND-OR-NOT gate
FJH181/7454	2+2+2+2 input AND-OR-NOT gate
FJH191/7480	FULL ADDER
FJH201/7482	2-bit binary FULL ADDER
FJH211/7483	4-bit FULL ADDER
FJH221/7402	quadruple 2-input NOR gate
FJH231/7401	quadruple 2-input NAND gate (open collector output)
FJH241/7404	sextuple single input INVERTER (with an active output; totem pole)
FJH251/7405	sextuple single input INVERTER (with an open collector output)
FJH261/7442	BCD-to-decimal DECODER
FJH271/7486	quadruple 2-input EXCLUSIVE-OR gate
FJH281/74180	8-bit ODD/EVEN PARITY GENERATOR/CHECKER
FJH291/7403	quadruple 2-input NAND gate
FJH301/7426	quadruple 2-input NAND gate (with open collector output)
FJH311/7401-S1	quadruple 2-input NAND gate (with open collector output)
FJH321/7405-S1	sextuple single input INVERTER (with open collector output)
FJH341/9311 /74154	single one-of-sixteen DECODER
FJH351/9312	single 8-input MULTIPLEXER
FJH371/9304	dual FULL ADDER
FJH381/9318	single 8-input priority ENCODER
FJH391/9322	quadruple 2-input digital MULTIPLEXER
FJH401/9309	dual 4-input MULTIPLEXER
FJJ101/7470	single JK FLIP-FLOP (AND-inputs)
FJJ111/7472	single JK master-slave FLIP-FLOP (AND-inputs)
FJJ121/7473	dual JK master-slave FLIP-FLOP
FJJ131/7474	dual D-type edge-triggered FLIP-FLOP
FJJ141/7490	BCD decade COUNTER
FJJ151/7491A	8-bit SHIFT REGISTER
FJJ181/7475	quadruple latch D FLIP-FLOP
FJJ191/7476	dual JK master-slave FLIP-FLOP
FJJ211/7493	single asynchronous 4-bit binary COUNTER
FJJ241/7496N	5-bit SHIFT REGISTER
FJJ251/7492	single asynchronous 4-bit binary COUNTER
FJJ261/74107	dual JK master-slave FLIP-FLOP
FJJ291/74118	hex set-reset LATCH
FJJ321/9300	single 4-bit SHIFT REGISTER
FJJ331/9306	up/down COUNTER
FJJ341/9314	quadruple 2-input LATCH FLIP-FLOP
FJJ351/9310	BCD decade COUNTER
FJJ361/9316	single synchronous 4-bit binary COUNTER
FJJ371/9328	dual 8-bit SHIFT REGISTER
FJJ381/9308	dual quadruple LATCH D FLIP-FLOP
FJK101/74121	monostable MULTIVIBRATOR
FJL101/7441A	single DECODER numerical indicator tube driver
FJL131/7413	dual 4-input SCHMITT-TRIGGER (positive NAND gate)
FJY101/7460	dual 4-input AND-OR-NOT EXPANDER

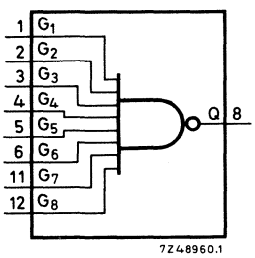
The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

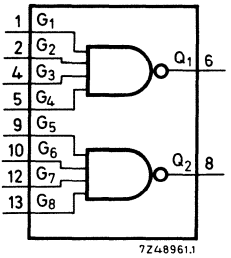
NAND GATES

In the standard temperature range the FJ family comprises the following NAND gates (positive logic):

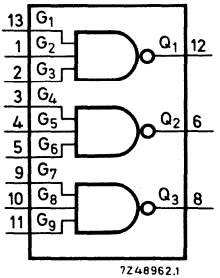
Single 8-input NAND gate	FJH101/7430
Dual 4-input NAND gate	FJH111/7420
Triple 3-input NAND gate	FJH121/7410
Quadruple 2-input NAND gate	FJH131/7400



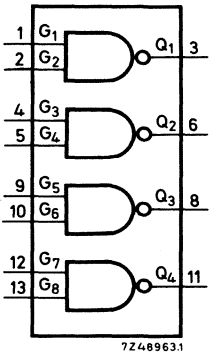
FJH101/7430



FJH111/7420



FJH121/7410



FJH131/7400

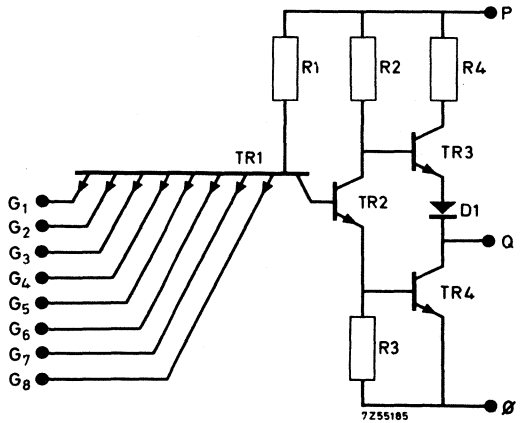
QUICK REFERENCE DATA				
Supply voltage	V_P		5.0 ± 5%	V
Operating ambient temperature range	T_{amb}		0 to +70	°C
Average propagation delay time N = fan-out = 10; T_{amb} = 25 °C	t_{pd}	typ.	11	ns
Available d.c. fan-out (full temperature range)	N_a	≥	10	
D.C. noise margin (full temperature range)	M_L	>	0.4	V
		typ.	1.0	V
Average power consumption (per gate) T_{amb} = 25 °C	P_{av}	typ.	10	mW

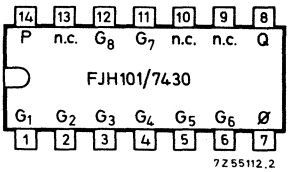
Each gate comprises a multi-emitter AND input gate followed by an inverting amplifier and a totem pole output stage.

PACKAGE OUTLINE: 14 lead plastic dual in-line (type A) (See General Section)

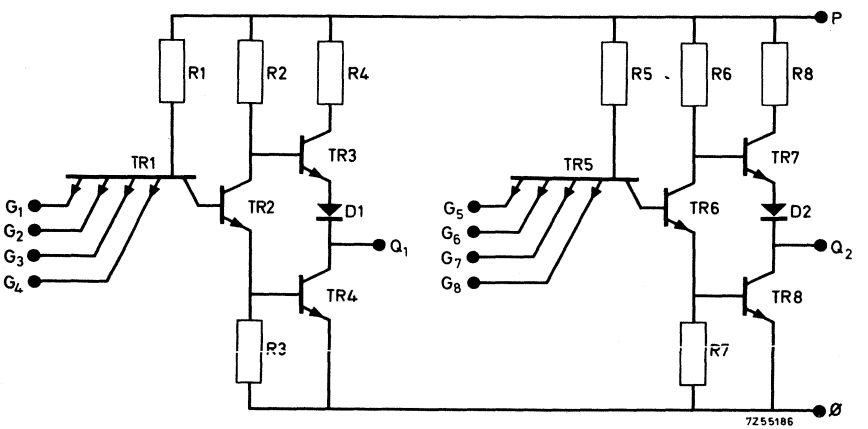
CIRCUIT DIAGRAMS AND TERMINAL CONNECTIONS

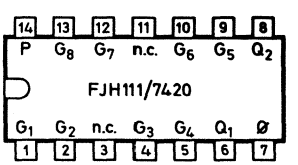
FJH101/7430
Single 8-input NAND gate





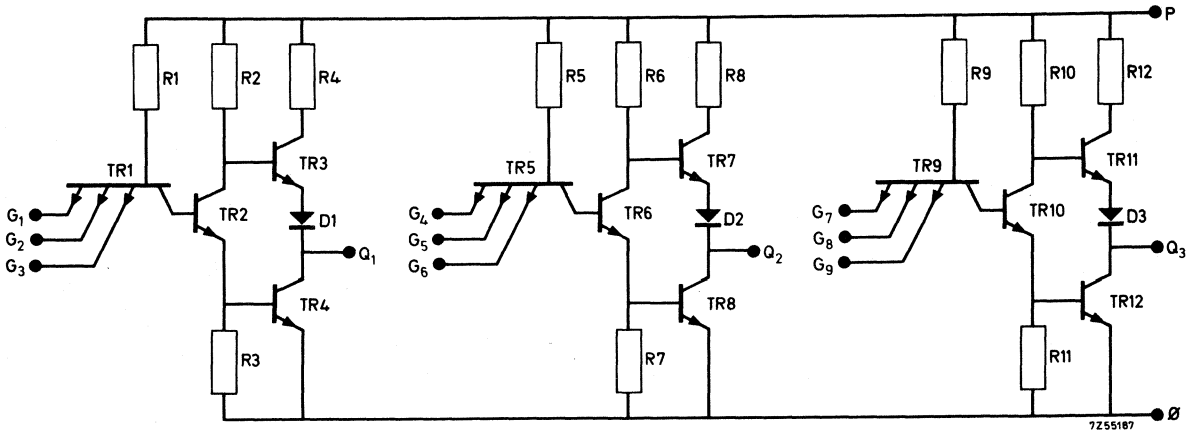
FJH111/7420
Dual 4-input NAND gate

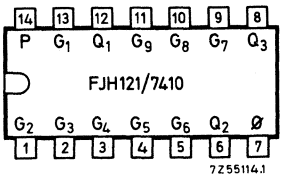




CIRCUIT DIAGRAMS AND TERMINAL CONNECTIONS (continued)

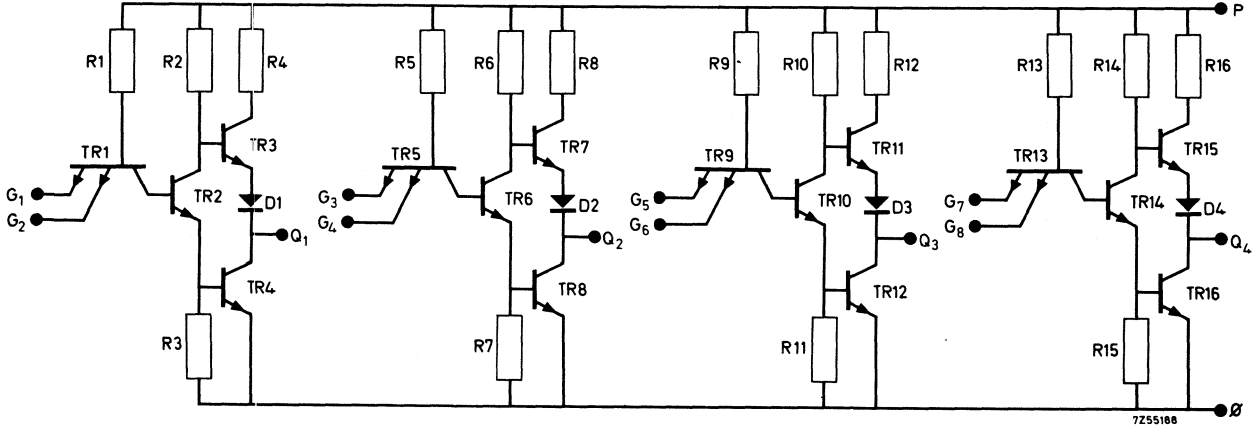
FJH121/7410
Triple 3-input NAND gate

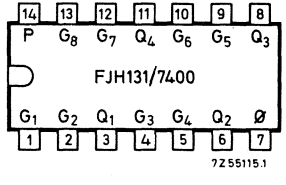




CIRCUIT DIAGRAMS AND TERMINAL CONNECTIONS (continued)

FJH131/7400
Quadruple 2-input NAND gate





LOGIC FUNCTION

Individual gate operation

$C = \overline{A.B}$ positive logic

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

Function table

A	B	C
L	L	H
L	H	H
H	L	H
H	H	L

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.	7.0	V
Output voltage	V_Q	max.	5.5	V
G input voltage	V_G	0 to	5.5	V [1]
Peak negative G input voltage	$-V_{GM}$	max.	2	V [2]
Storage temperature	T_{stg}	-65 to	+150	°C
Operating ambient temperature	T_{amb}	0 to	+ 70	°C

[1] In addition the voltage difference between any two inputs max. 5.5 V

[2] Pulse duration t_p = 20 ns; repetition frequency f = 5 MHz; source resistance $R_S \geq 75\ \Omega$.

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references	
		0	25	70		V_P (V)	
STATIC DATA							
Voltages							
Input threshold LOW	V_{GLmax}	0.8	0.8	0.8	V		
Input threshold HIGH	V_{GHmin}	2.0	2.0	2.0	V		
Output LOW	V_{QLmax}	0.4	0.4	0.4	V	4.75	$I_Q=I_{QLmax}$; $V_G=V_{GHmin}$
Output HIGH	V_{QHmin}	2.4	2.4	2.4	V	4.75	$-I_Q=-I_{QHmax}$; $V_G=V_{GLmax}$
Currents							
Input LOW	$-I_{GLmax}$	1.6	1.6	1.6	mA	5.25	$V_G=V_{QLmax}$; $I_Q=0$
Input HIGH	I_{GHmax}	40	40	40	µA	5.25	$V_G=V_{QHmin}$; $I_Q=0$ other inputs 0V
Output LOW	I_{QLmax}	16	16	16	mA		
Output HIGH	$-I_{QHmax}$	0.4	0.4	0.4	mA		
Output short-circuited 1)	$-I_{Qsc\ min}$ $-I_{Qsc\ max}$	18 55	18 55	18 55	mA mA	5.25	$V_Q=0$; $V_G=0$
DYNAMIC DATA							
Rise propagation delay time	t_{pdr} typ. t_{pdr} <	-	13 22	-	ns ns	5.0	N=10
Fall propagation delay time	t_{pdf} typ. t_{pdf} <	-	8 15	-	ns ns	5.0	N=10

1) Not more than one output should be short circuited at a time.

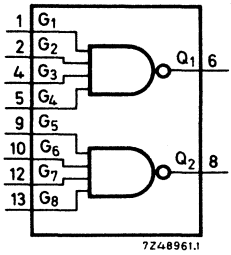
CHARACTERISTICS (continued)

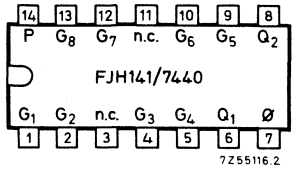
			T_{amb} (°C) 0	25	70		Conditions and references: V_P (V)	
SUPPLY DATA								
Supply current								
Output LOW								
FJH101/7430	I_{PL}	typ.	-	3	-	mA	5.0	V_G = 5.0 V, I_Q = 0
		<	6	6	6	mA	5.25	
FJH111/7420	I_{PL}	typ.	-	6	-	mA	5.0	
		<	11	11	11	mA	5.25	
FJH121/7410	I_{PL}	typ.	-	9	-	mA	5.0	
		<	16.5	16.5	16.5	mA	5.25	
FJH131/7400	I_{PL}	typ.	-	12	-	mA	5.0	
		<	22	22	22	mA	5.25	
Output HIGH								
FJH101/7430	I_{PH}	typ.	-	1	-	mA	5.0	V_G = 0, I_Q = 0
		<	2	2	2	mA	5.25	
FJH111/7420	I_{PH}	typ.	-	2	-	mA	5.0	
		<	4	4	4	mA	5.25	
FJH121/7410	I_{PH}	typ.	-	3	-	mA	5.0	
		<	6	6	6	mA	5.25	
FJH131/7400	I_{PH}	typ.	-	4	-	mA	5.0	
		<	8	8	8	mA	5.25	

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

DUAL NAND POWER GATE



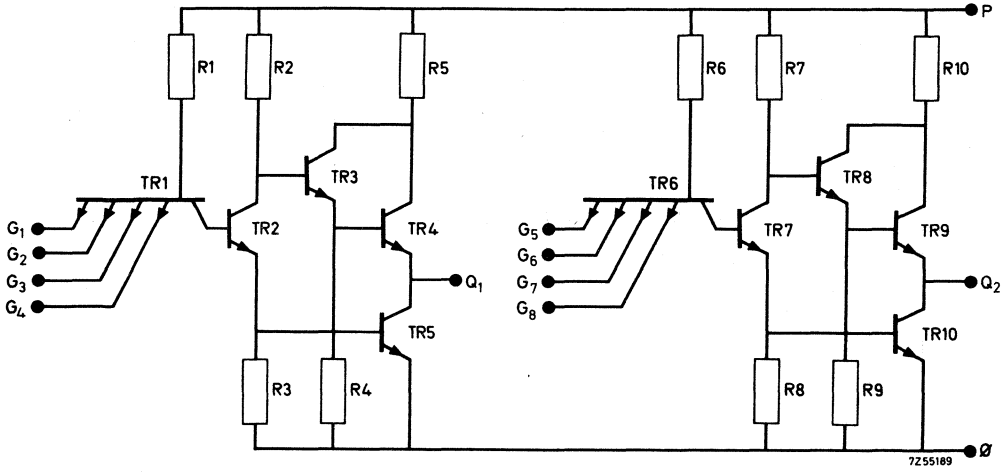


QUICK REFERENCE DATA				
Supply voltage	V_P		5.0±5%	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Average propagation delay time N = fan-out = 30; T_{amb} = 25 °C	t_{pd}	typ.	11	ns
Available d.c. fan-out (full temperature range)	N_a	⩾	30	
D.C. noise margin (full temperature range)	M_L	>	0.4	V
		typ.	1.0	V
Average power consumption (per gate) T_{amb} = 25 °C	P_{av}	typ.	26.5	mW

Each gate comprises a multi-emitter AND gate followed by an inverting amplifier and a totem pole power output stage.

PACKAGE OUTLINE 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAM (each gate)



LOGIC FUNCTION

Individual gate operation

$C = \overline{A.B}$ (positive logic)

Function table

A	B	C
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	7.0	V
Output voltage	V_Q	max.	5.5	V
G input voltage	V_G	max.	5.5	V [1]
Peak negative G input voltage	$-V_{GM}$	max.	2	V [2]
Storage temperature	T_{stg}	-65 to	+150	°C
Operating ambient temperature	T_{amb}	0 to	+70	°C

[1]) In addition, peak voltage difference between any two inputs = max. 5.5 V.
[2]) Pulse duration t_p = 20 ns; repetition frequency f = 5 MHz; source resistance $R_S \geq 75\,\Omega$.

CHARACTERISTICS

			T_{amb} (°C)				Conditions and references	
			0	25	70		V_P (V)	
STATIC DATA								
Voltages								
Input threshold LOW	V_{GLmax}		0.8	0.8	0.8	V		
Input threshold HIGH	V_{GHmin}		2.0	2.0	2.0	V		
Output LOW	V_{QLmax}		0.4	0.4	0.4	V	4.75	$I_Q=I_{QLmax}$; $V_G=V_{GHmin}$
Output HIGH	V_{QHmin}		2.4	2.4	2.4	V	4.75	$-I_Q=-I_{QHmax}$; $V_G=V_{GLmax}$
Currents								
Input LOW	$-I_{GLmax}$		1.6	1.6	1.6	mA	5.25	$V_G=V_{QLmax}$; $I_Q=0$
Input HIGH	I_{GHmax}		40	40	40	µA	5.25	$V_G=V_{QHmin}$; $I_Q=0$ other inputs 0V
Output LOW	I_{QLmax}		48	48	48	mA		
Output HIGH	$-I_{QHmax}$		1.2	1.2	1.2	mA		
Output short-circuited [1]	$-I_{Qscmin}$		18	18	18	mA	5.25	$V_Q=0$; $V_G=0$
	$-I_{Qscmax}$		70	70	70	mA		
SUPPLY DATA								
Supply current								
Output LOW	I_{PL}	typ.	-	17.2	-	mA	5.0	$V_G=5.0$ V; $I_Q=0$
		<	27	27	27	mA	5.25	
Output HIGH	I_{PH}	typ.	-	4.0	-	mA	5.0	$V_G=0$; $I_Q=0$
		<	8.0	8.0	8.0	mA	5.25	
DYNAMIC DATA								
Rise propagation delay time	t_{pdr}	typ.	-	13	-	ns	5.0	N=30
	t_{pdr}	<	-	22	-	ns		
Fall propagation delay time	t_{pdf}	typ.	-	8	-	ns	5.0	N=30
	t_{pdf}	<	-	15	-	ns		

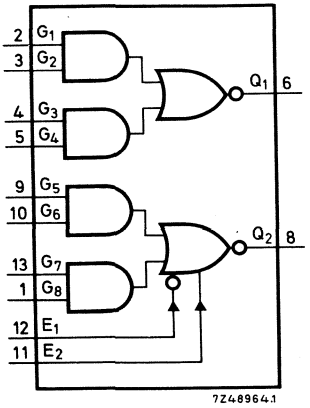
[1] Not more than one output should be short circuited at a time.

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

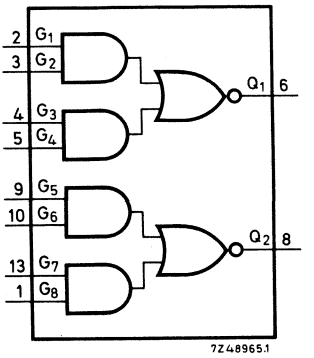
Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

DUAL AND-OR-NOT GATES

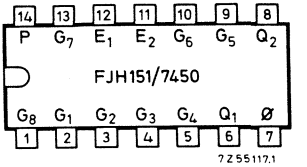
Dual expandable
2+2 input AND-OR-NOT gate FJH151/7450
Dual 2+2 input AND-OR-NOT gate FJH161/7451

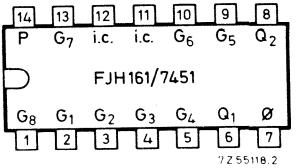


FJH151/7450



FJH161/7451





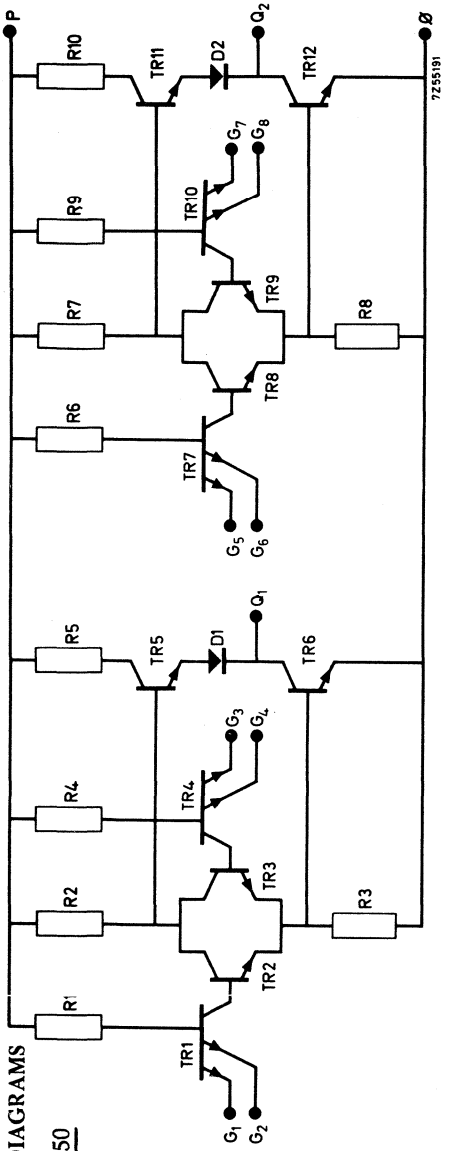
QUICK REFERENCE DATA			
Supply voltage	V_P	5.0 ± 5%	V
Operating ambient temperature range	T_{amb}	0 to +70	°C
Average propagation delay time N = fan-out = 10; T_{amb} = 25 °C	t_{pd}	typ. 11	ns
Available d.c. fan-out (full temperature range)	N_a	⩾ 10	
D.C. noise margin (full temperature range)	M_L	> 0.4 typ. 1.0	V V
Average power consumption (per gate) T_{amb} = 25 °C	P_{av}	typ. 14.25	mW

The FJH151/7450 is a dual 2+2 input AND-OR-NOT gate, one of the two gates having additional inputs for up to four FJY101/7460 expander circuits. It can be arranged to perform the exclusive OR function.
The FJH161/7451 is similar to the FJH151/7540, except for being non-expandable.

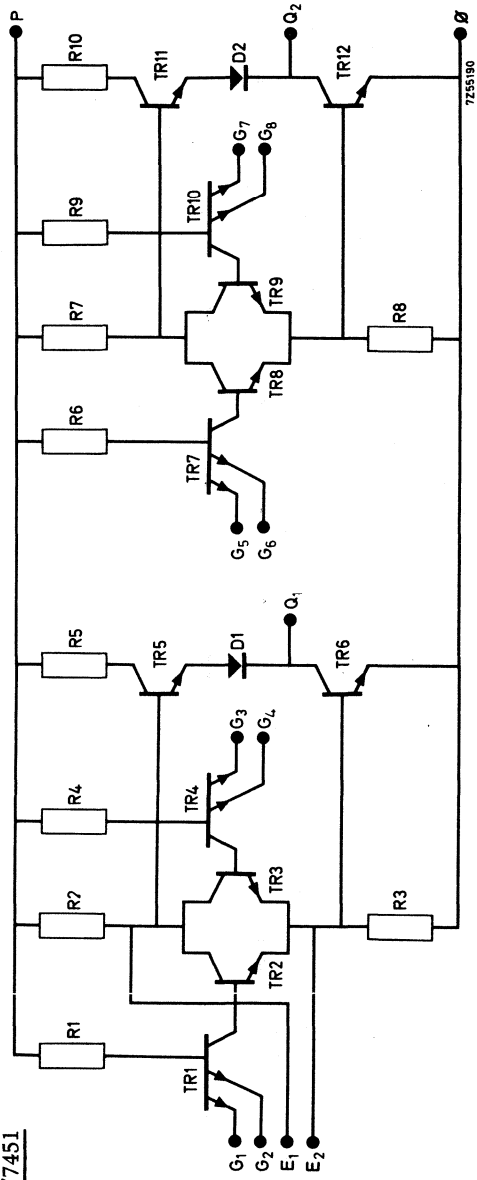
PACKAGE OUTLINE 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAMS

FJH151/7450



FJH161/7451



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	7.0	V
Output voltage	V_Q	max.	5.5	V
G input voltage	V_G	max.	5.5	V [1]
Peak negative G input voltage	$-V_{GM}$	max.	2	V [2]
Storage temperature	T_{stg}	-65 to	+150	°C
Operating ambient temperature	T_{amb}	0 to	70	°C

1) In addition, peak voltage difference between any two inputs = max. 5.5 V.
2) Pulse duration t_p = 20 ms; repetition frequency f = 5 MHz; source resistance $R_S \geq 75\ \Omega$.

CHARACTERISTICS

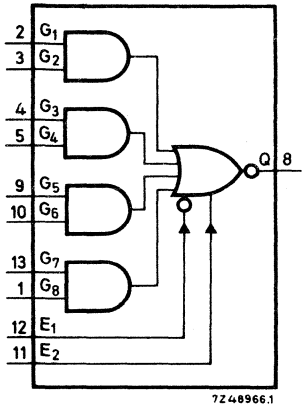
		T_{amb} (°C)				Conditions and references	
		0	25	70		V_P (V)	
STATIC DATA							
Voltages							
Input threshold LOW	V_{GLmax}	0.8	0.8	0.8	V		
Input threshold HIGH	V_{GHmin}	2.0	2.0	2.0	V		
Output LOW	V_{QLmax}	0.4	0.4	0.4	V	4.75	$I_Q=I_{QLmax}$; $V_G=V_{GHmin}$
Output HIGH	V_{QHmin}	2.4	2.4	2.4	V	4.75	$-I_Q=-I_{QHmax}$; $V_G=V_{GLmax}$
Currents							
Input LOW	$-I_{GLmax}$	1.6	1.6	1.6	mA	5.25	$V_G=V_{QLmax}$; $I_Q=0$
Input HIGH	I_{GHmax}	40	40	40	μA	5.25	$V_G=V_{QHmin}$; $I_Q=0$ other inputs 0V
Output LOW	I_{QLmax}	16	16	16	mA		
Output HIGH	$-I_{QHmax}$	0.4	0.4	0.4	mA		
Output short-circuited 1)	$-I_{Qscmin}$	18	18	18	mA	5.25	$V_Q=0$; $V_G=0$
	$-I_{Qscmax}$	55	55	55	mA		
SUPPLY DATA							
Supply current							
Output LOW	I_{PL} typ.	-	7.4	-	mA	5.0	$V_G=5.0$ V; $I_Q=0$
	I_{PL} <	14	14	14	mA	5.25	
Output HIGH	I_{PH} typ.	-	4.0	-	mA	5.0	$V_G=0$; $I_Q=0$
	I_{PH} <	8.0	8.0	8.0	mA	5.25	
DYNAMIC DATA							
Rise propagation delay time	t_{pdr} typ.	-	13	-	ns	5.0	N = 10, one pair of AND inputs at V_G = 0.4 V
	t_{pdr} <	-	22	-	ns		
Fall propagation delay time	t_{pdf} typ.	-	8	-	ns	5.0	
	t_{pdf} <	-	15	-	ns		

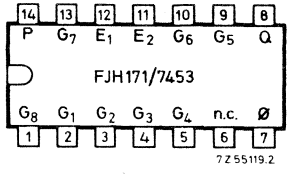
1) Not more than one output should be short circuited at a time.

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

EXPANDABLE 2+2+2+2 INPUT AND-OR-NOT GATE



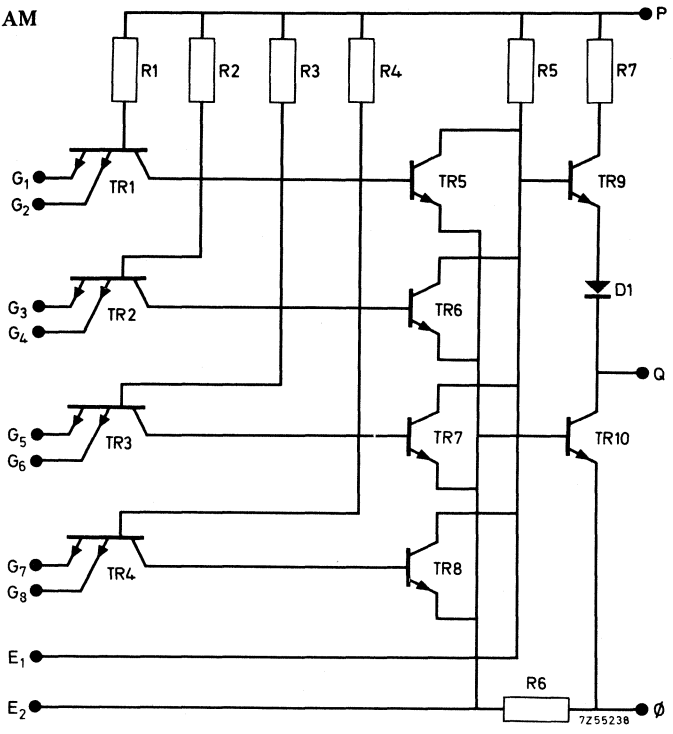


QUICK REFERENCE DATA				
Supply voltage	V_P		5.0 ± 5%	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Average propagation delay time N = fan-out = 10; T_{amb} = 25 °C	t_{pd}	typ.	11	ns
Available d.c. fan-out (full temperature range)	N_a	≥	10	
D.C. noise margin (full temperature range)	M_L	> typ.	0.4 1.0	V V
Average power consumption T_{amb} = 25 °C	P_{av}	typ.	22.75	mW

The FJH171/7453 has additional inputs for up to four FJY101/7460 expander circuits.

PACKAGE OUTLINE: 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAM



LOGIC FUNCTION

$Q = \overline{G_1.G_2 + G_3.G_4 + G_5.G_6 + G_7.G_8 + EX}$ (for positive logic)

EX represents the extra function available if gate expander FJY101 is used. (Connect E_1, E_2 to Q_1, Q_2 respectively or to Q_3, Q_4 respectively, of the FJY101 to get a 4-input NAND function).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	7.0	V
Output voltage	V_Q	max.	5.5	V
G input voltage	V_G	max.	5.5	V [1]
Peak negative G input voltage	$-V_{GM}$	max.	2	V [2]
Storage temperature	T_{stg}	-65 to	+150	°C
Operating ambient temperature	T_{amb}	0 to	+70	°C

[1] In addition, the voltage between any two inputs must not exceed 5.5 V.
[2] Pulse duration t_p = 20 ns; repetition frequency f = 5 MHz; source resistance $R_S \geq 75\,\Omega$.

CHARACTERISTICS

			T_{amb} (°C)				Conditions and references	
			0	25	70		V_P (V)	
STATIC DATA								
Voltages								
Input threshold LOW	V_{GLmax}		0.8	0.8	0.8	V		
Input threshold HIGH	V_{GHmin}		2.0	2.0	2.0	V		
Output LOW	V_{QLmax}		0.4	0.4	0.4	V	4.75	$I_Q = I_{QLmax}$ $V_G = V_{GHmin}$
Output HIGH	V_{QHmin}		2.4	2.4	2.4	V	4.75	$-I_Q = -I_{QHmax}$; $V_G = V_{GLmax}$
Currents								
Input LOW	$-I_{GLmax}$		1.6	1.6	1.6	mA	5.25	$V_G = V_{QLmax}$; $I_Q = 0$
Input HIGH	I_{GHmax}		40	40	40	μA	5.25	$V_G = V_{QHmin}$; $I_Q = 0$ other inputs 0 V
Output LOW	I_{QLmax}		16	16	16	mA		
Output HIGH	$-I_{QHmax}$		0.4	0.4	0.4	mA		
Output short-circuited (see note 1)	$-I_{Qsc}$	min	18	18	18	mA	5.25	$V_Q = 0$; $V_G = 0$
	$-I_{Qsc}$	max	55	55	55	mA		
SUPPLY DATA								
Supply current								
Output LOW	I_{PL}	typ.	-	5.1	-	mA	5.0	$V_G = 5.0$ V; $I_Q = 0$
		<	9.5	9.5	9.5	mA	5.25	
Output HIGH	I_{PH}	typ.	-	4.0	-	mA	5.0	$V_G = 0$; $I_Q = 0$
		<	8.0	8.0	8.0	mA	5.25	
DYNAMIC DATA								
Rise propagation delay time	t_{pdr}	typ.	-	13	-	ns	5.0	N = 10 one pair of AND inputs at $V_G = 0.4$ V
	t_{pdr}	<	-	22	-	ns	5.0	
Fall propagation delay time	t_{pdf}	typ.	-	8	-	ns	5.0	
	t_{pdf}	<	-	15	-	ns	5.0	

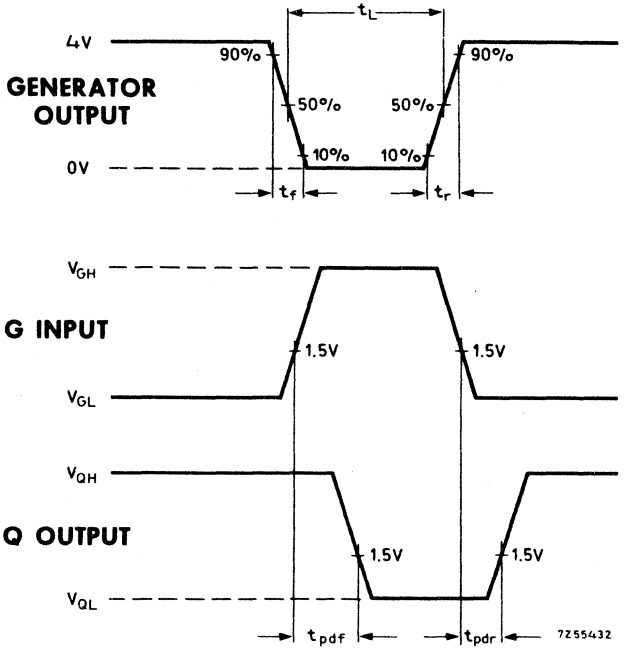
Note 1: Not more than one output must be short circuited at any time.

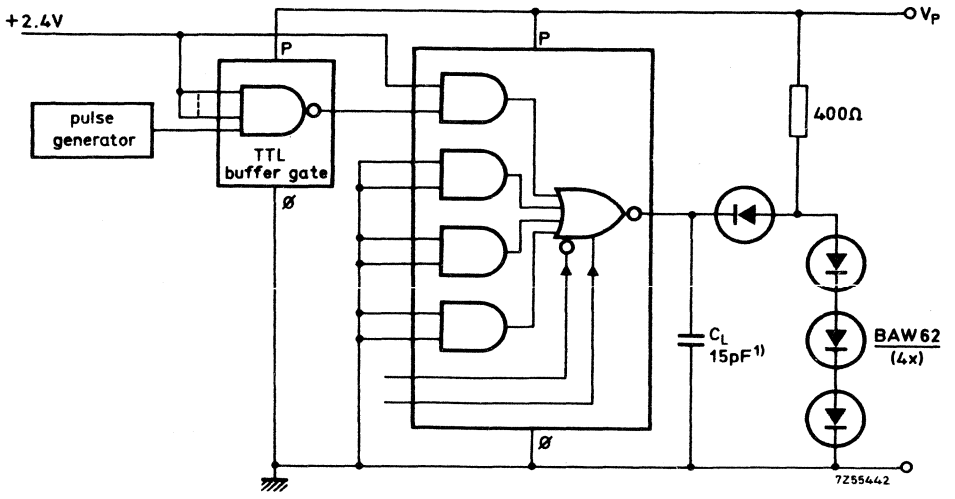
CHARACTERISTICS (continued)

DYNAMIC DATA

Generator:

f = 1 MHz
t_L = 0.5 μs
$t_f \leq 15$ ns
$t_r \leq 15$ ns
R_S = 50 Ω





1) Including probe and jig capacitance.

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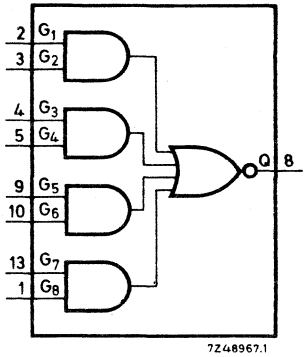
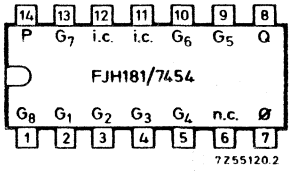
Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

2+2+2+2 INPUT AND-OR-NOT GATE

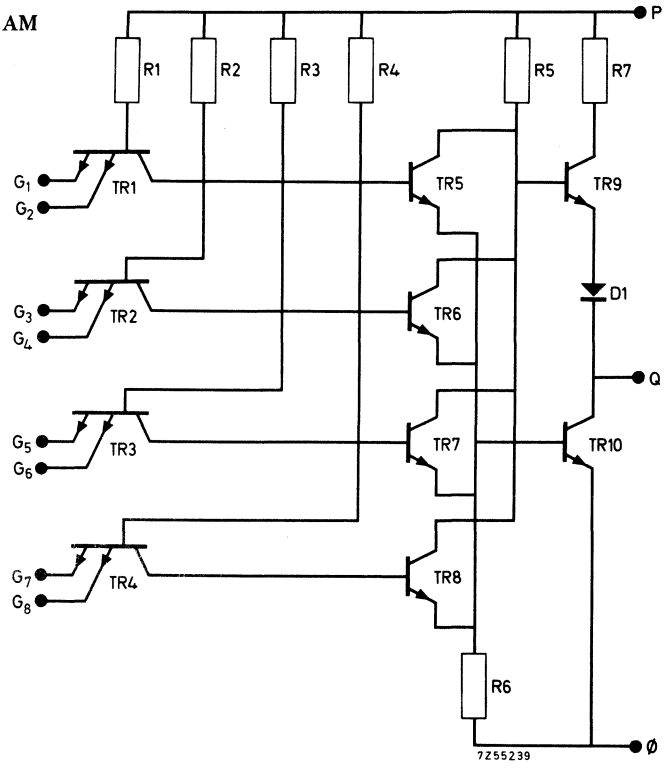




QUICK REFERENCE DATA				
Supply voltage	V_P		5.0 ±5%	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Average propagation delay time N = fan-out = 10; T_{amb} = 25 °C	t_{pd}	typ.	11	ns
Available d.c. fan-out (full temperature range)	N_a	≥	10	
D.C. noise margin (full temperature range)	M_L	> typ.	0.4 1.0	V V
Average power consumption T_{amb} = 25 °C	P_{av}	typ.	22.75	mW

PACKAGE OUTLINE 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAM



LOGIC FUNCTION

$Q = \overline{G_1 \cdot G_2 + G_3 \cdot G_4 + G_5 \cdot G_6 + G_7 \cdot G_8}$ (for positive logic)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.	7.0	V
Output voltage	V_Q	max.	5.5	V
G input voltage	V_G	max.	5.5	V [1]
Peak negative G input voltage	$-V_{GM}$	max.	2	V [2]
Storage temperature	T_{stg}	-65 to	+150	°C
Operating ambient temperature	T_{amb}	0 to	+70	°C

[1] In addition the voltage between any two inputs must not exceed 5.5 V.
[2] Pulse duration $t_p = 20$ ns; repetition frequency f = 5 MHz; source resistance $R_S \geq 75\ \Omega$.

CHARACTERISTICS

			T_{amb} (°C)				Conditions and references	
			0	25	70		V_P (V)	
STATIC DATA								
Voltages								
Input threshold LOW	V_{GLmax}		0.8	0.8	0.8	V		
Input threshold HIGH	V_{GHmin}		2.0	2.0	2.0	V		
Output LOW	V_{QLmax}		0.4	0.4	0.4	V	4.75	$I_Q = I_{QLmax}$ $V_G = V_{GHmin}$
Output HIGH	V_{QHmin}		2.4	2.4	2.4	V	4.75	$-I_Q = -I_{QHmax}$; $V_G = V_{GLmax}$
Currents								
Input LOW	$-I_{GLmax}$		1.6	1.6	1.6	mA	5.25	$V_G = V_{QLmax}$; $I_Q = 0$
Input HIGH	I_{GHmax}		40	40	40	μA	5.25	$V_G = V_{QHmin}$; $I_Q = 0$ other inputs 0 V
Output LOW	I_{QLmax}		16	16	16	mA		
Output HIGH	$-I_{QHmax}$		0.4	0.4	0.4	mA		
Output short-circuited [1]	$-I_{Qsc\ min}$		18	18	18	mA	5.25	$V_Q = 0$; $V_G = 0$
	$-I_{Qsc\ max}$		55	55	55	mA		
SUPPLY DATA								
Supply current								
Output LOW	I_{PL}	typ.	-	5.1	-	mA	5.0	$V_G = 5.0$ V; $I_Q = 0$
		<	9.5	9.5	9.5	mA	5.25	
Output HIGH	I_{PH}	typ.	-	4.0	-	mA	5.0	$V_G = 0$; $I_Q = 0$
		<	8.0	8.0	8.0	mA	5.25	
DYNAMIC DATA								
Rise propagation delay time	t_{pdr}	typ.	-	13	-	ns	5.0	N = 10 one pair AND inputs at $V_G = 0.4$ V
	t_{pdr}	<	-	22	-	ns	5.0	
Fall propagation delay time	t_{pdf}	typ.	-	8	-	ns	5.0	
	t_{pdf}	<	-	15	-	ns	5.0	

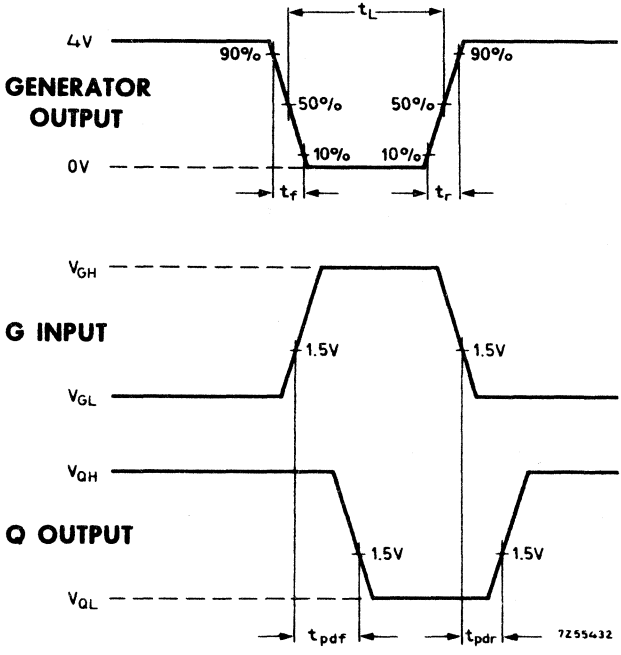
[1] Not more than one output should be short circuited at a time.

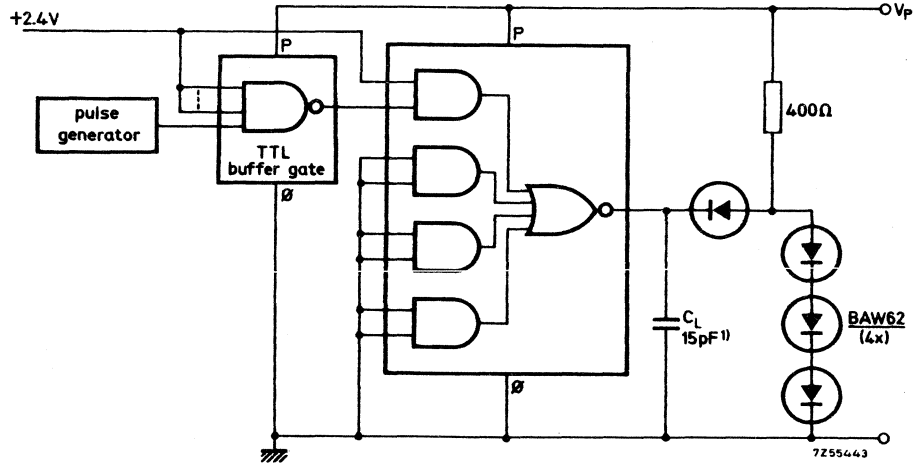
CHARACTERISTICS (continued)

DYNAMIC DATA

Generator

f = 1 MHz
t_L = 0.5 μs
$t_f \leq 15$ ns
$t_r \leq 15$ ns
R_S = 50 Ω





[1]) Including probe and jig capacitance.

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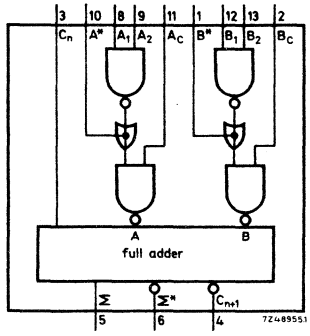
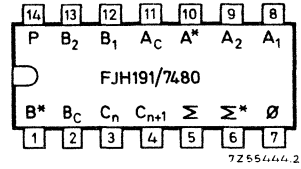
Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

FULL ADDER



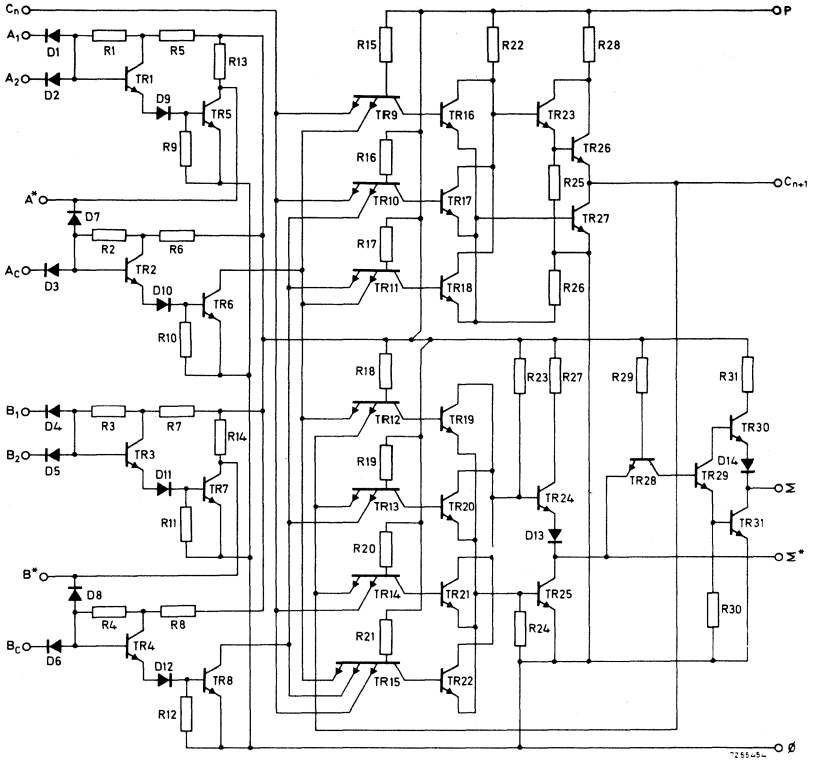


QUICK REFERENCE DATA			
Supply voltage	V_P	5.0 ± 5%	V
Operating ambient temperature	T_{amb}	0 to +70	°C
Available d.c. fan-out for outputs: Σ; Σ* (sum outputs)	N_a	≥ 10	
C_n+1 (inverted carry output)	N_a	≥ 5	
Average power consumption	P_{av}	typ. 105	mW

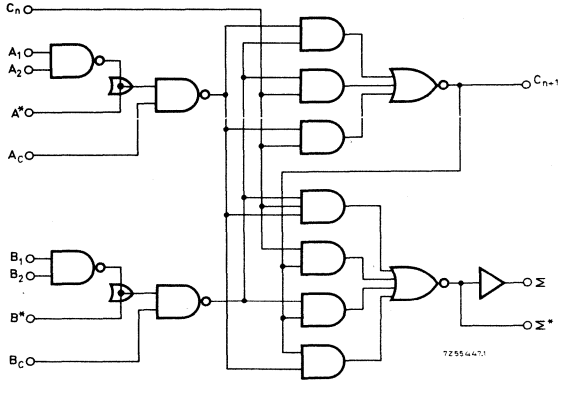
The FJH191/7480 is a single-bit, high speed, binary full adder with gated complementary inputs, complementary sum outputs (Σ and Σ*), and inverted carry output.

PACKAGE OUTLINE :14 lead plastic dual in-line (type A) See General Section

CIRCUIT DIAGRAM



LOGIC DIAGRAM



FUNCTION TABLE

C_n	A	B	C_{n+1}	Σ	Σ^*
L	L	L	H	L	H
L	H	L	H	H	L
L	L	H	H	H	L
L	H	H	L	L	H
H	L	L	H	H	L
H	H	L	L	L	H
H	L	H	L	L	H
H	H	H	L	H	L

$$A = \overline{A^* \cdot A_C}$$
$$A^* = \overline{A_1 \cdot A_2}$$
$$B = \overline{B^* \cdot B_C}$$
$$B^* = \overline{B_1 \cdot B_2}$$

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

Notes

When A^* is used as an input, A_1 and A_2 must be connected to ϕ; when B^* is used as an input, B_1 and B_2 must be connected to ϕ.

When A_1 and A_2 are used as inputs, A^* must either be open or in wired-OR use; the same applies to B^* when B_1 and B_2 are used as inputs.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	7.0	V
Input voltage	V_G; V_{Q_1}; V_{Q_2}	max.	5.5	V
Peak negative input voltage	$-V_{IM}$	max.	2	V [1]
Operating ambient temperature	T_{amb}	0 to	+70	°C
Storage temperature	T_{stg}	-65 to	+125	°C

1) Pulse duration $t_p = 20$ ns; repetition frequency $f = 5$ MHz; source resistance $R_S > 75\ \Omega$

CHARACTERISTICS

		T_{amb} (°C)				Conditions and References	
		0	25	70		V_P (V)	
STATIC DATA							
Input threshold LOW	V_{ILmax}	0.8	0.8	0.8	V		
Input threshold HIGH	V_{IHmin}	2.0	2.0	2.0	V		
Output LOW							
at Σ ; Σ*	V_{OLmax}	0.4	0.4	0.4	V	4.75	I_O = 16 mA
at C_{n+1}	V_{OLmax}	0.4	0.4	0.4	V	4.75	I_O = 8 mA
at A*; B*	V_{OLmax}	0.4	0.4	0.4	V	4.75	I_O = 4.8 mA
Output HIGH							
at Σ ; Σ*	V_{OHmin}	2.4	2.4	2.4	V	4.75	I_O = −400 μA
at C_{n+1}	V_{OHmin}	2.4	2.4	2.4	V	4.75	I_O = −200 μA
at A*; B*	V_{OHmin}	2.4	2.4	2.4	V	4.75	I_O = −120 μA
Currents							
Input LOW							
at C_n	$-I_{ILmax}$	8.0	8.0	8.0	mA	5.25	$V_I = V_{OLmax}$; $I_O = 0$
at A_1; A_2; A_C; B_1; B_2; B_C	$-I_{ILmax}$	1.6	1.6	1.6	mA	5.25	$V_I = V_{OLmax}$; $I_O = 0$
at A*; B*	$-I_{ILmax}$	2.6	2.6	2.6	mA	5.25	$V_O = V_{OLmax}$; $I_O = 0$
Input HIGH							
at C_n	I_{IHmax}	200	200	200	μA	5.25	$V_I = V_{OLmax}$; $I_O = 0$
	I_{IHmax}	1	1	1	mA	5.25	V_I = 5.5 V; I_O = 0
at A_1; A_2; A_C	I_{IHmax}	15	15	15	μA	5.25	$V_I = V_{OHmin}$; $I_O = 0$
B_1; B_2; B_C	I_{IHmax}	1	1	1	mA	5.25	V_I = 5.5 V; I_O = 0
Output short circuit							
at Σ ; Σ*	$-I_{Oscmin}$	18	18	18	mA	5.25	V_O = 0; V_O = 0
	$-I_{Oscmax}$	57	57	57	mA	5.25	
at C_{n+1}	I_{Oscmin}	18	18	18	mA	5.25	V_O = 0; V_I = 0
see Note 1	I_{Oscmax}	70	70	70	mA	5.25	
SUPPLY DATA							
Supply current	I_P typ.	-	21	-	mA	5.0	All terminals open
	I_P <	35	35	35	mA	5.25	

1) Not more than one output should be short circuited at a time.

CHARACTERISTICS (continued)

		T_{amb} (°C)			Conditions and References		
		0	25	70	V_p (V)	Waveform Fig.1	loading circuit
DYNAMIC DATA							
Rise propagation delay times:							
$C_n \rightarrow C_{n+1}$	t_{pdr} typ.	–	13	– ns	5.0	A	Fig.2
	t_{pdr} <	–	17	– ns	5.0		
$A_1 \rightarrow A^*$	t_{pdr} typ.	–	48	– ns	5.0	A	Fig.3
	t_{pdr} <	–	65	– ns	5.0		
$B_1 \rightarrow B^*$	t_{pdr} typ.	–	48	– ns	5.0	A	Fig.4
	t_{pdr} <	–	65	– ns	5.0		
$B_C \rightarrow C_{n+1}$	t_{pdr} typ.	–	18	– ns	5.0	B	Fig.5
	t_{pdr} <	–	25	– ns	5.0		
$A_C \rightarrow \Sigma$	t_{pdr} typ.	–	52	– ns	5.0	B	Fig.6
	t_{pdr} <	–	70	– ns	5.0		
$B_C \rightarrow \Sigma^*$	t_{pdr} typ.	–	38	– ns	5.0	B	Fig.7
	t_{pdr} <	–	55	– ns	5.0		
Fall propagation delay times:							
$C_n \rightarrow C_{n+1}$	t_{pdf} typ.	–	8	– ns	5.0	A	Fig.2
	t_{pdf} <	–	12	– ns	5.0		
$A_1 \rightarrow A^*$	t_{pdf} typ.	–	17	– ns	5.0	A	Fig.3
	t_{pdf} <	–	25	– ns	5.0		
$B_1 \rightarrow B^*$	t_{pdf} typ.	–	17	– ns	5.0	A	Fig.4
	t_{pdf} <	–	25	– ns	5.0		
$B_C \rightarrow C_{n+1}$	t_{pdf} typ.	–	38	– ns	5.0	B	Fig.5
	t_{pdf} <	–	55	– ns	5.0		
$A_C \rightarrow \Sigma$	t_{pdf} typ.	–	62	– ns	5.0	B	Fig.6
	t_{pdf} <	–	80	– ns	5.0		
$B_C \rightarrow \Sigma^*$	t_{pdf} typ.	–	56	– ns	5.0	B	Fig.7
	t_{pdf} <	–	75	– ns	5.0		

CHARACTERISTICS (continued)

DYNAMIC DATA

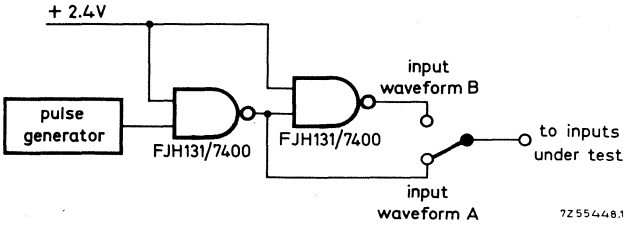


Fig.1

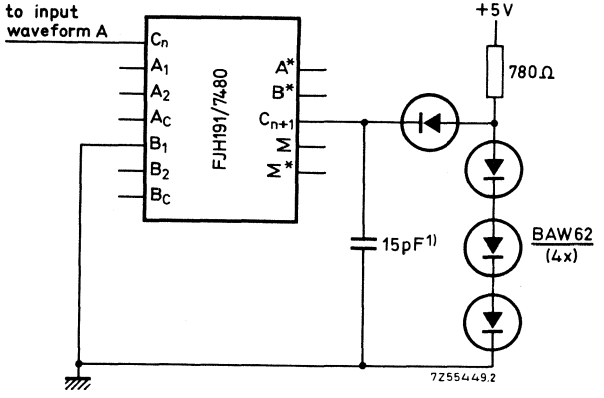


Fig.2 Fan out: N = 5

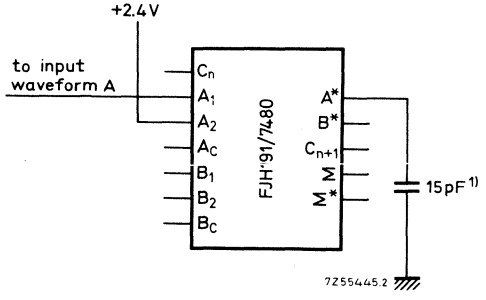


Fig.3

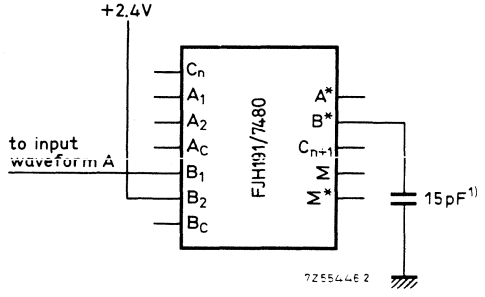


Fig.4

1) Including probe and jig capacitance

CHARACTERISTICS (continued)

DYNAMIC DATA

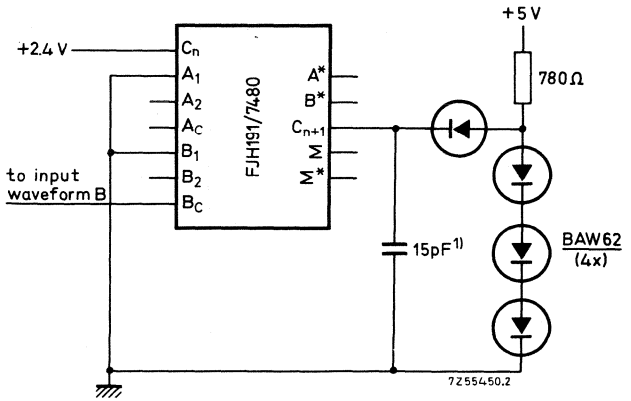


Fig.5 Fan out: N = 5

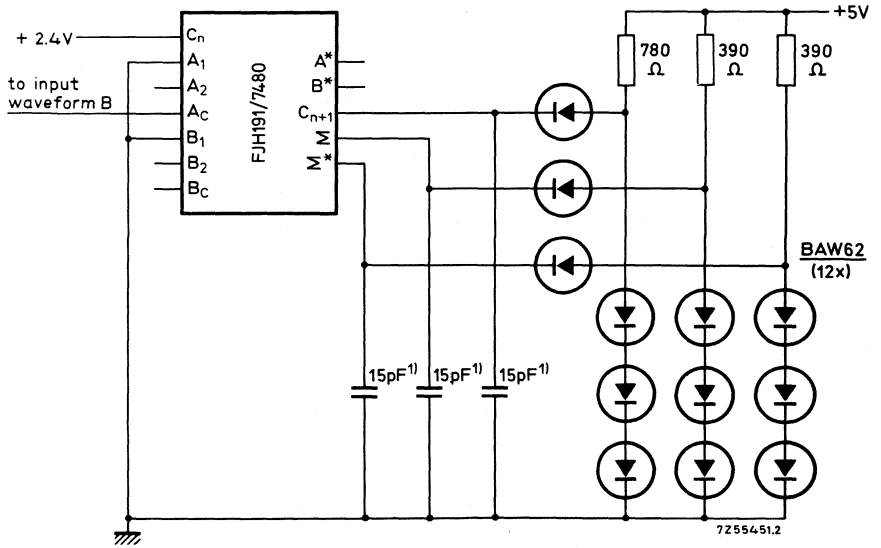


Fig.6 Fan out Q_4: N = 10
Fan out Q_5: N = 10
Fan out Q_3: N = 5

1) Including probe and jig capacitance

CHARACTERISTICS (continued)

DYNAMIC DATA

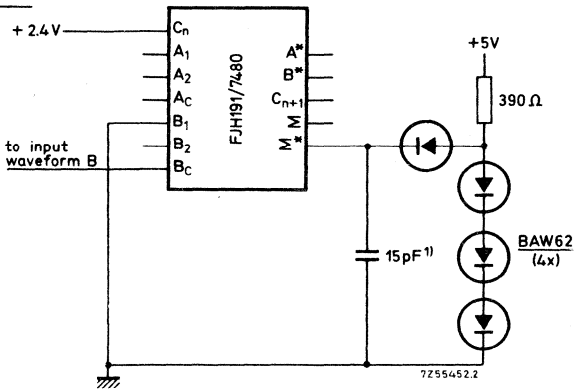
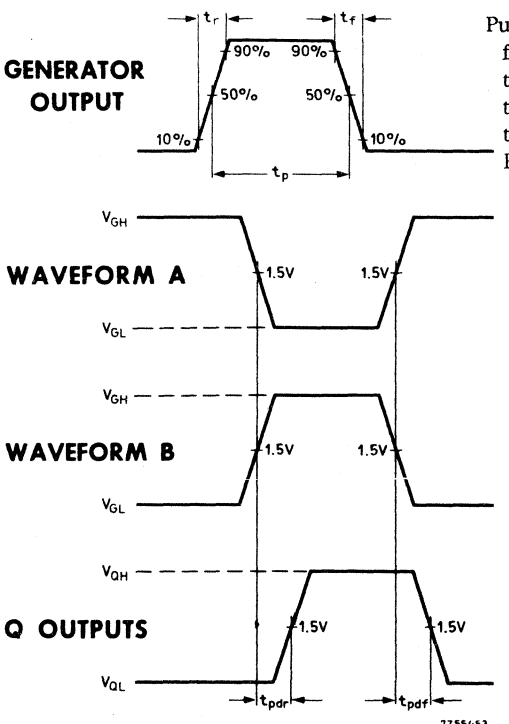


Fig.7 Fan out: N = 10



1) Including probe and jig capacitance

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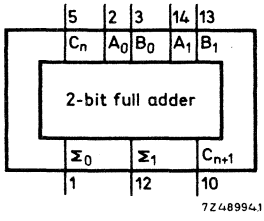
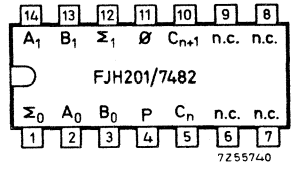
Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

2 - BIT BINARY FULL ADDER

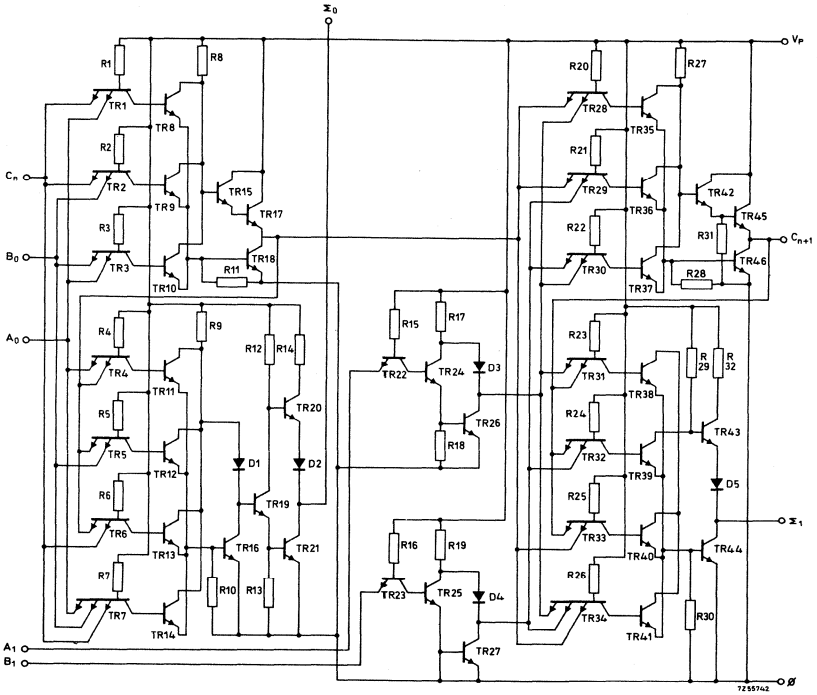




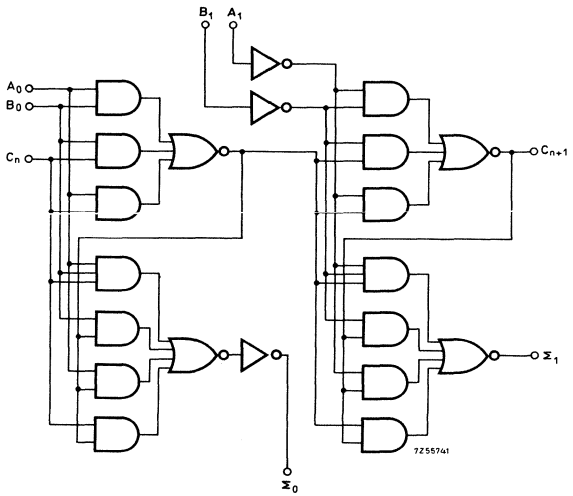
QUICK REFERENCE DATA			
Supply voltage	V_P	5.0 ±5%	V
Operating ambient temperature	T_{amb}	0 to +70	°C
Available d.c. fan-out			
for outputs: Σ_0; Σ_1 (sum outputs)	N_a	≥ 10	
C_{n+1} (carry output)	N_a	≥ 5	
Average power consumption	P_{av}	175	mW

PACKAGE OUTLINE: 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAM



LOGIC DIAGRAM



The FJH201/7482 full adder is designed for medium-to-high speed, multiple-bit, parallel-add/serial-carry applications and performs the addition of two 2-bit binary numbers. The summation outputs (Σ_0 and Σ_1) are provided for each bit and the resultant carry output (C_{n+1}) is obtained from the second bit. High speed serial-carry circuitry within each bit minimises the necessity for extensive "look-ahead" and carry-cascading circuits.

INPUT				OUTPUT					
				C_n = L			C_n = H		
A_0	B_0	A_1	B_1	Σ_0	Σ_1	C_{n+1}	Σ_0	Σ_1	C_{n+1}
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	7.0	V
D.C. input voltage	V_I	max.	5.5	V [1]
Peak negative transient input voltage	$-V_{IM}$	max.	2.0	V [2]
Operating ambient temperature	T_{amb}	0 to	+70	°C
Storage temperature	T_{stg}	−65 to	+150	°C

[1] In addition, the voltage between any two inputs must not exceed 5.5 V.
[2] Pulse duration t_p = 20 ns; repetition frequency f = 5 MHz; source resistance $R_S \geq 75\ \Omega$

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references	
		0	25	70		V_P (V)	
STATIC DATA							
Voltages							
Input threshold LOW	V_{ILmax}	0.8	0.8	0.8	V	4.75	
Input threshold HIGH	V_{IHmin}	2.0	2.0	2.0	V	4.75	
Output LOW							
at Σ_0; Σ_1	V_{OLmax}	0.4	0.4	0.4	V	4.75	I_O = 16 mA
at C_{n+1}	V_{OLmax}	0.4	0.4	0.4	V	4.75	I_O = 8 mA
Output HIGH							
at Σ_0; Σ_1	V_{OHmin}	2.4	2.4	2.4	V	4.75	I_O = −400 µA
at C_{n+1}	V_{OHmin}	2.4	2.4	2.4	V	4.75	I_O = −200 µA
Currents							
Input LOW							
at A_1; B_1	$-I_{ILmax}$	1.6	1.6	1.6	mA	5.25	V_I = 0.4 V
at A_0; B_0; C_n	$-I_{ILmax}$	6.4	6.4	6.4	mA	5.25	V_I = 0.4 V
Input HIGH							
at A_1; B_1	I_{IHmax}	40	40	40	µA	5.25	V_I = 2.4 V
	I_{IHmax}	1	1	1	mA	5.25	V_I = 5.5 V
at A_0; B_0; C_n	I_{IHmax}	160	160	160	µA	5.25	V_I = 2.4 V
	I_{IHmax}	1	1	1	mA	5.25	V_I = 5.5 V
Output LOW							
at Σ_0; Σ_1	I_{OLmax}	16	16	16	mA		
at C_{n+1}	I_{OLmax}	8	8	8	mA		
Output HIGH							
at Σ_0; Σ_1	$-I_{OHmax}$	0.4	0.4	0.4	mA		
at C_{n+1}	$-I_{OHmax}$	0.2	0.2	0.2	mA		
Output short circuit [1]							
at Σ_0; Σ_1; C_{n+1}	$-I_{scmin}$	18	18	18	mA	5.25	
at Σ_0; Σ_1	$-I_{scmax}$	55	55	55	mA	5.25	
at C_{n+1}	$-I_{scmax}$	70	70	70	mA	5.25	
SUPPLY DATA							
Supply current	I_p typ.	–	35	–	mA	5.0	All terminals open
	I_p <	58	58	58	mA	5.25	

[1] Only one output to be shorted at a time

CHARACTERISTICS (continued)

		T_{amb} (°C)			Conditions and references	
		0	25	70	V_P (V)	
DYNAMIC DATA						
Rise propagation delay times						
$C_n \rightarrow \Sigma_0$	t_{pdr} <	–	34	– ns	5.0	C_L = 15 pF; N_a = 10
$B_1 \rightarrow \Sigma_1$	t_{pdr} <	–	40	– ns	5.0	
$C_n \rightarrow \Sigma_1$	t_{pdr} <	–	38	– ns	5.0	
$C_n \rightarrow C_{n+1}$	t_{pdr} typ.	–	12	– ns	5.0	C_L = 15 pF; N_a = 5
	t_{pdr} <	–	29	– ns	5.0	
Fall propagation delay times						
$C_n \rightarrow \Sigma_0$	t_{pdf} <	–	40	– ns	5.0	C_L = 15 pF; N_a = 10
$B_1 \rightarrow \Sigma_1$	t_{pdf} <	–	35	– ns	5.0	
$C_n \rightarrow \Sigma_1$	t_{pdf} <	–	42	– ns	5.0	
$C_n \rightarrow C_{n+1}$	t_{pdf} typ.	–	17	– ns	5.0	C_L = 15 pF; N_a = 5
	t_{pdf} <	–	27	– ns	5.0	

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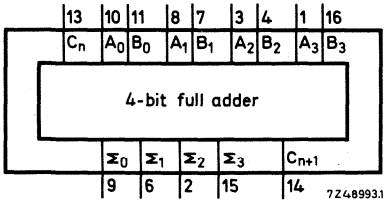
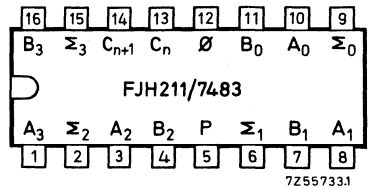
4 - BIT FULL ADDER

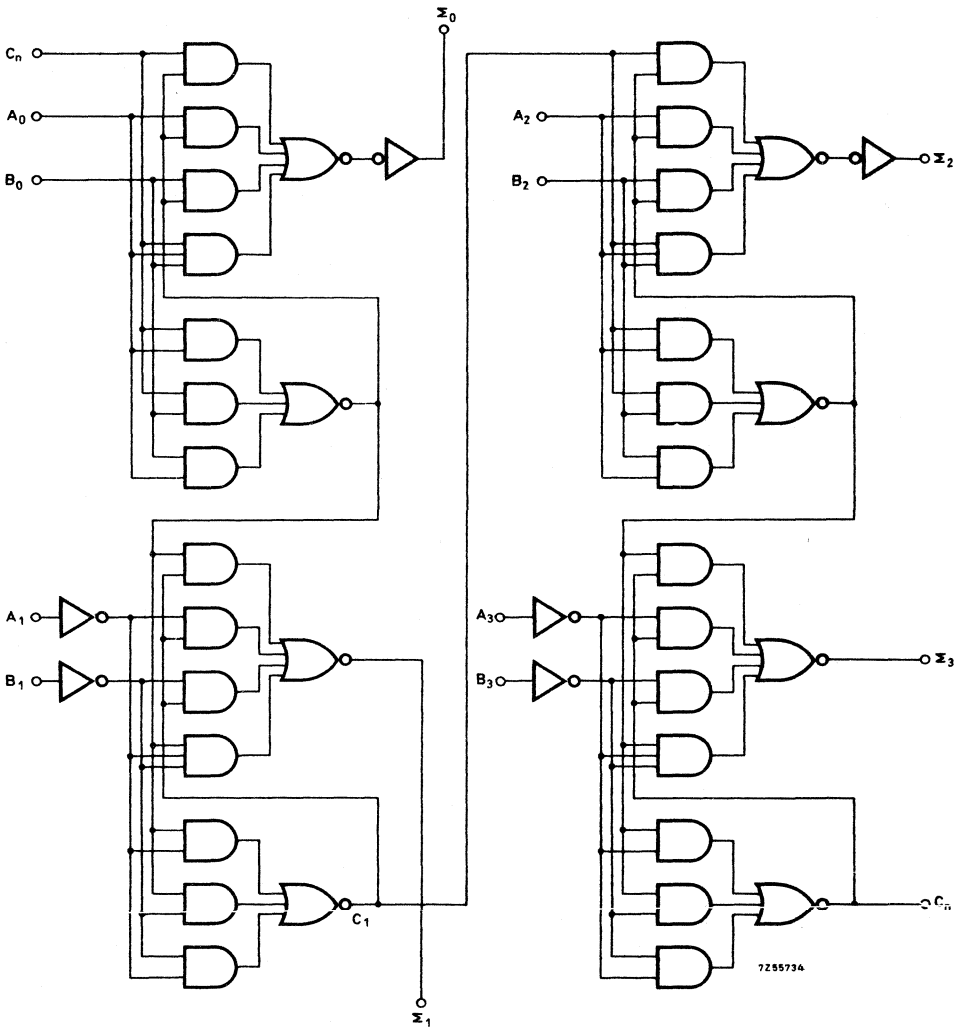




QUICK REFERENCE DATA				
Supply voltage	V_P	5.0 ± 5%		V
Operating ambient temperature	T_{amb}	0 to +70		°C
Available d.c. fan-out (full temperature range)				
from Σ_0, Σ_1, Σ_2, Σ_3	N_a	>	10	
from C_{n+1}	N_a	>	5	
Average propagation delay time				
$C_n \rightarrow C_{n+1}$	t_{pd}	typ.	29	ns
$C_n \rightarrow \Sigma_3$	t_{pd}	<	55	ns
$B_3 \rightarrow \Sigma_3$	t_{pd}	<	38	ns
D.C. noise margin (full temperature range)	M	>	0.4	V
Average power consumption		typ.	1.0	V
T_{amb} = 25 °C	P_{av}	typ.	390	mW

PACKAGE OUTLINE : 16 lead plastic dual in-line (type A) (See General Section)

LOGIC FUNCTION



The FJH211/7483 consists of a full adder for two words of four bits each plus a carry input (C_n). Sum outputs (Σ) are provided for each bit and the carry output (C_{n+1}) is obtained from the last bit. The high-speed internal serial carry circuitry used in the FJH211/7483 minimises the need for external "carry look ahead" logic when cascading adders for long word-length addition.

FUNCTION TABLE

To simplify the function table, it is presented in two parts:

Input conditions at A_0, A_1, B_0, B_1 and C_n determine the outputs Σ_0 and Σ_1 together with the internal carry (C_1) obtained from this addition.

Input conditions at A_2, A_3, B_2, B_3 and the internal carry C_1 determine the outputs Σ_2, Σ_3 and C_{n+1}.

INPUT				OUTPUT					
				C_n = L			C_n = H		
				C_1 = L			C_1 = H		
A_0 / A_2	B_0 / B_2	A_1 / A_3	B_1 / B_3	Σ_0 / Σ_2	Σ_1 / Σ_3	C_1 / C_{n+1}	Σ_0 / Σ_2	Σ_1 / Σ_3	C_1 / C_{n+1}
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	7.0	V
Output voltage	V_O	max.	5.5	V
D.C. input voltage	V_I	max.	5.5	V 1)
Peak negative input voltage	$-V_{IM}$	max.	2	V 2)
Operating ambient temperature	T_{amb}	0 to	+70	°C
Storage temperature	T_{stg}	−65 to	+150	°C

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references	
		0	25	70		V_P (V)	
STATIC DATA							
Voltages							
Input threshold LOW	V_{ILmax}	0.8	0.8	0.8	V		
Input threshold HIGH	V_{IHmin}	2.0	2.0	2.0	V		
Output LOW							
at Σ_0, Σ_1, Σ_2, Σ_3	V_{OLmax}	0.4	0.4	0.4	V	4.75	I_O = 16 mA
at C_{n+1}	V_{OLmax}	0.4	0.4	0.4	V	4.75	I_O = 8 mA
Output HIGH							
at Σ_0, Σ_1, Σ_2, Σ_3	V_{OHmin}	2.4	2.4	2.4	V	4.75	$-I_O$ = 400 µA
at C_{n+1}	V_{OHmin}	2.4	2.4	2.4	V	4.75	$-I_O$ = 200 µA
Currents							
Input LOW							
at A_0, A_2, B_0, B_2, C_n	$-I_{ILmax}$	6.4	6.4	6.4	mA	5.25	V_I = 0.4 V
at A_1, A_3, B_1, B_3	$-I_{ILmax}$	1.6	1.6	1.6	mA	5.25	V_I = 0.4 V
Input HIGH							
at A_0, A_2, B_0, B_2, C_n	I_{IHmax}	160	160	160	µA	5.25	V_I = 2.4 V
at A_1, A_3, B_1, B_3	I_{IHmax}	40	40	40	µA	5.25	V_I = 2.4 V
at all inputs	I_{IHmax}	1	1	1	mA	5.25	V_I = 5.5 V
Output LOW							
at Σ_0, Σ_1, Σ_2, Σ_3	I_{OLmax}	16	16	16	mA		
at C_{n+1}	I_{OLmax}	8	8	8	mA		

1) In addition, the voltage between any two inputs max. 5.5 V
2) Pulse duration t_p = 20 ns; repetition frequency f = 5 MHz; source resistance $R_S \geq 75\,\Omega$

CHARACTERISTICS (continued)

		T_{amb} (°C) 0	25	70		Conditions and references: V_P (V)	
STATIC DATA							
Output HIGH							
at Σ_0; Σ_1; Σ_2; Σ_3	$-I_{OHmax}$	400	400	400	μA		
at C_{n+1}	$-I_{OHmax}$	200	200	200	μA		
Output short-circuited [1]							
all outputs	$-I_{scmin}$	18	18	18	mA	5.25	
at Σ_0; Σ_1; Σ_2; Σ_3	$-I_{scmax}$	55	55	55	mA	5.25	
at C_{n+1}	$-I_{scmax}$	70	70	70	mA	5.25	
SUPPLY DATA							
Supply current	I_P typ	–	78	–	mA	5.0	
	I_P <	128	128	128	mA	5.25	
DYNAMIC DATA							
Rise propagation delay time							
$C_n \rightarrow \Sigma_0$	t_{pdr} <	–	34	–	ns	5.0	$N_a = 10$; $C_L = 15$ pF
$C_n \rightarrow \Sigma_1$	t_{pdr} <	–	38	–	ns	5.0	
$C_n \rightarrow \Sigma_2$	t_{pdr} <	–	50	–	ns	5.0	
$C_n \rightarrow \Sigma_3$	t_{pdr} <	–	55	–	ns	5.0	
$C_n \rightarrow C_{n+1}$	t_{pdr} typ	–	35	–	ns	5.0	$N_a = 5$; $C_L = 15$ pF
	t_{pdr} <	–	48	–	ns	5.0	
A_1; $B_1 \rightarrow \Sigma_1$	t_{pdr} <	–	40	–	ns	5.0	$N_a = 10$; $C_L = 15$ pF
A_3; $B_3 \rightarrow \Sigma_3$	t_{pdr} <	–	40	–	ns	5.0	
Fall propagation delay time							
$C_n \rightarrow \Sigma_0$	t_{pdf} <	–	40	–	ns	5.0	$N_a = 10$; $C_L = 15$ pF
$C_n \rightarrow \Sigma_1$	t_{pdf} <	–	42	–	ns	5.0	
$C_n \rightarrow \Sigma_2$	t_{pdf} <	–	60	–	ns	5.0	
$C_n \rightarrow \Sigma_3$	t_{pdf} <	–	55	–	ns	5.0	
$C_n \rightarrow C_{n+1}$	t_{pdf} typ	–	22	–	ns	5.0	$N_a = 5$; $C_L = 15$ pF
	t_{pdf} <	–	32	–	ns	5.0	
A_1; $B_1 \rightarrow \Sigma_1$	t_{pdf} <	–	35	–	ns	5.0	$N_a = 10$; $C_L = 15$ pF
A_3; $B_3 \rightarrow \Sigma_3$	t_{pdf} <	–	35	–	ns	5.0	

[1] Not more than one output must be shorted at a time

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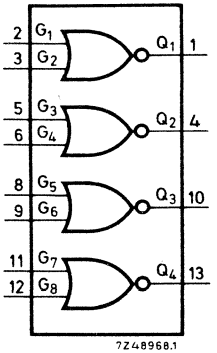
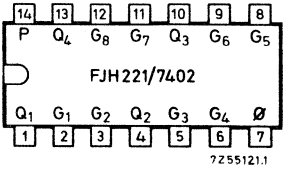
QUADRUPLE 2-INPUT NOR GATE

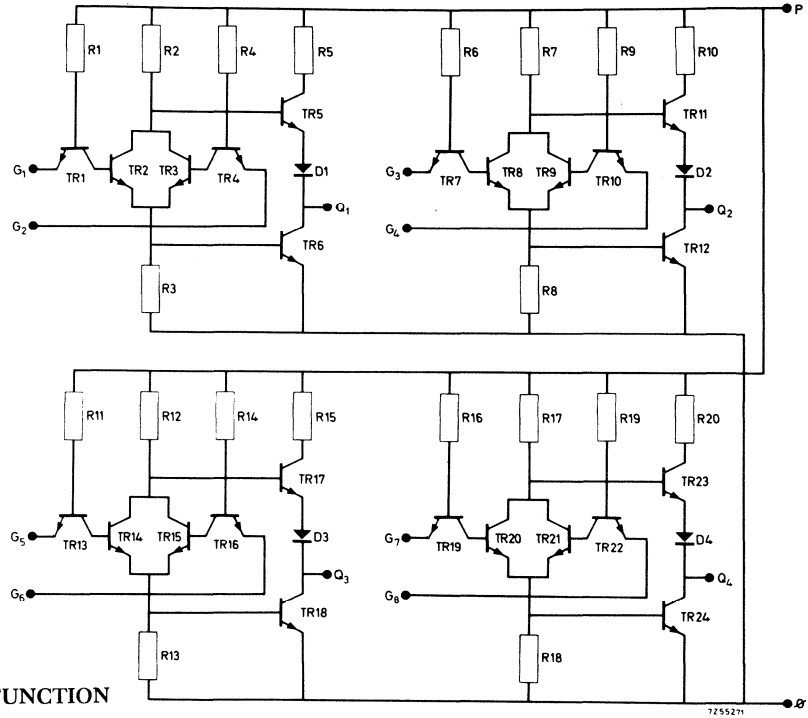




QUICK REFERENCE DATA			
Supply voltage	V_P	5.0 ±5%	V
Operating ambient temperature	T_{amb}	0 to +70	°C
Average propagation delay time N = fan-out = 10; T_{amb} = 25 °C	t_{pd}	typ. 10	ns
Available d.c. fan-out (full temperature range)	N_a	≥ 10	
D.C. noise margin (full temperature range)	M_L	> 0.4	V
Average power consumption (per gate) T_{amb} = 25 °C	P_{av}	typ. 14.25	mW

PACKAGE OUTLINE: 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAM



LOGIC FUNCTION

$Q_1 = \overline{G_1 + G_2}$ $\quad Q_3 = \overline{G_5 + G_6}$

$Q_2 = \overline{G_3 + G_4}$ $\quad Q_4 = \overline{G_7 + G_8}$

} for positive logic

Function table

$G_1;G_3$ $G_5;G_7$	$G_2;G_4$ $G_6;G_8$	$Q_1;Q_2$ $Q_3;Q_4$
L	L	H
L	H	L
H	L	L
H	H	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.	7.0	V
Output voltage	V_Q	max.	5.5	V
G input voltage	V_G	max.	5.5	V [1]
Peak negative G input voltage	$-V_{GM}$	max.	2	V [2]
Storage temperature	T_{stg}	-65 to	+150	°C
Operating ambient temperature	T_{amb}	0 to	+70	°C

[1] In addition, the voltage between any two inputs must not exceed 5.5 V.
[2] Pulse duration $t_p = 20$ ns; repetition frequency f = 5 MHz; source resistance $R_S \geq 75\,\Omega$.

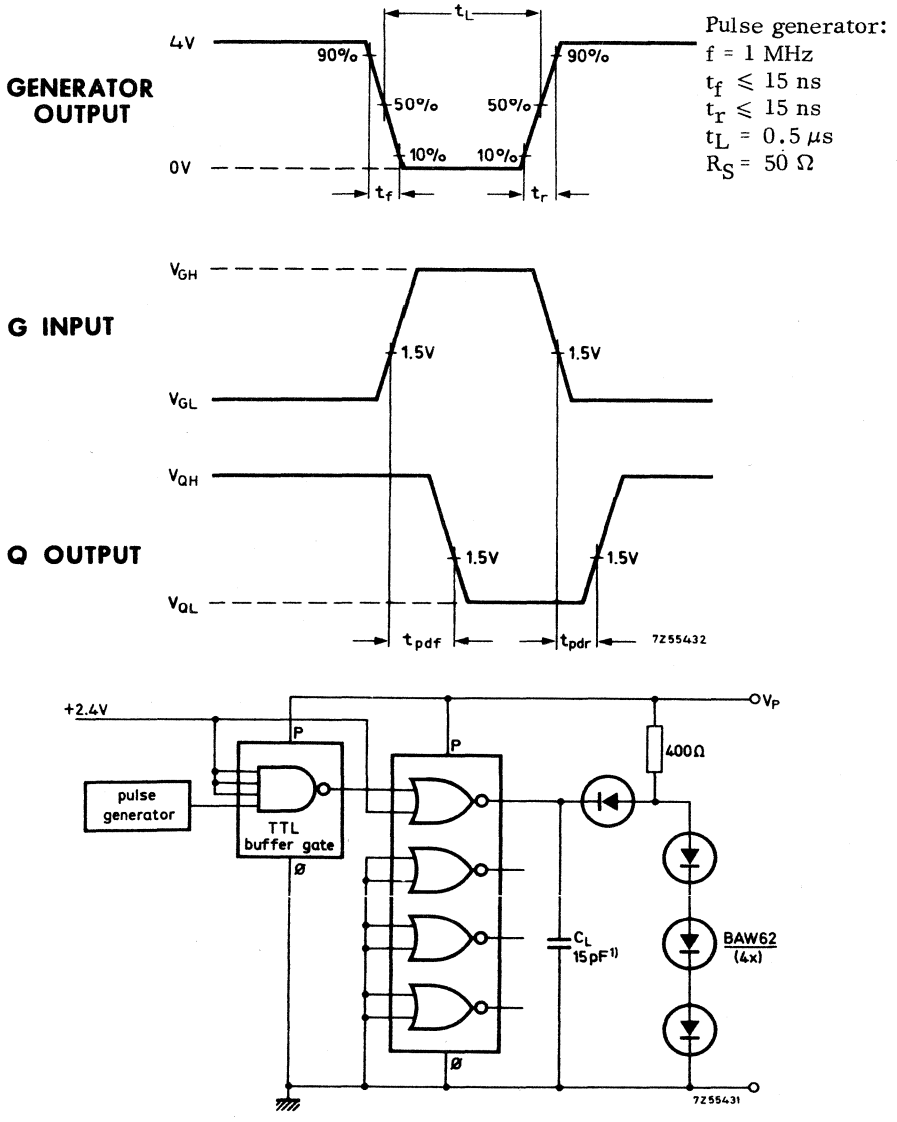
CHARACTERISTICS

			T_{amb} (°C)				Conditions and references	
			0	25	70		V_P (V)	
STATIC DATA								
Voltages								
Input threshold LOW	V_{GLmax}		0.8	0.8	0.8	V		
Input threshold HIGH	V_{GHmin}		2.0	2.0	2.0	V		
Output LOW	V_{QLmax}		0.4	0.4	0.4	V	4.75	$I_Q=I_{QLmax}$ $V_G=V_{GHmin}$
Output HIGH	V_{QHmin}		2.4	2.4	2.4	V	4.75	$-I_Q=-I_{QHmax}$; $V_G=V_{GLmax}$
Currents								
Input LOW	$-I_{GLmax}$		1.6	1.6	1.6	mA	5.25	$V_G=V_{QLmax}$; $I_Q=0$
Input HIGH	I_{GHmax}		40	40	40	μA	5.25	$V_G=V_{QHmin}$; $I_Q=0$ other inputs 0 V
Output LOW	I_{QLmax}		16	16	16	mA		
Output HIGH	$-I_{QHmax}$		0.4	0.4	0.4	mA		
Output short-circuited 1)	$-I_{Qsc\ min}$		18	18	18	mA	5.25	$V_Q=0$; $V_G=0$
	$-I_{Qsc\ max}$		55	55	55	mA		
SUPPLY DATA								
Supply current								
Output LOW	I_{PL}	typ.	-	14.8	-	mA	5.0	$V_G=5.0$ V; $I_Q=0$
		<	27	27	27	mA	5.25	
Output HIGH	I_{PH}	typ.	-	8.0	-	mA	5.0	$V_G=0$; $I_Q=0$
		<	16	16	16	mA	5.25	
DYNAMIC DATA								
Rise propagation delay time	t_{pdr}	typ.	-	12	-	ns	5.0	N = 10 one pair AND inputs at $V_G=0.4$ V
		<	-	22	-	ns	5.0	
Fall propagation delay time	t_{pdf}	typ.	-	8	-	ns	5.0	
		<	-	15	-	ns	5.0	

1) Not more than one output should be short circuited at a time.

CHARACTERISTICS (continued)

DYNAMIC DATA

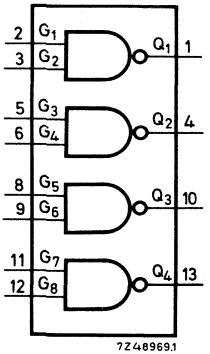


1) Including probe and jig capacitance

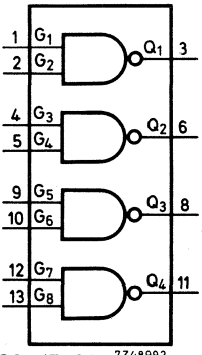
The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

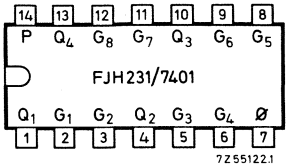
QUADRUPLE 2-INPUT NAND GATE

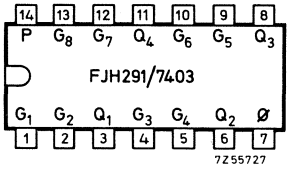


FJH231/7401



FJH291/7403



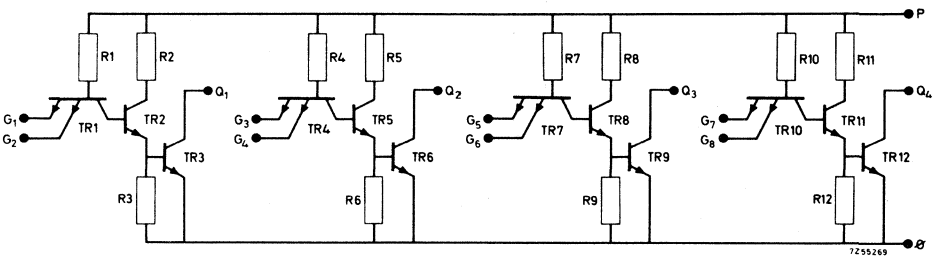


QUICK REFERENCE DATA			
Supply voltage	V_P	5.0 ± 5%	V
Operating ambient temperature	T_{amb}	0 to +70	°C
Average propagation delay time N = fan-out = 10; T_{amb} = 25 °C	t_{pd}	typ. 22	ns
Available d.c. fan-out (full temperature range)	N_a	≥ 10	
D.C. noise margin (full temperature range)	M_L	> 0.4 typ. 1.0	V V
Average power consumption (each gate) T_{amb} = 25 °C	P_{av}	typ. 10.0	mW

The FJH231/7401 and FJH291/7403 are quadruple 2-input NAND gates with open-collector output transistors for use in "wired-OR" connection with other gates of the FJ family.
The FJH291/7403 is pin-compatible with the FJH131/7400 NAND gate.

PACKAGE OUTLINE 14 lead plastic dual in-line (type A) (See general Section)

CIRCUIT DIAGRAM



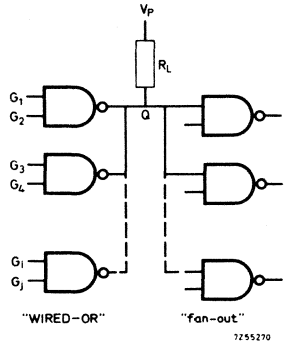
RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	7.0	V
D.C. output voltage (applied through $R_L \geq 270\ \Omega$)	V_Q	max.	7.0	V
G input voltage	V_G	max.	5.5	V [1]
Peak negative G input voltage	$-V_{GM}$	max.	2	V [2]
Storage temperature	T_{stg}	-65 to +150		°C
Operating ambient temperature	T_{amb}	0 to +70		°C

[1] In addition, the voltage between any two inputs must not exceed 5.5 V.
[2] Pulse duration t_p = 20 ms; repetition frequency f = 5 MHz; source resistance $R_S \geq 75\ \Omega$.

Fan-out and the "wired-OR" function

TTL gates with open collector can be connected to a common load resistor (R_L) to give a wired-OR function.
A gate alone will drive 10 TTL loads; when it is paralleled with other gates, it can drive from 1 to 9 loads.



To find the proper value of R_L, see application information on page 6.

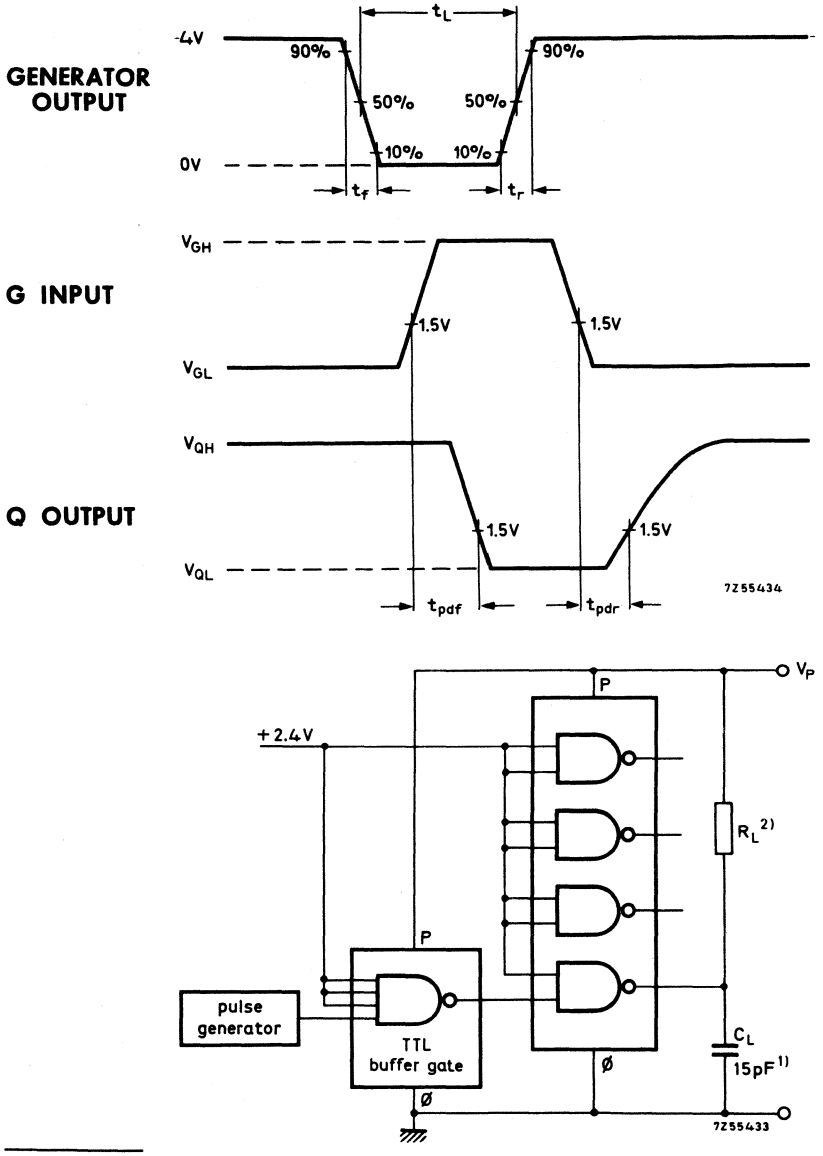
Wired-OR logic function (positive logic)

$$Q = \overline{G_1.G_2 + G_3.G_4 + \ldots\ldots + G_i.G_j}$$

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references	
		0	25	70		V_P (V)	
STATIC DATA							
Voltages							
Input threshold LOW	V_{GLmax}	0.8	0.8	0.8	V		
Input threshold HIGH	V_{GHmin}	2.0	2.0	2.0	V		
Output LOW	V_{QLmax}	0.4	0.4	0.4	V	4.75	$I_Q = I_{QLmax}$; $V_G = V_{GHmin}$
Output HIGH	V_{QHmin}	2.4	2.4	2.4	V	4.75	$-I_Q = -I_{QHmax}$; $V_G = V_{GLmax}$
Currents							
Input LOW	$-I_{GLmax}$	1.6	1.6	1.6	mA	5.25	$V_G = V_{QLmax}$; $I_Q = 0$
Input HIGH	I_{GHmax}	40	40	40	µA	5.25	$V_G = V_{QHmin}$; $I_Q = 0$ other inputs 0 V
Output LOW	I_{QLmax}	16	16	16	mA		
Output HIGH (reverse)	I_{QHmax}	250	250	250	µA	4.75	$V_G = V_{GLmax}$ $V_Q = 5.5$ V
SUPPLY DATA							
Supply current							
Output LOW	I_{PL} typ.	-	12	-	mA	5.0	$V_G = 5.0$ V; $I_Q = 0$
	I_{PL} <	22	22	22	mA	5.25	
Output HIGH	I_{PH} typ.	-	4.0	-	mA	5.0	$V_G = 0$; $I_Q = 0$
	I_{PH} <	8	8	8	mA	5.25	
DYNAMIC DATA							
Rise propagation delay time	t_{pdr} typ.	-	35	-	ns	5.0	$R_L = 3.9$ kΩ; $C_L = 15$ pF
	t_{pdr} <	-	45	-	ns	5.0	
Fall propagation delay time	t_{pdf} typ.	-	8	-	ns	5.0	$R_L = 390$ Ω; $C_L = 15$ pF
	t_{pdf} <	-	15	-	ns	5.0	

CHARACTERISTICS (continued)



1) Including probe and jig capacitance

2) R_L = 390 Ω for t_{pdf}
R_L = 3900 Ω for t_{pdr}

APPLICATION INFORMATION

Determining the value of R_L

Proper operation of the functions mentioned depends on the value of the common load resistor. The maximum value is set by the need to ensure sufficient load current to TTL loads and off current I_{QHmax} through paralleled outputs when the output is HIGH. A minimum value is set by the need to limit the total current through the resistor, including the "sink" current of the TTL loads, so that the output voltage does not rise above the LOW level, even when one of the paralleled outputs is absorbing all the current. The table shows minimum and maximum resistor values for up to 10 TTL loads and up to 7 gates connected in wired-OR.

Table I

fan-out to TTL loads	wired-OR outputs							
	1	2	3	4	5	6	7	1 to 7
1	8965	4814	3291	2500	2015	1688	1452	319
2	7878	4482	3132	2407	1954	1645	1420	359
3	7027	4193	2988	2321	1897	1604	1390	410
4	6341	3939	2857	2241	1843	1566	1361	479
5	5777	3714	2736	2166	1793	1529	1333	575
6	5306	3513	2626	2096	1744	1494	1306	718
7	4905	3333	2524	2031	1699	1460	1280	958
8	4561	3170	2429	1969	1656	X	X	1437
9	4262	3023	X	X	X	X	X	2875
10	4000	X	X	X	X	X	X	4000*
	maximum							min.
	load resistor values in ohms							

X = not recommended or not possible

* = the thoretical value is ∞

All values shown in the table are based on:

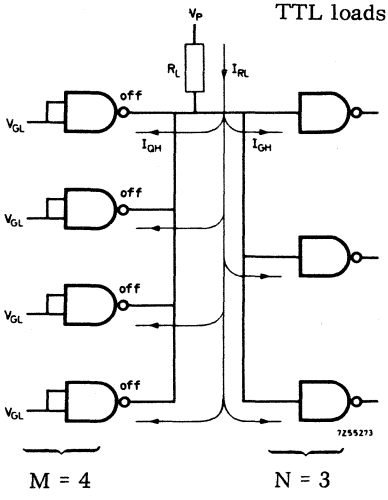
Logical HIGH conditions: V_P = 5 V; V_{QH} required = 2.4 V

Logical LOW conditions: V_P = 5 V; V_{QL} required = 0.4 V

APPLICATION INFORMATION (continued)

Circuit calculations

HIGH (off level) configurations (see figure below)



$M.I_{QH} = 4 \times 250\ \mu A$ $\quad N.I_{GH} = 3 \times 40\ \mu A$ $\quad R_{Lmax} = \dfrac{(5-2.4)V}{(0.001 + 0.00012)A} = 2321\ \Omega$

The allowable voltage drop across the load resistor (V_{RL}) is the difference between V_P applied and the output voltage V_{QH} required at the TTL load.

$$V_{RL} = V_P - V_{QHmin}$$

The total current through the load resistor (I_{RL}) is the sum of the load currents I_{GH} and off-level reverse current I_{QH} through each of the "wired-OR" connected outputs. Putting N as the number of TTL loads, and M as the number of outputs, the current is given by

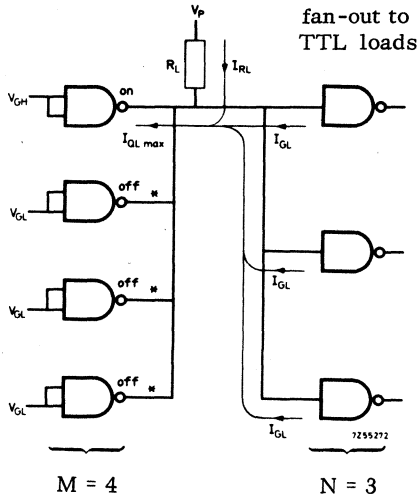
$$I_{RL} = M.I_{QH} + N.I_{GH}$$

Therefore, the maximum value of R_L is

$$R_{Lmax} = \frac{V_P - V_{QHmin}}{M.I_{QH} + N.I_{GH}}$$

APPLICATION INFORMATION (continued)

LOW (on level) configurations (see figure below)



I_{QLmax} = 16 mA N. $|I_{GLmax}|$ = 3 x 1.6 mA $R_{Lmin} = \frac{(5-0.4)V}{(0.016-0.0048)A} = 410\ \Omega$

*current through OFF outputs negligible at LOW output state

The current through the resistor must be limited to the maximum for one output transistor. If several outputs are "wired-OR" connected the current through R_L may be shared among the paralleled output transistors, but, unless it can be guaranteed that more than one transistor will be in the ON-(= conducting) state during the LOW output periods, the current must be limited to 16 mA, i.e. the maximum current that will still ensure a maximum LOW output voltage of 0.4 V.
The fan-out current must be considered as well. Part of the 16 mA will be supplied from the inputs being driven, which further reduces the current through R_L.
These considerations lead to the minimum value of R_L

$$R_{Lmin} = \frac{V_P - V_{QLmax}}{I_{QLmax} - N.|I_{GLmax}|}$$

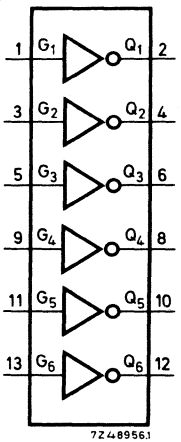
For up to 10 TTL loads and up to 7 "wired-OR" connected outputs table I gives the maximum and minimum values of R_L calculated in this way.
For a single output the values are determined by the fan-out plus the leakage current of one transistor.
More than 7 outputs can be connected in "wired-OR" provided valid maximum and minimum resistor values are possible.
The value of R_L for driving 10 loads should be infinite according to these calculations but 4 kΩ is sufficient to satisfy logic HIGH while keeping logic LOW to less than 0.43 V.

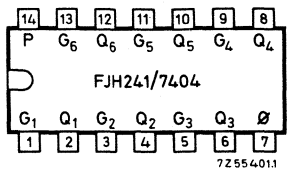
The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

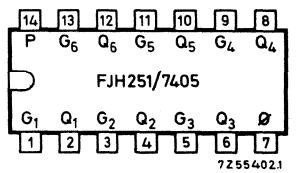
Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

SEXTUPLE SINGLE INPUT INVERTERS

Sextuple single input inverter with an active output (totem pole): FJH241/7404
Sextuple single input inverter with an open collector output: FJH251/7405







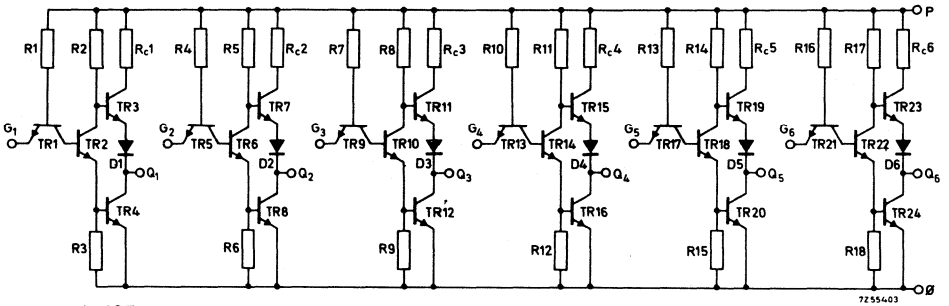
QUICK REFERENCE DATA			
Supply voltage	V_P	5.0 ± 5%	V
Operating ambient temperature	T_{amb}	0 to +70	°C
Average propagation delay time			
N = fan-out = 10; T_{amb} = 25 °C	FJH241/7404: t_{pd}	typ. 10	ns
	FJH251/7405: t_{pd}	typ. 24	ns
Available d.c. fan-out; full temperature range (for FJH251/7405 see table on page 5)	N_a	< 10	
D.C. noise margin (full temperature range)	M_L	> 0.4	V
		typ. 1.0	V
Average power consumption (each gate)			
T_{amb} = 25 °C	P_{av}	typ. 10	mW

The FJH241/7404 is a sextuple single-input inverter with an active output (totem pole). The FJH251/7405 is a sextuple single-input inverter with an open collector output transistor. It can be used in wired-OR connections with other gates of the FJ family.

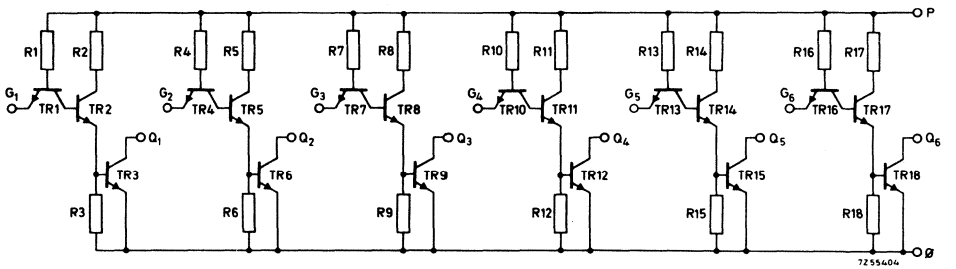
PACKAGE OUTLINE: 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAMS

FJH241/7404



FJH251/7405

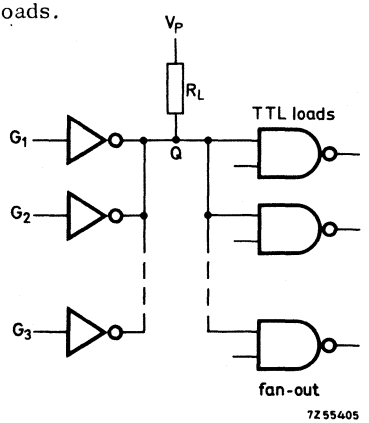


RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	7.0	V
G input voltage	V_G	max.	5.5	V
Peak negative G input voltage	$-V_{GM}$	max.	2	V [1]
Storage temperature	T_{stg}	-65 to	+150	°C
Operating ambient temperature	T_{amb}	0 to	+70	°C

Fan-out and "wired-OR" function of FJH251/7405

TTL inverters with open collector can be connected to a common load resistor (R_L) to give a wired-OR function.
An inverter alone will drive 10 TTL loads; when it is paralleled with other inverters it can drive from 1 to 9 TTL loads.



To find the proper value of R_L see application information on page 5.

Wired-OR logic function (positive logic)

$$Q = \overline{G_1 + G_2 + \ldots . G_i}$$

[1]) Pulse duration t_p = 20 ns; repetition frequency f = 5 MHz; source resistance $R_S \geq 75\ \Omega$.

CHARACTERISTICS

		T_{amb} (°C) 0	25	75	Conditions and References V_P (V)	
STATIC DATA						
Voltages						
Input threshold LOW	V_{GLmax}	0.8	0.8	0.8 V		
Input threshold HIGH	V_{GHmin}	2.0	2.0	2.0 V		
Output LOW	V_{QLmax}	0.4	0.4	0.4 V	4.75	$I_Q = I_{QLmax}$; $V_G = V_{GHmin}$
Output HIGH	V_{QHmin}	2.4	2.4	2.4 V	4.75	$-I_Q = -I_{QHmax}$; $V_G = V_{GLmax}$
Currents						
Input LOW	$-I_{GLmax}$	1.6	1.6	1.6 mA	5.25	$V_G = V_{QLmax}$; $I_Q = 0$
Input HIGH	I_{GHmax}	40	40	40 μA	5.25	$V_G = V_{QHmin}$; $I_Q = 0$
Output LOW	I_{QLmax}	16	16	16 mA		
Output HIGH FJH241/7404	$-I_{QHmax}$	400	400	400 μA	4.75	$V_Q = V_{QHmin}$
Output reverse HIGH; FJH251/7405	I_{QHmax}	250	250	250 μA	4.75	$V_G = V_{GLmax}$; $V_Q = 5.5$ V
Output short circuited FJH241/7404 See note 1	$-I_{Qscmin}$	18	18	18 mA	5.25	$V_G = 0$; $V_Q = 0$
	$-I_{Qscmax}$	55	55	55 mA	5.25	
SUPPLY DATA						
Output LOW	I_{PL} typ.	-	18	- mA	5.0	$V_G = 5$ V; $I_Q = 0$
	<	33	33	33 mA	5.25	
Output HIGH	I_{PH} typ.	-	6	- mA	5.0	$V_G = 0$; $I_Q = 0$
	<	12	12	12 mA	5.25	
DYNAMIC DATA						
Rise propagation delay time: FJH241/7404	t_{pdr} typ.	-	12	- ns	5.0	$R_L = 390\ \Omega$; $C_L = 15$ pF
	t_{pdr} <	-	22	- ns	5.0	
FJH251/7405	t_{pdr} typ.	-	40	- ns	5.0	$R_L = 3.9\ k\Omega$; $C_L = 15$ pF
	t_{pdr} <	-	55	- ns	5.0	
Fall propagation delay time	t_{pdf} typ.	-	8	- ns	5.0	$R_L = 390\ \Omega$; $C_L = 15$ pF
	t_{pdf} <	-	15	- ns	5.0	

Note 1: Not more than one output should be short circuited at a time

APPLICATION INFORMATION for FJH251/7405

Determining the value of R_L

Proper operation of the functions mentioned depends on the value of the common load resistor. The maximum value is set by the need to ensure sufficient load current to TTL loads and off current I_{QHmax} through paralleled outputs when the output is HIGH. A minimum value is set by the need to limit the total current through the resistor, including the "sink" current of the TTL loads, so that the output voltage does not rise above the LOW level, even when one of the paralleled outputs is absorbing all the current. The table shows minimum and maximum resistor values for up to 10 TTL loads and up to 7 gates connected in wired-OR.

Table I

fan-out to TTL loads	wired-OR outputs							
	1	2	3	4	5	6	7	1 to 7
1	8965	4814	3291	2500	2015	1688	1452	319
2	7878	4482	3132	2407	1954	1645	1420	359
3	7027	4193	2988	2321	1897	1604	1390	410
4	6341	3939	2857	2241	1843	1566	1361	479
5	5777	3714	2736	2166	1793	1529	1333	575
6	5306	3513	2626	2096	1744	1494	1306	718
7	4905	3333	2524	2031	1699	1460	1280	958
8	4561	3170	2429	1969	1656	X	X	1437
9	4262	3023	X	X	X	X	X	2875
10	4000	X	X	X	X	X	X	4000*
	maximum							min.
	load resistor values in ohms							

X = not recommended or not possible

* = the theoretical value is ∞

All values shown in the table are based on:

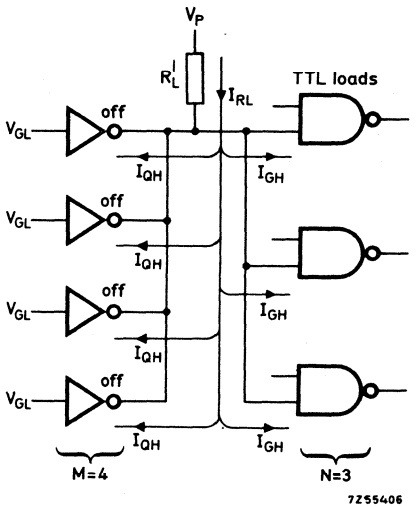
Logical HIGH conditions: V_P = 5 V; V_{QH} required = 2.4 V

Logical LOW conditions: V_P = 5 V; V_{QL} required = 0.4 V

APPLICATION INFORMATION (continued)

Circuit calculations

HIGH (off level) configurations (see figure below)



$M.I_{QH} = 4 \times 250\ \mu A$ $\quad N.I_{GH} = 3 \times 40\ \mu A$ $\quad R_{Lmax} = \dfrac{(5-2.4)V}{(0.001 + 0.00012)A} = 2321\ \Omega$

The allowable voltage drop across the load resistor (V_{RL}) is the difference between V_P applied and the output voltage V_{QH} required at the TTL load.

$$V_{RL} = V_P - V_{QHmin}$$

The total current through the load resistor (I_{RL}) is the sum of the load currents I_{GH} and off-level reverse current I_{QH} through each of the "wired-OR" connected outputs. Putting N as the number of TTL loads, and M as the number of outputs, the current is given by

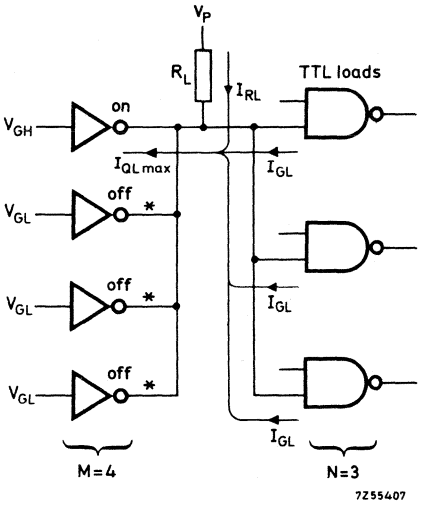
$$I_{RL} = M.I_{QH} + N.I_{GH}$$

Therefore, the maximum value of R_L is

$$R_{Lmax} = \frac{V_P - V_{QHmin}}{M.I_{QH} + N.I_{GH}}$$

APPLICATION INFORMATION (continued)

LOW (on level) configurations (see figure below)



I_{QLmax} = 16 mA N. $|I_{GLmax}|$ = 3 x 1.6 mA $R_{Lmin} = \frac{(5-0.4)V}{(0.016-0.0048)A} = 410\ \Omega$

*current through OFF outputs negligible at LOW output state

The current through the resistor must be limited to the maximum for one output transistor. If several outputs are "wired-OR" connected the current through R_L may be shared among the paralleled output transistor, but, unless it can be guaranteed that more than one transistor will be in the ON-(= conducting) state during the LOW output periods, the current must be limited to 16 mA, i.e. the maximum current that will still ensure a maximum LOW output voltage of 0.4 V.
The fan-out current must be considered as well. Part of the 16 mA will be supplied from the inputs being driven, which further reduces the current through R_L;
These considerations lead to the minimum value of R_L

$$R_{Lmin} = \frac{V_P - V_{QLmax}}{I_{QLmax} - N.|I_{GLmax}|}$$

For up to 10 TTL loads and up to 7 "wired-OR" connected outputs table I gives the maximum and minimum values of R_L calculated in this way.
For a single output the values are determined by the fan-out plus the leakage current of one transistor.
More than 7 outputs can be connected in "wired-OR" provided valid maximum and minimum resistor values are possible.
The value of R_L for driving 10 loads should be infinite according to these calculations but 4 kΩ is sufficient to satisfy logic HIGH while keeping logic LOW to less than 0.43 V.

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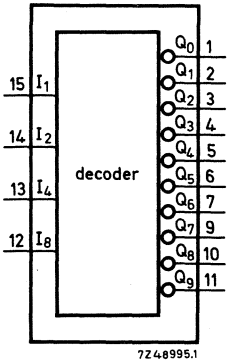
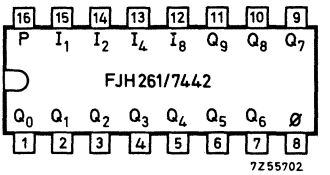
BCD-to-DECIMAL DECODER





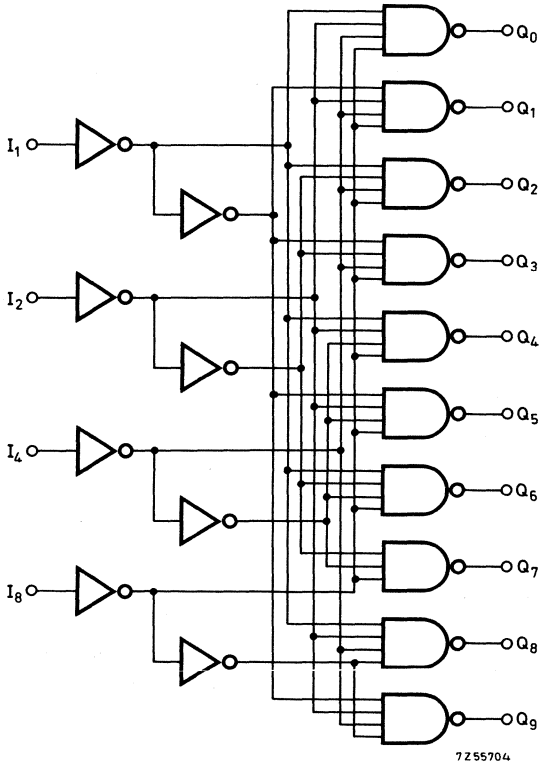
QUICK REFERENCE DATA			
Supply voltage	V_P	5 ±5%	V
Operating ambient temperature	T_{amb}	0 to +70	°C
Available d.c. fan-out (each output)	N_a	≥ 10	
Average propagation delay	t_{pd}	typ. 20	ns
Average power consumption	P_{av}	typ. 140	mW

PACKAGE OUTLINE 16 lead plastic dual in-line (type A) (See General Section)

GENERAL DESCRIPTION

The FJH261/7442 is a multipurpose decoder which accepts four BCD (8-4-2-1 code) inputs and provides ten mutually exclusive outputs.
The active LOW outputs facilitate addressing functions when inverting drivers are used. Full decoding of valid input logic ensures that all outputs remain HIGH (off) for input binary codes greater than nine.
The most significant input (I_8) provides a useful inhibit function when the FJH261/7442 is used as a 1-of-8 decoder, as shown in the APPLICATION INFORMATION section on page 6.

LOGIC DIAGRAM



FUNCTION TABLE

inputs				outputs									
I_8	I_4	I_2	I_1	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8	Q_9
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH (the more positive voltage)
L = LOW (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	7	V
Input voltage (d.c.)	V_I	max.	5.5	V [1]
Negative transient input voltage (t_p = 20 ns; f = 5 MHz, $R_S \geq 75\ \Omega$)	$-V_{IM}$	max.	2	V
Operating ambient temperature	T_{amb}	0 to	+70	°C
Storage temperature	T_{stg}	−65 to	+150	°C

[1]) In addition, the voltage between any two inputs must not exceed 5.5 V.

CHARACTERISTICS

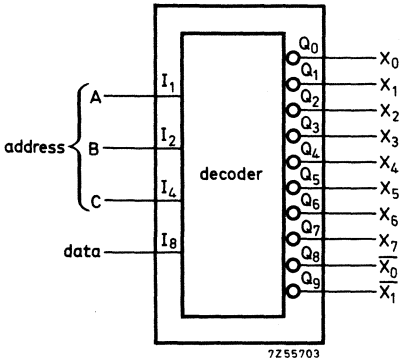
		T_{amb} (°C)				Conditions and references	
		0	25	70		V_P (V)	
STATIC DATA							
Voltages							
Input threshold LOW	V_{ILmax}	0.8	0.8	0.8	V		
Input threshold HIGH	V_{IHmin}	2.0	2.0	2.0	V		
Output LOW	V_{QLmax}	0.4	0.4	0.4	V	4.75	$I_Q = I_{QLmax}$
Output HIGH	V_{QHmin}	2.4	2.4	2.4	V	4.75	$-I_Q = -I_{QHmax}$
Currents							
Input LOW (each input)	$-I_{ILmax}$	1.6	1.6	1.6	mA	5.25	$V_I = 0.4$ V
Input HIGH (each input)	I_{IHmax}	40	40	40	µA	5.25	$V_I = 2.4$ V
	I_{IHmax}	1	1	1	mA	5.25	$V_I = 5.5$ V
Output LOW	I_{QLmax}	16	16	16	mA		$V_Q = V_{QLmax}$
Output HIGH	$-I_{QHmax}$	400	400	400	µA		$V_Q = V_{QHmin}$
Output short circuited [1]	$-I_{Qsc\ min}$	18	18	18	mA	5.25	
	$-I_{Qsc\ max}$	55	55	55	mA	5.25	
SUPPLY DATA							
Supply current	I_P typ.	–	28	–	mA	5.0	$V_I = 0$ V
	$I_P \leq$	56	56	56	mA	5.25	$V_I = 0$ V
DYNAMIC DATA		min.	typ.	max.			
Propagation delay times							
Rise: through two logic levels	t_{pdr}	10	17	25	ns	5.0	$C_L = 15$ pF, $N = 10$, $T_{amb} = 25$ °C
through three logic levels	t_{pdr}	–	26	35	ns	5.0	$C_L = 15$ pF, $N = 10$, $T_{amb} = 25$ °C
Fall: through two logic levels	t_{pdf}	10	22	30	ns	5.0	$C_L = 15$ pF, $N = 10$, $T_{amb} = 25$ °C
through three logic levels	t_{pdf}	–	23	35	ns	5.0	$C_L = 15$ pF, $N = 10$, $T_{amb} = 25$ °C

[1]) Only one output to be shorted at a time.

APPLICATION INFORMATION

Digital demultiplexer

Data may be routed from a single source to any of 8 outputs by addressing that output. All other outputs remain HIGH. Complements of outputs Q_0 and Q_1 are available at Q_8 and Q_9 respectively.

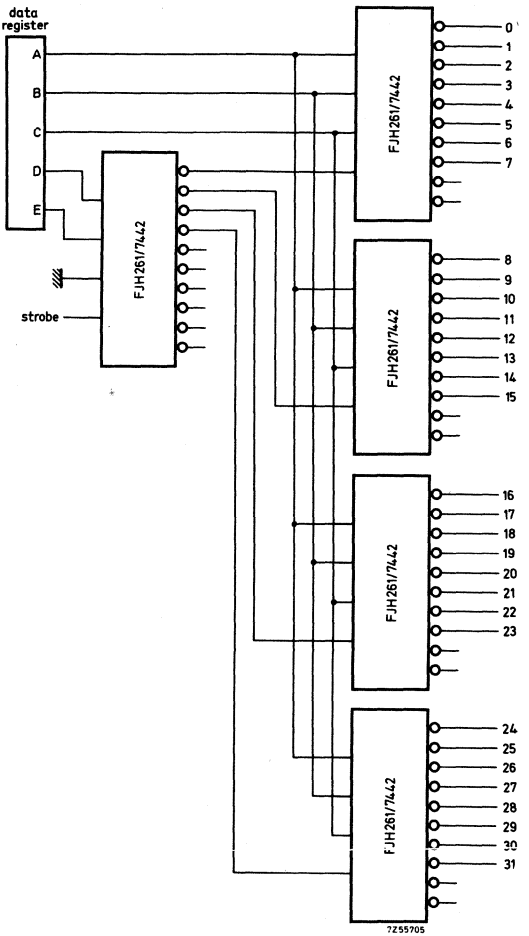


address			output
A	B	C	line
L	L	L	X_0
H	L	L	X_1
L	H	L	X_2
H	H	L	X_3
L	L	H	X_4
H	L	H	X_5
L	H	H	X_6
H	H	H	X_7

APPLICATION INFORMATION (continued)

1-of-32 decoding

The general purpose nature of the FJH261/7442 is shown by this application, where the most significant input (I_8) is used as an inhibit in the four 1-of-8 decoders.



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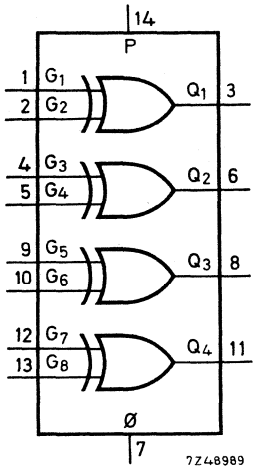
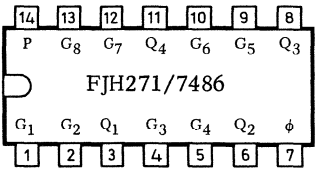
QUADRUPLE 2-INPUT EXCLUSIVE-OR GATE



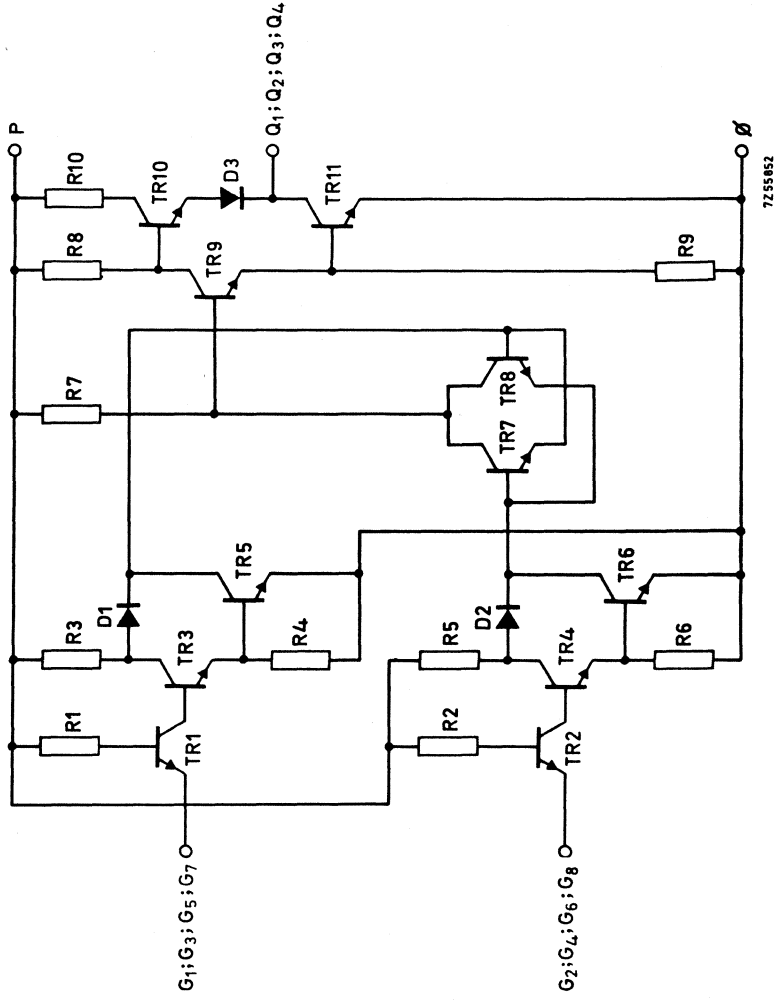


QUICK REFERENCE DATA				
Supply voltage	V_P		5.0 ± 5 %	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Average propagation delay time N = fan-out = 10; T_{amb} = 25 °C	t_{pd}	typ.	12	ns
Available d.c. fan-out (full temperature range)	N_{aL}	≥	10	1)
D.C. noise margin (full temperature range)	M_L	>	0.4	V
		typ.	1.0	V
Average power consumption (per gate) T_{amb} = 25 °C	P_{av}	typ.	37.5	mW

1) $N_{aH} \geq 20$

PACKAGE OUTLINE : 14 lead plastic dual in-line (type A) **(See General Section).**

CIRCUIT DIAGRAM



LOGIC FUNCTION

$Q_1 = G_1 \cdot \bar{G}_2 + \bar{G}_1 \cdot G_2$

Function table

G_1; G_3 G_5; G_7	G_2; G_4 G_6; G_8	Q_1; Q_2 Q_3; Q_4
L	L	L
H	L	H
L	H	H
H	H	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134).

Supply voltage	V_P	max.	7.0	V
Output voltage	V_Q	max.	5.5	V
G-input voltage	V_G	max.	5.5	V [1]
Peak negative G-input voltage	$-V_{GM}$	max.	2	V [2]
Storage temperature	T_{stg}	−65 to +150		°C
Operating ambient temperature	T_{amb}	0 to +70		°C

[1] In addition, the voltage between any two inputs must not exceed 5.5 V.
[2] Pulse duration t_p = 20 ns; repetition frequency f = 5 MHz; source resistance $R_S \geq 75\ \Omega$.

CHARACTERISTICS

			T_{amb} (°C)				Conditions and references
			0	25	70	V_P (V)	
STATIC DATA							
Voltages							
Input threshold LOW	V_{GL} max		0.8	0.8	0.8 V		
Input threshold HIGH	V_{GH} min		2.0	2.0	2.0 V		
Output LOW	V_{QL} max		0.4	0.4	0.4 V	4.75	$I_Q = I_{QL}$ max; $V_G = V_{GH}$ min or V_{GL} max (both inputs)
Output HIGH	V_{QH} min		2.4	2.4	2.4 V	4.75	$-I_Q = -I_{QH}$ max; $V_{G1} = V_{GL}$ max; $V_{G2} = V_{GH}$min
Currents							
Input LOW	$-I_{GL}$ max		1.6	1.6	1.6 mA	5.25	$V_G = V_{QL}$ max; $I_Q = 0$
Input HIGH	I_{GH} max		40	40	40 μA	5.25	$V_G = V_{QH}$min; $I_Q = 0$
Output LOW	I_{GH} max I_{QL} max		1 16	1 16	1 mA 16 mA		V_G = 5.5 V
Output HIGH	$-I_{QH}$ max		0.8	0.8	0.8 mA		
Output short-circuited	$-I_{Qsc}$ min $-I_{Qsc}$ max		18 55	18 55	18 mA 55 mA	5.25	$V_Q = 0$; $V_{G1} = V_{QL}$max; V_{G2} = 4.5 V
SUPPLY DATA							
Supply current	I_P	typ. <	– 50	30 50	– mA 50 mA	5.0 5.25	$V_{G1} = V_{G2}$ = 4.5 V; $I_Q = 0$
DYNAMIC DATA							
Rise propagation delay time (other input LOW)	t_{pdr} t_{pdr}	typ. <	– –	15 23	– ns – ns	5.0	R_L = 400 Ω; C_L = 15 pF
Rise propagation delay time (other input HIGH)	t_{pdr} t_{pdr}	typ. <	– –	18 30	– ns – ns	5.0	R_L = 400 Ω; C_L = 15 pF
Fall propagation delay time (other input LOW)	t_{pdf} t_{pdf}	typ. <	– –	11 17	– ns – ns	5.0	R_L = 400 Ω; C_L = 15 pF
Fall propagation delay time (other input HIGH)	t_{pdf} t_{pdf}	typ. <	– –	13 22	– ns – ns	5.0	R_L = 400 Ω; C_L = 15 pF

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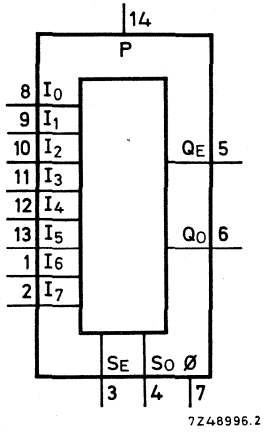
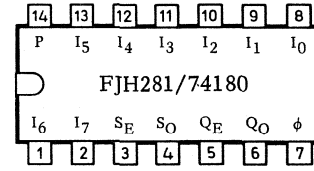
8-BIT ODD/EVEN PARITY GENERATOR/CHECKER

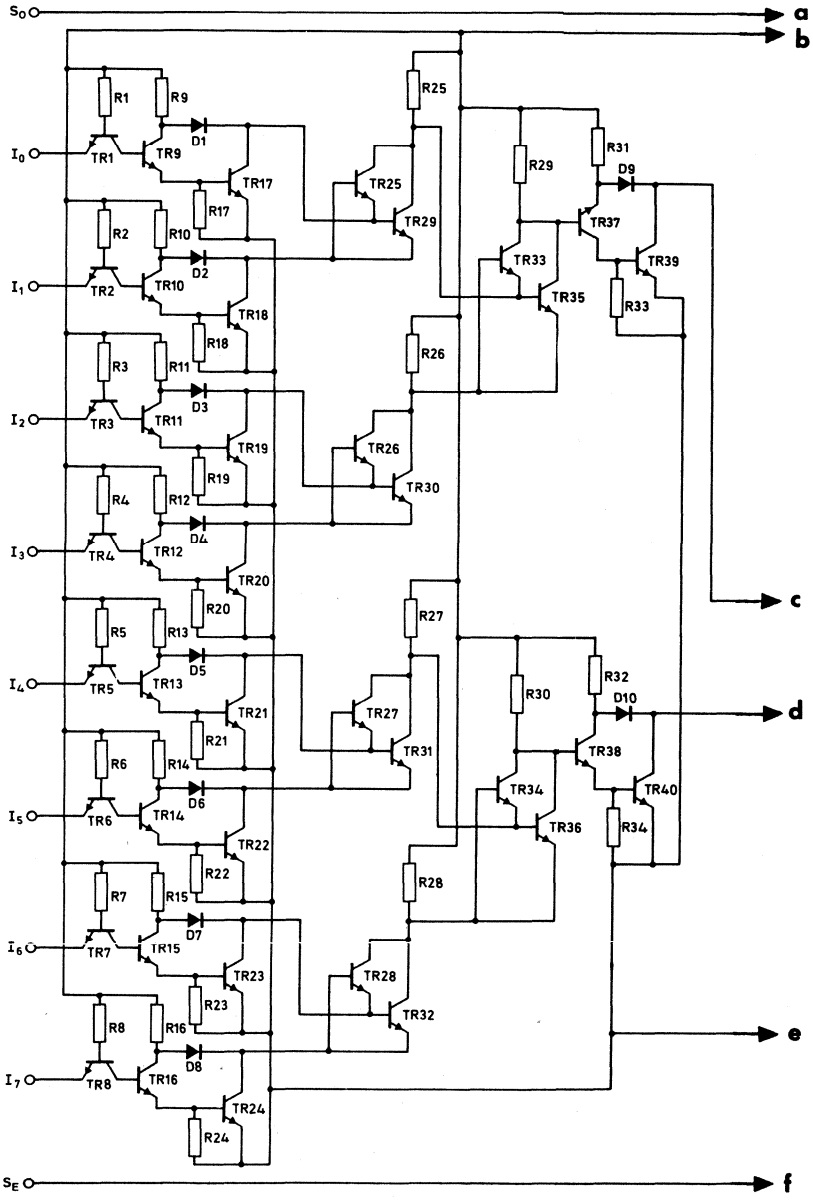




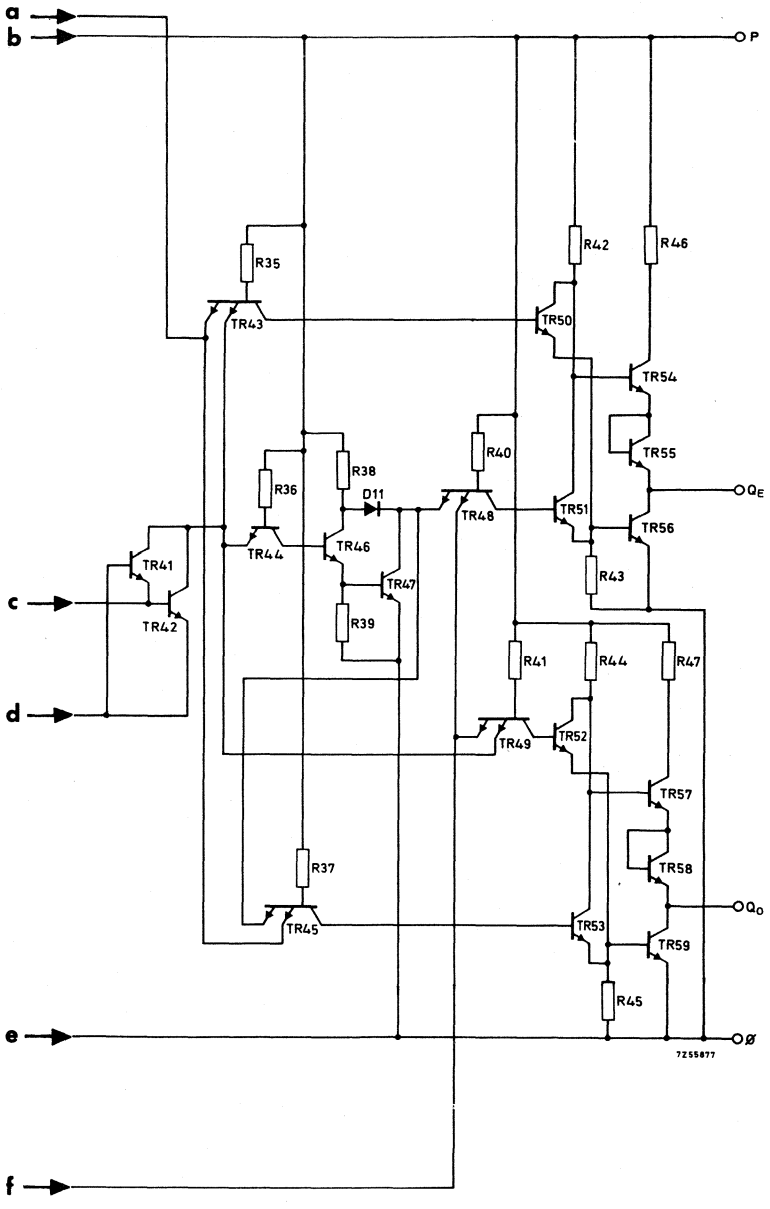
QUICK REFERENCE DATA				
Supply voltage	V_P		5.0 ±5%	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Available d.c. fan-out: LOW state	N_a	≥	10	
HIGH state	N_a	≥	20	
D.C. noise margin (full temperature range)	M_L	>	0.4	V
		typ.	1.0	V
Average power consumption (duty cycle 50 %; T_{amb} = 25 °C)	P_{av}	typ.	170	mW

PACKAGE OUTLINE : 14 lead plastic dual in-line (type A) (See General Section).

CIRCUIT DIAGRAM



CIRCUIT DIAGRAM (continued)



GENERAL DESCRIPTION

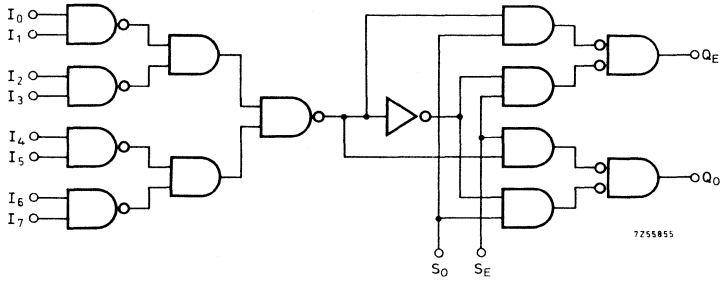
These devices feature odd/even outputs and control inputs to facilitate operation in either odd-or even- parity applications. The word length capability is easily expanded by cascading. Input buffers are provided so that each data input represents only one normalised load. A full fan-out to 10 normalised loads is available from each of the outputs in the LOW state. A fan-out of 20 normalised loads is provided in the HIGH state to facilitate the connection of unused inputs to used inputs.

FUNCTION TABLE

Inputs			Outputs	
I_0 to I_7 HIGH state	S_E	S_O	Q_E	Q_O
even	H	L	H	L
odd	H	L	L	H
even	L	H	L	H
odd	L	H	H	L
x	H	H	L	L
x	L	L	H	H

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

LOGIC DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.	7.0	V
Input voltages (all inputs)				
	V_I	max.	5.5	V
Peak negative input voltages	$-V_{IM}$	max.	2.0	V [1]
Storage temperature	T_{stg}	−65 to	+150	°C
Operating ambient temperature	T_{amb}	0 to	+70	°C

[1]) Pulse duration t_p = 20 ns; repetition frequency f = 5 MHz; source resistance $R_S \geq 75\Omega$.

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references	
		0	25	70		V_P (V)	
STATIC DATA							
Voltages							
Input threshold LOW	V_{ILmax}	0.8	0.8	0.8	V		
Input threshold HIGH	V_{IHmin}	2.0	2.0	2.0	V		
Output LOW	V_{QLmax}	0.4	0.4	0.4	V	4.75	$I_Q = I_{QLmax}$
Output HIGH	V_{QHmin}	2.4	2.4	2.4	V	4.75	$-I_Q = -I_{QHmax}$
Currents							
Input LOW (data input)	$-I_{ILmax}$	1.6	1.6	1.6	mA	5.25	$V_I = V_{QLmax}$
(odd or even input)	$-I_{ILmax}$	3.2	3.2	3.2	mA	5.25	$V_I = V_{QLmax}$
Input HIGH (data input)	I_{IHmax}	40	40	40	µA	5.25	$V_I = V_{QHmin}$
(odd or even input)	I_{IHmax}	80	80	80	µA	5.25	$V_I = V_{QHmin}$
(all inputs)	I_{IHmax}	1	1	1	mA	5.25	$V_I = 5.5$ V
Output LOW	I_{QLmax}	16	16	16	mA		
Output HIGH	$-I_{QHmax}$	0.8	0.8	0.8	mA		
Output short circuited	$-I_{Qsc\ min}$	18	18	18	mA	5.25	$V_I = 0; V_Q = 0$
	$-I_{Qsc\ max}$	55	55	55	mA	5.25	$V_I = 0; V_Q = 0$
SUPPLY DATA							
Supply current	I_P typ.	-	34	-	mA	5.0	
	I_P <	56	56	56	mA	5.25	

CHARACTERISTICS (continued)

			T_{amb} (°C) 0	25	70		V_P (V)	Conditions and references $C_L = 15\,pF; R_L = 400\,\Omega$
DYNAMIC DATA								
Rise propagation delay times								
I → Q_E	t_{pdr}	typ.	–	40	–	ns	5.0	S_E = 0 V; S_O = 5 V
		<	–	60	–	ns	5.0	
I → Q_O	t_{pdr}	typ.	–	32	–	ns	5.0	S_E = 0 V; S_O = 5 V
		<	–	48	–	ns	5.0	
I → Q_E	t_{pdr}	typ.	–	32	–	ns	5.0	S_E = 5 V; S_O = 0 V
		<	–	48	–	ns	5.0	
I → Q_O	t_{pdr}	typ.	–	40	–	ns	5.0	S_E = 5 V; S_O = 0 V
		<	–	60	–	ns	5.0	
S_E → Q_E S_O → Q_O	t_{pdr}	typ.	–	13	–	ns	5.0	all inputs 5.0 V; see also note 1
		<	–	20	–	ns	5.0	
Fall propagation delay times								
I → Q_E	t_{pdf}	typ.	–	25	–	ns	5.0	S_E = 0 V; S_O = 5 V
		<	–	38	–	ns	5.0	
I → Q_O	t_{pdf}	typ.	–	45	–	ns	5.0	S_E = 0 V; S_O = 5 V
		<	–	68	–	ns	5.0	
I → Q_E	t_{pdf}	typ.	–	45	–	ns	5.0	S_E = 5 V; S_O = 0 V
		<	–	68	–	ns	5.0	
I → Q_O	t_{pdf}	typ.	–	25	–	ns	5.0	S_E = 5 V; S_O = 0 V
		<	–	38	–	ns	5.0	
S_E → Q_E S_O → Q_O	t_{pdf}	typ.	–	7	–	ns	5.0	all inputs 5.0 V; see also note 2
		<	–	10	–	ns	5.0	

Note 1:

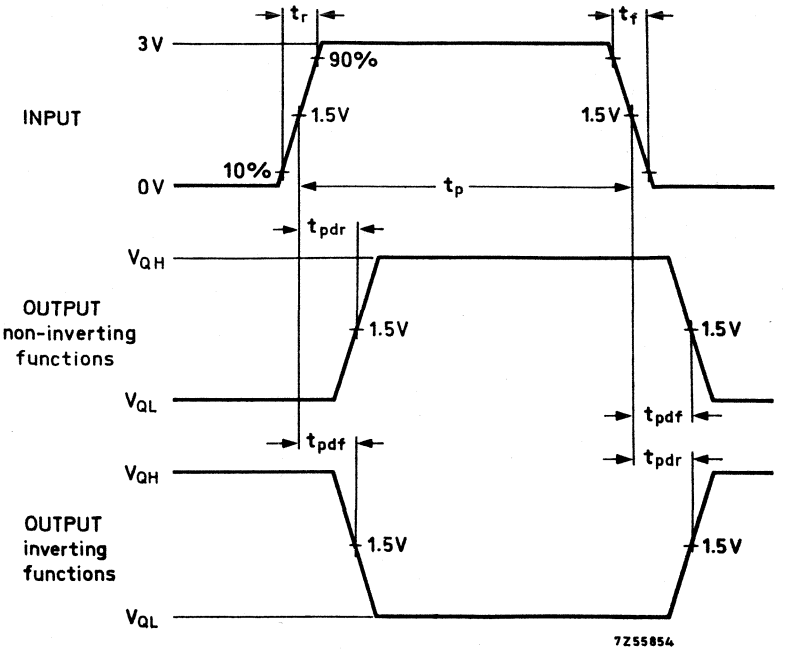
S_E → Q_O S_O → Q_E	t_{pdr}	typ. <	13 20	all inputs 5.0 V except S_O = 0 V

Note 2:

S_E → Q_O S_O → Q_E	t_{pdf}	typ. <	7 10	all inputs 5.0 V except S_O = 0 V

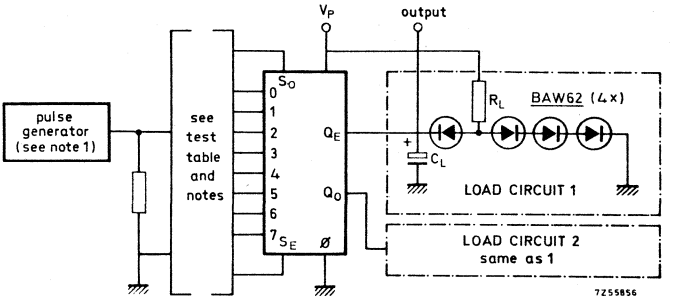
CHARACTERISTICS (continued)

DYNAMIC DATA



Pulse generator:

$t_r = t_f = 10$ ns
$t_p = 500$ ns
$f = 1$ MHz
$R_S = 50\ \Omega$



Notes:

1. C_L includes probe and jig capacitance.
2. t_{pdr} and t_{pdf} are tested for each condition shown.
3. for test table see page 8.

CHARACTERISTICS (continued)

Test No.	Input conditions		Output tested (see note 2)
	Pulse	earth (ϕ) [1]	
1	0	ODD	Q_E
2	1	ODD	Q_E
3	2	ODD	Q_E
4	3	ODD	Q_E
5	4	ODD	Q_E
6	5	ODD	Q_E
7	6	ODD	Q_E
8	7	ODD	Q_E
9	0	ODD	Q_O
10	1	ODD	Q_O
11	2	ODD	Q_O
12	3	ODD	Q_O
13	4	ODD	Q_O
14	5	ODD	Q_O
15	6	ODD	Q_O
16	7	ODD	Q_O
17	EVEN	None	Q_E
18	ODD	0	Q_E
19	EVEN	0	Q_O
20	ODD	None	Q_O

[1]) Tests 1 to 16 to be repeated with EVEN at earth (ϕ).

QUADRUPLE 2-INPUT NAND GATE

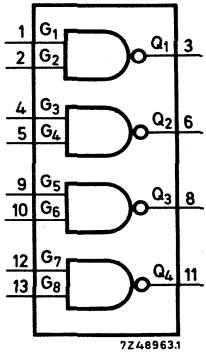
For data of this type please refer to FJH231/7401

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

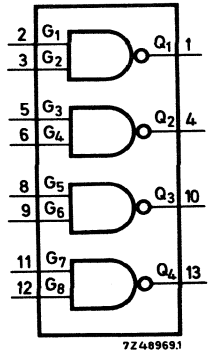
Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

NAND GATES

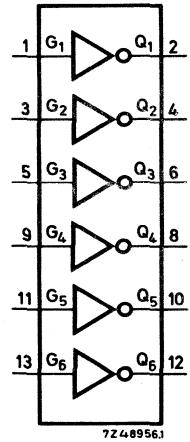
Quadruple 2-input NAND gate, with open collector — FJH301/7426
Quadruple 2-input NAND gate, with open collector — FJH311/7401-S1
Sextuple single input inverter, with open collector — FJH321/7405-S1



FJH301/7426



FJH311/7401-S1



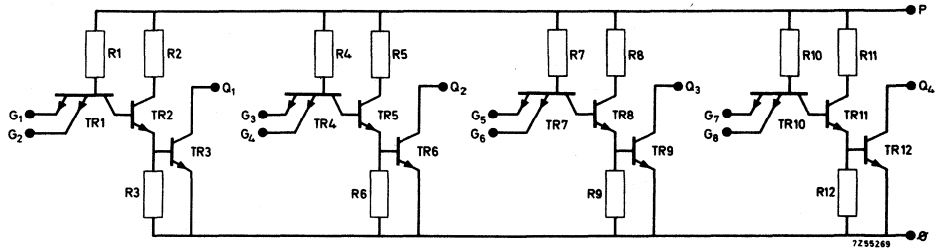
FJH321/7405-S1

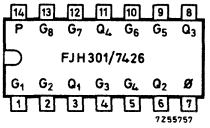
QUICK REFERENCE DATA				
Supply voltage	V_P	5.0 ± 5%		V
Operating ambient temperature	T_{amb}	0 to +70		°C
Output voltage	V_Q	max.	15	V
Average propagation delay				
N = fan-out = 10; T_{amb} = 25 °C	t_{pd}	max.	30	ns
Available d.c. fan-out (full temperature range)	N_a	≥	10	
D.C. noise margin (full temperature range)	M_L	>	0.4	V
		typ.	1.0	V
Average power consumption at T_{amb} = 25 °C (per gate)	P_{av}	typ.	10	mW

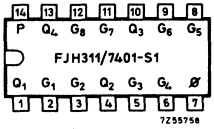
PACKAGE OUTLINE : 14 lead plastic dual in-line (type A) See General Section

CIRCUIT DIAGRAMS

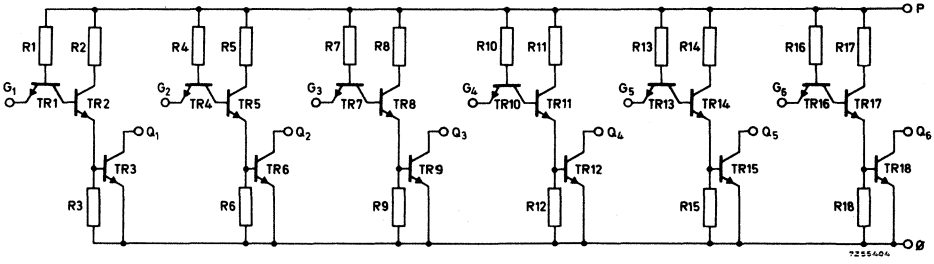
FJH301/7426 and FJH311/7401-S1

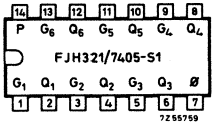






FJH321/7405-S1





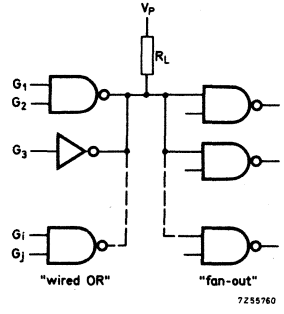
This series of open-collector NAND gates features 15 V output voltage ratings and is intended to be used for interfacing with MOS logic or as open-collector drivers for indicator lamps and relays.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	7.0	V
D.C. output voltage	V_Q	max.	15	V
D.C. input voltage	V_G	max.	5.5	V [1]
Peak negative input voltage	$-V_{GM}$	max.	2	V [2]
Storage temperature	T_{stg}	−65 to	+150	°C
Operating ambient temperature	T_{amb}	0 to	+70	°C

Fan-out and the "wired-OR" function

TTL gates with open collector can be connected to a common load resistor (R_L) to give a wired-OR function.
A gate alone will drive 10 TTL loads; when it is paralleled with other gates, it can drive from 1 to 9 loads.



To find the proper value of R_L, see application information on page 6.

Wired-OR logic function (positive logic)

$$Q = \overline{G_1 \cdot G_2 + G_3 + \ldots\ldots\ldots + G_i \cdot G_j}$$

1) In addition, the voltage between any two inputs must not exceed 5.5 V
2) Pulse duration t_p = 20 ns; repetition frequency f = 5 MHz; source resistance $R_S \geq 75\ \Omega$

CHARACTERISTICS

		T_{amb} (°C)				Conditions and References	
		0	25	70		V_P (V)	
STATIC DATA							
Voltages							
Input threshold LOW	V_{GLmax}	0.8	0.8	0.8	V		
Input threshold HIGH	V_{GHmin}	2.0	2.0	2.0	V		
Output LOW	V_{QLmax}	0.4	0.4	0.4	V	4.75	$I_Q = I_{QLmax}$; $V_G = V_{GHmin}$
Output HIGH [1]	V_{QHmin}	15	15	15	V	4.75	I_{QH} = 1 mA; $V_G = V_{GLmax}$
Currents							
Input LOW	$-I_{GLmax}$	1.6	1.6	1.6	mA	5.25	$V_G = V_{QLmax}$; $I_Q = 0$
Input HIGH	I_{GHmax}	40	40	40	µA	5.25	V_G = 2.4 V; $I_Q = 0$
Output LOW	I_{QLmax}	16	16	16	mA		
Output reverse HIGH [2]	I_{QHmax}	50	50	50	µA	4.75	$V_G = V_{GLmax}$; V_Q = 12 V
SUPPLY DATA							
Supply current							
Output LOW	I_{PL} typ.	–	12	–	mA	5.0	V_G = 5 V; $I_Q = 0$
	I_{PL} <	–	22	–	mA	5.25	
Output HIGH	I_{PH} typ.	–	4	–	mA	5.0	V_G = 0; $I_Q = 0$
	I_{PH} <	–	8	–	mA	5.25	
DYNAMIC DATA							
Rise propagation delay time:	t_{pdr} typ.	–	35	–	ns	5.0	R_L = 390 Ω; C_L = 15 pF
	t_{pdr} <	–	45	–	ns	5.0	
Fall propagation delay time:	t_{pdf} typ.	–	8	–	ns	5.0	R_L = 390 Ω; C_L = 15 pF
	t_{pdf} <	–	15	–	ns	5.0	

[1] Not for FJH311/7401-S1 and FJH321/7405-S1

[2] For FJH311/7401-S1 and FJH321/7405-S1:
I_{QHmax} = 250 µA at $V_G = V_{GLmax}$ and V_Q = 15 V.

APPLICATION INFORMATION

Determining the value of R_L

Proper operation of the functions mentioned depends on the value of the common load resistor. The maximum value is set by the need to ensure sufficient load current to TTL loads and off current I_{QHmax} through paralleled outputs when the output is HIGH. A minimum value is set by the need to limit the total current through the resistor, including the "sink" current of the TTL loads, so that the output voltage does not rise above the LOW level, even when one of the paralleled outputs is absorbing all the current. The table shows minimum and maximum resistor values for up to 10 TTL loads and up to 7 gates connected in wired-OR.

Table 1

fan-out to TTL loads	wired-OR outputs							
	1	2	3	4	5	6	7	1 to 7
1	8965	4814	3291	2500	2015	1688	1452	319
2	7878	4482	3132	2407	1954	1645	1420	359
3	7027	4193	2988	2321	1897	1604	1390	410
4	6341	3939	2857	2241	1843	1566	1361	479
5	5777	3714	2736	2166	1793	1529	1333	575
6	5306	3513	2626	2096	1744	1494	1306	718
7	4905	3333	2524	2031	1699	1460	1280	958
8	4561	3170	2429	1969	1656	X	X	1437
9	4262	3023	X	X	X	X	X	2875
10	4000	X	X	X	X	X	X	4000*
	maximum							min.
	load resistor values in ohms							

X = not recommended or not possible

* = the theoretical value is ∞

All values shown in the table are based on:

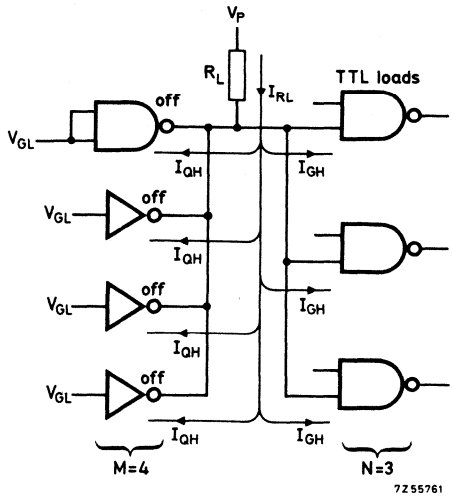
Logical HIGH conditions: V_P = 5 V; V_{QH} required = 2.4 V

Logical LOW conditions: V_P = 5 V; V_{QL} required = 0.4 V

APPLICATION INFORMATION (continued)

Circuit calculations

HIGH (off level) configurations (see figure below)



$M.I_{QH} = 4 \times 250\ \mu A$ $\quad N.I_{GH} = 3 \times 40\ \mu A$ $\quad R_{Lmax} = \frac{(5-2.4)V}{(0.001 + 0.00012)A} = 2321\ \Omega$

The allowable voltage drop across the load resistor (V_{RL}) is the difference between V_P applied and the output voltage V_{QH} required at the TTL load.

$$V_{RL} = V_P - V_{QHmin}$$

The total current through the load resistor (I_{RL}) is the sum of the load currents I_{GH} and off-level reverse current I_{QH} through each of the "wired-OR" connected outputs. Putting N as the number of TTL loads, and M as the number of outputs, the current is given by

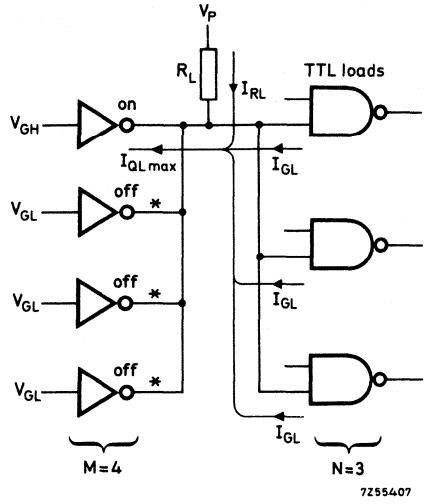
$$I_{RL} = M.I_{QH} + N.I_{GH}$$

Therefore, the maximum value of R_L is

$$R_{Lmax} = \frac{V_P - V_{QHmin}}{M.I_{QH} + N.I_{GH}}$$

APPLICATION INFORMATION (continued)

LOW (on level) configurations (see figure below)



I_{QLmax} = 16 mA N. $|I_{GLmax}|$ = 3 x 1.6 mA $R_{Lmin} = \frac{(5-0.4)V}{(0.016-0.0048)A} = 410\ \Omega$

*current through OFF outputs negligible at LOW output state

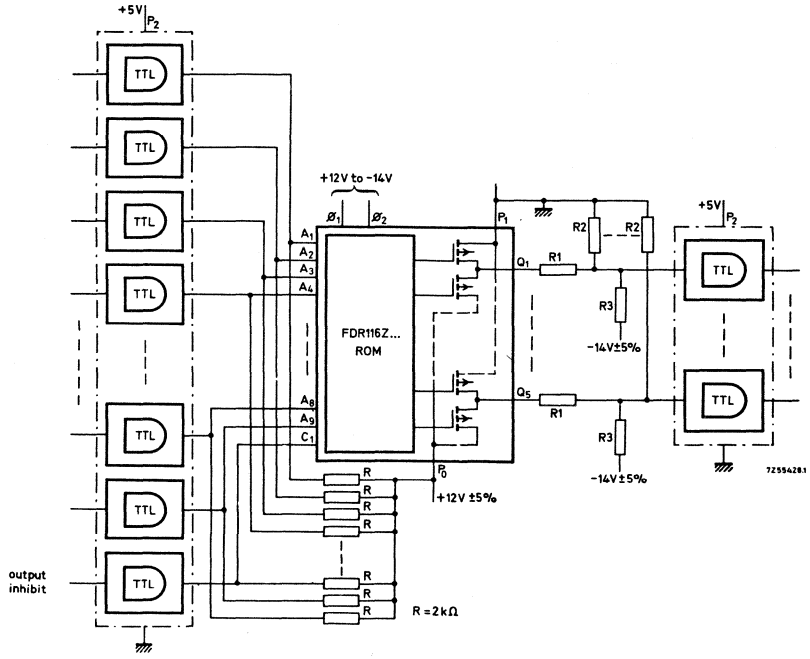
The current through the resistor must be limited to the maximum for one output transistor. If several outputs are "wired-OR" connected the current through R_L may be shared among the paralleled output transistor, but, unless it can be guaranteed that more than one transistor will be in the ON-(= conducting) state during the LOW output periods, the current must be limited to 16 mA, i.e. the maximum current that will still ensure a maximum LOW output voltage of 0.4 V.
The fan-out current must be considered as well. Part of the 16 mA will be supplied from the inputs being driven, which further reduces the current through R_L;
These considerations lead to the minimum value of R_L

$$R_{Lmin} = \frac{V_P - V_{QLmax}}{I_{QLmax} - N.\,|I_{GLmax}|}$$

For up to 10 TTL loads and up to 7 "wired-OR" connected outputs table I gives the maximum and minimum values of R_L calculated in this way.
For a single output the values are determined by the fan-out plus the leakage current of one transistor.
More than 7 outputs can be connected in "wired-OR" provided valid maximum and minimum resistor values are possible.
The value of R_L for driving 10 loads should be infinite according to these calculations but 4 kΩ is sufficient to satisfy logic HIGH while keeping logic LOW to less than 0.43 V.

APPLICATION INFORMATION (continued)

Typical application of open-collector gates as interface with MOS circuit.



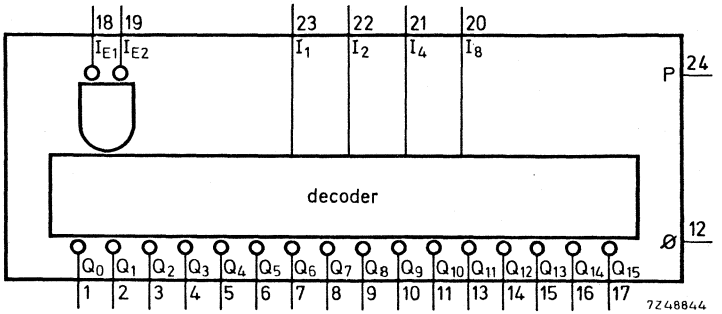
The example above shows a FDR116Z 2560-bit read-only memory being used together with TTL.

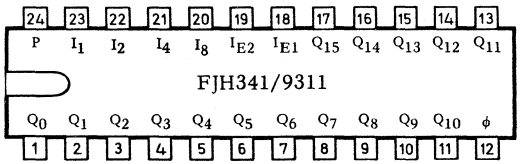
Open-collector gates are used at the input interface, each collector being taken through a 2 kΩ resistor to the 12 V positive supply voltage of the FDR116Z. A normal totem-pole output FJ type is used as the output to restore the TTL logic levels.

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

SINGLE ONE-OF-SIXTEEN DECODER





QUICK REFERENCE DATA				
Supply voltage	V_P		5.0 ± 5 %	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Propagation delay time	t_{pd}	typ.	23	ns
Available d.c. fan-out (full temperature range)	N_a	≥	10	
D.C. noise margin (full temperature range)	M_L	≥	0.4	V
Total power dissipation	P_{tot}	typ.	175	mW

PACKAGE OUTLINE 24 lead ceramic dual in-line **(See General Section).**

GENERAL DESCRIPTION

The FJH341/9311 is a multipurpose decoder which accepts four BCD inputs and provides sixteen mutually exclusive outputs. Its features include a fan-out of 10 over the full temperature and supply voltage range, a demultiplexing capability and a typical propagation delay of 23 ns from data input to output.

FUNCTION TABLE

inputs						output LOW-state *)
I_{E1}	I_{E2}	I_1	I_2	I_4	I_8	
H	H	X	X	X	X	**)
H	L	X	X	X	X	**)
L	H	X	X	X	X	**)
L	L	L	L	L	L	Q_0
L	L	H	L	L	L	Q_1
L	L	L	H	L	L	Q_2
L	L	H	H	L	L	Q_3
L	L	L	L	H	L	Q_4
L	L	H	L	H	L	Q_5
L	L	L	H	H	L	Q_6
L	L	H	H	H	L	Q_7
L	L	L	L	L	H	Q_8
L	L	H	L	L	H	Q_9
L	L	L	H	L	H	Q_{10}
L	L	H	H	L	H	Q_{11}
L	L	L	L	H	H	Q_{12}
L	L	H	L	H	H	Q_{13}
L	L	L	H	H	H	Q_{14}
L	L	H	H	H	H	Q_{15}

*) all other outputs are HIGH
**) all outputs are HIGH

H = HIGH (the more positive voltage)
L = LOW (the less positive voltage)
X = state immaterial

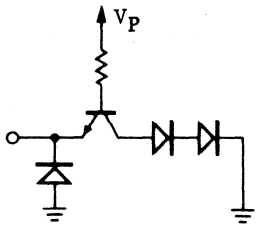
RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134).

Supply voltage	V_P	−0.5 to +7	V
Input voltage	All inputs	−0.5 to +5.5	V
Output voltage (HIGH state)	V_Q	−0.5 to V_P	V
Storage temperature	T_{stg}	−65 to +150	°C
Operating ambient temperature	T_{amb}	0 to +70	°C

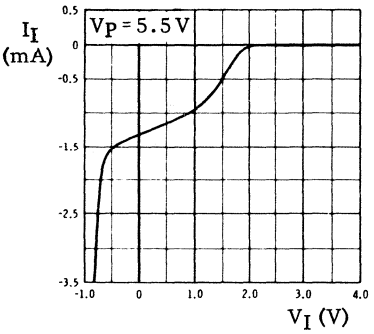
CHARACTERISTICS

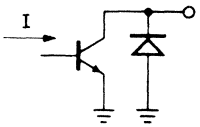
		T_{amb} (°C) 0	25	70		Conditions and references: V_P (V)	
STATIC DATA							
Voltages							
Input threshold LOW (any input)	V_{IL} max	0.8	0.8	0.8	V		
Input threshold HIGH (any input)	V_{IH} min	2.0	2.0	2.0	V		
Output LOW	V_{QL} max	0.4	0.4	0.4	V	5.25	$I_Q = I_{QL}$ max
		0.4	0.4	0.4	V	4.75	
Output HIGH	V_{QH} min	2.4	2.4	2.4	V	4.75	$-I_Q = -I_{QH}$max
Currents							
Input LOW	$-I_{IL}$ max	1.6	1.6	1.6	mA	5.25	$V_I = V_{QL}$ max
		1.41	1.41	1.41	mA	4.75	
Input HIGH	I_{IH} max	–	60	60	µA	5.25	V_I = 4.5 V
Output LOW	I_{QL} max	16	16	16	mA	5.25	
		14.1	14.1	14.1	mA	4.75	
Output HIGH	$-I_{QH}$ max	600	600	600	µA	4.75	
SUPPLY DATA							
Supply current	I_P ≤	–	60	–	mA	5	
	I_P typ.	–	35	–	mA	5	
DYNAMIC DATA							
Performance							
Rise propagation delay time							
I→Q	t_{pdr} ≤	–	40	–	ns	5	C_L = 15 pF
	t_{pdr} typ.	–	23	–	ns	5	
I_E→Q	t_{pdr} ≤	–	26	–	ns	5	
	t_{pdr} typ.	–	17	–	ns	5	
Fall propagation delay time							
I→Q	t_{pdf} ≤	–	35	–	ns	5	C_L = 15 pF
	t_{pdf} typ.	–	20	–	ns	5	
I_E→Q	t_{pdf} ≤	–	31	–	ns	5	
	t_{pdf} typ.	–	17	–	ns	5	

CHARACTERISTICS (continued) at T_{amb} =25 °C

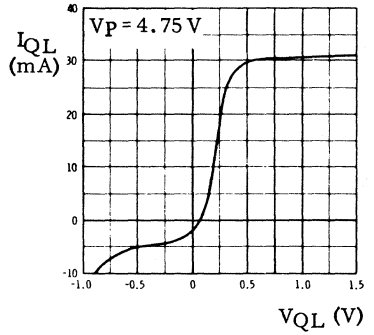


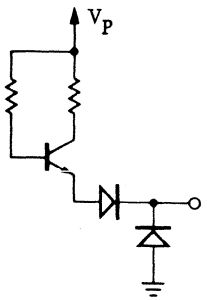
Equivalent input circuit



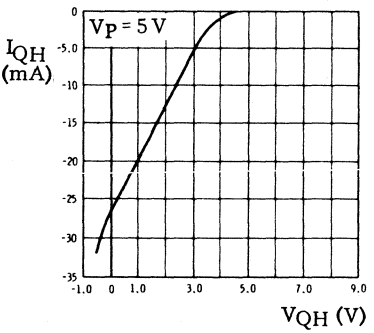


Equivalent output circuit (LOW state)

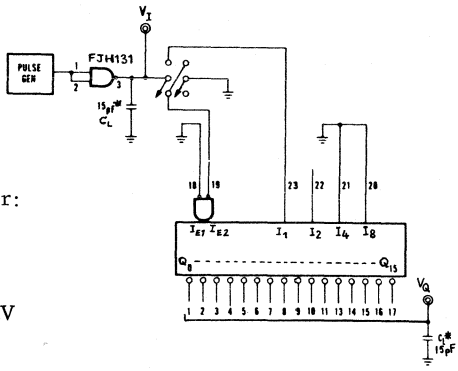




Equivalent output circuit (HIGH state)



CHARACTERISTICS (continued)



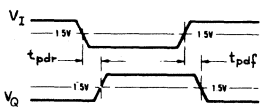
Pin 24 = V_P
Pin 12 = ϕ

Pulse generator:

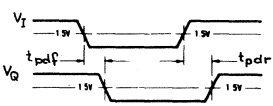
f = 1 MHz
t_p = 100 ns
$t_r = t_f \leq 15$ ns
Amplitude = 4 V

*) Including probe and jig capacitance

From I to Q

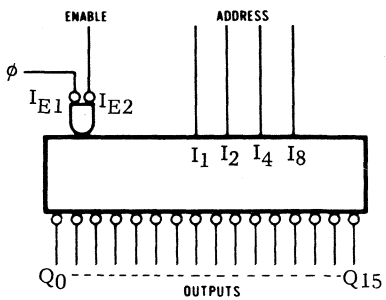


From I_E to Q



Switching time test circuit and waveforms

APPLICATION INFORMATION



decimal digit	output selection *) BCD code			
	8421	5421	excess 3	grey
0	Q_0	Q_0	Q_3	Q_0
1	Q_1	Q_1	Q_4	Q_1
2	Q_2	Q_2	Q_5	Q_3
3	Q_3	Q_3	Q_6	Q_2
4	Q_4	Q_4	Q_7	Q_6
5	Q_5	Q_8	Q_8	Q_7
6	Q_6	Q_9	Q_9	Q_5
7	Q_7	Q_{10}	Q_{10}	Q_4
8	Q_8	Q_{11}	Q_{11}	Q_{12}
9	Q_9	Q_{12}	Q_{12}	Q_{13}

*) A selected output will be LOW

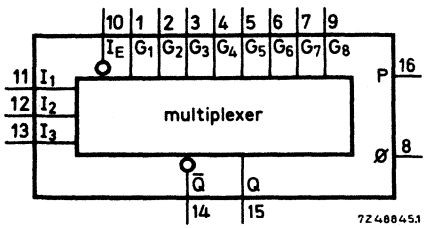
Decode any BCD code

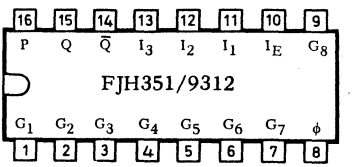
Decode any BCD code using a FJH341/9311 element. Any 4 bit BCD code may be decoded by selecting outputs. Some examples are shown in the table.

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

SINGLE 8-INPUT MULTIPLEXER





QUICK REFERENCE DATA				
Supply voltage	V_P		5.0 ± 5 %	V
Operating ambient temperature	T_{amb}		0 to 70	°C
Propagation delay time	t_{pd}	typ.	25	ns
D.C. noise margin (full temperature range)	M_L	≥	0.4	V
Average power consumption	P_{av}	typ.	135	mW

PACKAGE OUTLINE 16 lead plastic dual in-line (type A) **(See General Section)**

GENERAL DESCRIPTION

The FJH351/9312 is a monolithic high speed, eight-input digital multiplexer circuit, providing the ability to select one bit of data from up to eight sources. It can be used as a universal function generator to generate any logic function of four variables. Complementary outputs are provided.

FUNCTIONAL DESCRIPTION

The FJH351/9312 is a logical implementation of a single-pole eight-position switch with the switch position controlled by the state of three select inputs, I_1, I_2 and I_3. Both normal and inverted outputs are provided. The enable input (I_E) is active when in the LOW state. When it is not activated the inverted output is HIGH and the normal output is LOW regardless of all other inputs. The logic function provided at the output is:

$$Q = \overline{I}_E.(G_1.\overline{I}_1.\overline{I}_2.\overline{I}_3 + G_2.I_1.\overline{I}_2.\overline{I}_3 + G_3.\overline{I}_1.I_2.\overline{I}_3 + G_4.I_1.I_2.\overline{I}_3 +$$

$$G_5.\overline{I}_1.\overline{I}_2.I_3 + G_6.I_1.\overline{I}_2.I_3 + G_7.\overline{I}_1.I_2.I_3 + G_8.I_1.I_2.I_3)$$

The FJH351/9312 provides the ability, in one package, to select from eight sources of data or control information. By proper manipulation of the inputs, the device can provide any logic function of four variables and its complement. Thus any number of random logic elements used to generate unusual truth tables can be replaced by one FJH351/9312.

FUNCTION TABLE

inputs												outputs	
I_E	I_3	I_2	I_1	G_1	G_2	G_3	G_4	G_5	G_6	G_7	G_8	Q	$\overline{Q}$
H	X	X	X	X	X	X	X	X	X	X	X	L	H
L	L	L	L	L	X	X	X	X	X	X	X	L	H
L	L	L	L	H	X	X	X	X	X	X	X	H	L
L	L	L	H	X	L	X	X	X	X	X	X	L	H
L	L	L	H	X	H	X	X	X	X	X	X	H	L
L	L	H	L	X	X	L	X	X	X	X	X	L	H
L	L	H	L	X	X	H	X	X	X	X	X	H	L
L	L	H	H	X	X	X	L	X	X	X	X	L	H
L	L	H	H	X	X	X	H	X	X	X	X	H	L
L	H	L	L	X	X	X	X	L	X	X	X	L	H
L	H	L	L	X	X	X	X	H	X	X	X	H	L
L	H	L	H	X	X	X	X	X	L	X	X	L	H
L	H	L	H	X	X	X	X	X	H	X	X	H	L
L	H	H	L	X	X	X	X	X	X	L	X	L	H
L	H	H	L	X	X	X	X	X	X	H	X	H	L
L	H	H	H	X	X	X	X	X	X	X	L	L	H
L	H	H	H	X	X	X	X	X	X	X	H	H	L

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134).

Supply voltage	V_P		−0.5 to +7	V
Input voltage	All inputs		−0.5 to +5.5	V [1]
Input current	All inputs		−30 to +5	mA
Output voltage (HIGH state)	V_Q		0 to V_P	V
Output current (LOW state)	I_Q	max.	30	mA
Storage temperature	T_{stg}		−65 to +150	°C
Operating ambient temperature	T_{amb}		0 to +70	°C

[1]) Either input voltage or input current limit is sufficient to protect the inputs.

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references	
		0	25	70		V_P (V)	
STATIC DATA							
Voltages [1]							
Input threshold LOW (any input)	V_{GLmax}	0.8	0.8	0.8	V		
Input threshold HIGH (any input)	V_{GHmin}	2.0	2.0	2.0	V		
Output LOW:							
Q	V_{QLmax}	0.4	0.4	0.4	V	5.25	I_{QL} = 16 mA
	V_{QLmax}	0.4	0.4	0.4	V	4.75	I_{QL} = 14.1 mA
$\bar{Q}$	$V_{\bar{Q}Lmax}$	0.4	0.4	0.4	V	5.25	$I_{\bar{Q}L}$ = 14.4 mA
	$V_{\bar{Q}Lmax}$	0.4	0.4	0.4	V	4.75	$I_{\bar{Q}L}$ = 12.7 mA
Output HIGH:							
Q	V_{QHmin}	2.4	2.4	2.4	V	4.75	$-I_{QH}$ = 1.2 mA
$\bar{Q}$	$V_{\bar{Q}Hmin}$	2.4	2.4	2.4	V	4.75	$-I_{\bar{Q}H}$ = 1.08 mA
Currents							
Input LOW	$-I_{GLmax}$	1.6	1.6	1.6	mA	5.25	$V_G = V_{QLmax}$
	$-I_{GLmax}$	1.41	1.41	1.41	mA	4.75	
Input HIGH	I_{GHmax}	-	60	60	µA	5.25	V_G = 4.5 V
Output LOW							
Q	I_{QLmax}	16	16	16	mA	5.25	$V_Q = V_{QLmax}$
	I_{QLmax}	14.1	14.1	14.1	mA	4.75	
$\bar{Q}$	$I_{\bar{Q}Lmax}$	14.4	14.4	14.4	mA	5.25	$V_{\bar{Q}} = V_{\bar{Q}Lmax}$
	$I_{\bar{Q}Lmax}$	12.7	12.7	12.7	mA	4.75	
Output HIGH							
Q	$-I_{QHmax}$	-	1.2	1.2	mA	4.75	$V_Q = V_{QHmin}$
$\bar{Q}$	$-I_{\bar{Q}Hmax}$	-	1.08	1.08	mA	4.75	$V_{\bar{Q}} = V_{\bar{Q}Hmin}$
SUPPLY DATA							
Supply current	$I_P \leq$	43	43	43	mA	5.0	
	I_P typ.	-	27	-	mA	5.0	

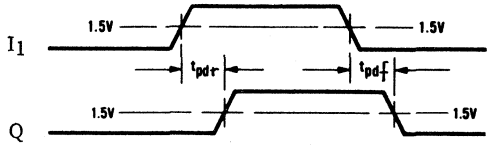
[1] Inputs at threshold voltage (V_{GHmin} or V_{GLmax})

CHARACTERISTICS (continued)

		T_{amb} (°C)				Conditions and references	
		0	25	70		V_P (V)	
DYNAMIC DATA							
Performance							
Rise propagation delay time I → Q	t_{pdr} ≤	–	34	–	ns	5.0	C_L = 15 pF
	t_{pdr} typ.	–	23	–	ns	5.0	
Fall propagation delay time I → Q	t_{pdf} ≤	–	36	–	ns	5.0	
	t_{pdf} typ.	–	25	–	ns	5.0	

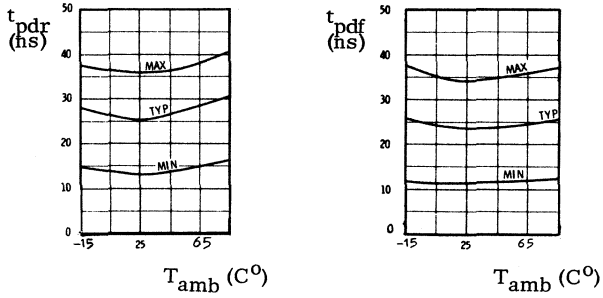
CHARACTERISTICS (continued)

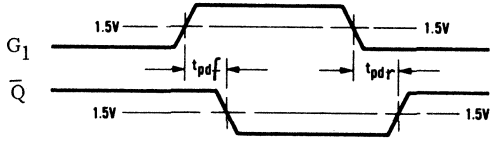
All measurements are made with $V_P = 5$ V. The active input is driven by a FJH131 gate with the output loaded with 15 pF. Both outputs of the **FJH351/9312** are loaded with 15 pF.



Conditions:
I_2; I_3; G_1; I_E connected to ϕ
$G_2 = V_P$ via 1 kΩ

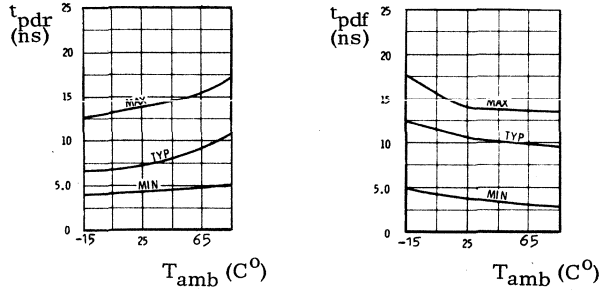
Waveforms illustrating the measurement of t_{pdr} and t_{pdf} from I_1 to Q



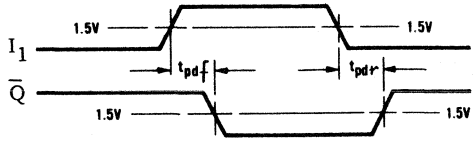


Condition:
I_E; I_1; I_2; I_3 connected to ϕ

Waveforms illustrating the measurement of t_{pdr} and t_{pdf} from G_1 to $\overline{Q}$

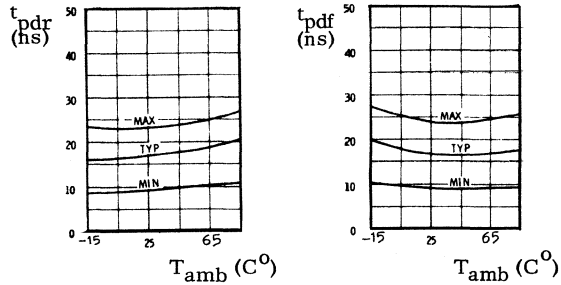


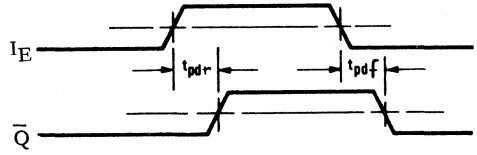
CHARACTERISTICS (continued) at conditions of page 6



Conditions:
G_1; I_E; I_2; I_3 connected to ϕ
$G_2 = V_P$ via 1 kΩ

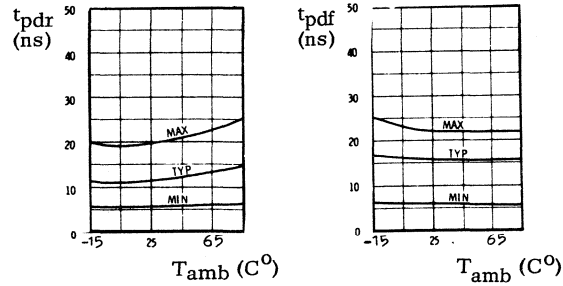
Waveforms illustrating the measurement of t_{pdr} and t_{pdf} from I_1 to $\overline{Q}$





Conditions:
I_1; I_2; I_3 connected to ϕ
$G_1 = V_P$ via 1 kΩ

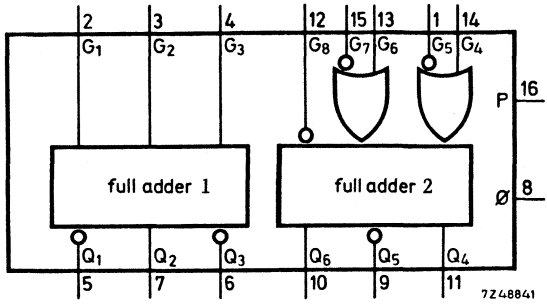
Waveforms illustrating the measurement of t_{pdr} from I_E to $\overline{Q}$

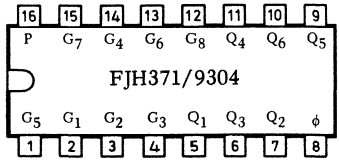


The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

DUAL FULL ADDER





QUICK REFERENCE DATA				
Supply voltage	V_P		5.0 ± 5 %	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Carry propagation delay time	t_{pd}	typ.	8	ns
D.C. noise margin (full temperature range)	M_L	≥	0.4	V
Total power dissipation	P_{tot}	typ.	150	mW

PACKAGE OUTLINE 16 lead plastic dual in-line (type A) **(See General Section).**

GENERAL DESCRIPTION

The FJH371/9304 dual full adder may be used in a wide variety of applications including multiple bit parallel add/serial carry addition, parity generation and checking, code conversion, and majority gating.
Its features include: multi-function capability; two independent binary full adders; a carry propagation delay time of 8 ns; and complementary inputs and outputs.

FUNCTIONAL DESCRIPTION

The logic block consists of two separate high speed full adders.
This design allows a minimum carry propagation delay time when the adders are used in ripple carry applications.
One of the adders has the additional facility for either active HIGH or active LOW inputs. The adders produce a LOW carry and both LOW and HIGH sum with active HIGH inputs, a HIGH carry and both HIGH and LOW sum when active LOW inputs are used.

FUNCTION TABLE

adder 1					
G_1	G_2	G_3	Q_1	Q_2	Q_3
L	L	L	H	L	H
H	L	L	H	H	L
L	H	L	H	H	L
H	H	L	L	L	H
L	L	H	H	H	L
H	L	H	L	L	H
L	H	H	L	L	H
H	H	H	L	H	L

For positive logic:
$Q_1 = \overline{\text{carry}}$
$Q_2 = \text{sum}$
$Q_3 = \overline{\text{sum}}$

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

FUNCTION TABLE (continued)

adder 2							
G_8	G_6	G_4	G_7	G_5	Q_4	Q_6	Q_5
L	L	L	L	L	H	H	L
L	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H
L	L	L	H	H	L	H	L
L	L	H	L	L	H	H	L
L	L	H	L	H	H	H	L
L	L	H	H	L	H	L	H
L	L	H	H	H	H	L	H
L	H	L	L	L	H	H	L
L	H	L	L	H	H	L	H
L	H	L	H	L	H	H	L
L	H	L	H	H	H	L	H
L	H	H	L	L	H	H	L
L	H	H	L	H	H	H	L
L	H	H	H	L	H	H	L
L	H	H	H	H	H	H	L
H	L	L	L	L	H	L	H
H	L	L	L	H	L	H	L
H	L	L	H	L	L	H	L
H	L	L	H	H	L	L	H
H	L	H	L	L	H	L	H
H	L	H	L	H	H	L	H
H	L	H	H	L	L	H	L
H	L	H	H	H	L	H	L
H	H	L	L	L	H	L	H
H	H	L	L	H	L	H	L
H	H	L	H	L	H	L	H
H	H	L	H	H	L	H	L
H	H	H	L	L	H	L	H
H	H	H	L	H	H	L	H
H	H	H	H	L	H	L	H
H	H	H	H	H	H	L	H

For positive logic:
Q_4 = carry
Q_5 = $\overline{\text{sum}}$
Q_6 = sum

H = HIGH state (the more positive voltage)

L = LOW state (the more negative voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134).

Supply voltage	V_P	−0.5 to +7.0	V
Input voltage	All inputs	−0.5 to +5.5	V
Output voltage (HIGH state)	V_Q	−0.5 to V_P	V
Storage temperature	T_{stg}	−65 to +150	°C
Operating ambient temperature	T_{amb}	0 to +70	°C

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references	
		0	25	70		V_P (V)	
STATIC DATA							
Voltages							
Input threshold LOW (any input)	V_{GLmax}	0.8	0.8	0.8	V		
Input threshold HIGH (any input)	V_{GHmin}	2.0	2.0	2.0	V		
Output LOW	V_{Q2Lmax}	0.4	0.4	0.4	V	5.25	I_{Q2L} = 16 mA
	V_{Q2Lmax}	0.4	0.4	0.4	V	4.75	I_{Q2L} = 14.1 mA
	V_{Q5Lmax}	0.4	0.4	0.4	V	5.25	I_{Q5L} = 16 mA
	V_{Q5Lmax}	0.4	0.4	0.4	V	4.75	I_{Q5L} = 14.1 mA
	V_{Q3Lmax}	0.4	0.4	0.4	V	5.25	I_{Q3L} = 14.4 mA
	V_{Q3Lmax}	0.4	0.4	0.4	V	4.75	I_{Q3L} = 12.7 mA
	V_{Q6Lmax}	0.4	0.4	0.4	V	5.25	I_{Q6L} = 14.4 mA
	V_{Q6Lmax}	0.4	o.4	0.4	V	4.75	I_{Q6L} = 12.7 mA
	V_{Q1Lmax}	0.4	0.4	0.4	V	5.25	I_{Q1L} = 11.2 mA
	V_{Q1Lmax}	0.4	0.4	0.4	V	4.75	I_{Q1L} = 9.85 mA
	V_{Q4Lmax}	0.4	0.4	0.4	V	5.25	I_{Q4L} = 11.2 mA
	V_{Q4Lmax}	0.4	0.4	0.4	V	4.75	I_{Q4L} = 9.85 mA
Output HIGH	V_{Q2Hmin}	2.4	2.4	2.4	V	4.75	$-I_{Q2H}$ = 1.2 mA
	V_{Q5Hmin}	2.4	2.4	2.4	V	4.75	$-I_{Q5H}$ = 1.2 mA
	V_{Q3Hmin}	2.4	2.4	2.4	V	4.75	$-I_{Q3H}$ = 1.08 mA
	V_{Q6Hmin}	2.4	2.4	2.4	V	4.75	$-I_{Q6H}$ = 1.08 mA
	V_{Q1Hmin}	2.4	2.4	2.4	V	4.75	$-I_{Q1H}$ = 0.84 mA
	V_{Q4Hmin}	2.4	2.4	2.4	V	4.75	$-I_{Q4H}$ = 0.84 mA
Currents							
Input LOW							
G_4; G_6	$-I_{G4Lmax}$ $-I_{G6Lmax}$	1.6	1.6	1.6	mA	5.25	$V_{G4} = V_{G6} = V_{QLmax}$; all other inputs: 5.25 V
G_1;G_2;G_3;G_5;G_7;G_8	$-I_{G1Lmax}$ $-I_{G2Lmax}$ $-I_{G3Lmax}$ $-I_{G5Lmax}$ $-I_{G7Lmax}$ $-I_{G8Lmax}$	6.4	6.4	6.4	mA	5.25	$V_{G1} = V_{G2} = V_{G4} = V_{G5} = V_{G7} = V_{G8} = V_{QLmax}$; all other inputs: 5.25 V

CHARACTERISTICS (continued)

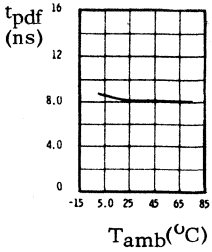
		T_{amb} (°C) 0	25	70		V_P (V)	Conditions and references
Currents (continued)							
Input LOW							
$G_4;G_6$	$-I_{G4Lmax}$ $-I_{G6Lmax}$	1.41	1.41	1.41	mA	4.75	$V_{G4}=V_{G6}=V_{QLmax}$; all other inputs: 5.25 V
$G_1;G_2;G_3;G_5;G_7;G_8$	$-I_{G1Lmax}$ $-I_{G2Lmax}$ $-I_{G3Lmax}$ $-I_{G5Lmax}$ $-I_{G7Lmax}$ $-I_{G8Lmax}$	5.64	5.64	5.64	mA	4.75	$V_{G1}=V_{G2}=V_{G3}=V_{G5}=V_{G7}$; all other inputs: 5.25 V
Input HIGH							
$G_4;G_6$	I_{G4Hmax} I_{G6Hmax}	–	60	60	µA	5.25	$V_{G4}=V_{G6}=4.5$ V; other inputs to ϕ
$G_1;G_2;G_3$ $G_5;G_7;G_8$	I_{G1Hmax} I_{G2Hmax} I_{G3Hmax} I_{G5Hmax} I_{G7Hmax} I_{G8Hmax}	–	240	240	µA	5.25	$V_{G1}=V_{G2}=V_{G3}=V_{G5}=V_{G7}=V_{G8}=4.5$V; other inputs to ϕ
Output LOW							
$Q_1;Q_4$	I_{Q1Lmax} I_{Q4Lmax}	11.2	11.2	11.2	mA	5.25	$V_{Q1}=V_{Q4}=V_{QLmax}$
$Q_1;Q_4$	I_{Q1Lmax} I_{Q4Lmax}	9.85	9.85	9.85	mA	4.75	$V_{Q1}=V_{Q4}=V_{QLmax}$
$Q_3;Q_6$	I_{Q3Lmax} I_{Q6Lmax}	14.4	14.4	14.4	mA	5.25	$V_{Q2}=V_{Q6}=V_{QLmax}$
$Q_3;Q_6$	I_{Q3Lmax} I_{Q6Lmax}	12.7	12.7	12.7	mA	4.75	$V_{Q3}=V_{Q6}=V_{QLmax}$
$Q_2;Q_5$	I_{Q2Lmax} I_{Q5Lmax}	16.0	16.0	16.0	mA	5.25	$V_{Q2}=V_{Q5}=V_{QLmax}$
$Q_2;Q_5$	I_{Q2Lmax} I_{Q5Lmax}	14.1	14.1	14.1	mA	4.75	$V_{Q2}=V_{Q5}=V_{QLmax}$
Output HIGH							
$Q_1;Q_4$	$-I_{Q1Hmax}$ $-I_{Q4Hmax}$	–	420	420	µA	5.25	$V_{Q1}=V_{Q4}=V_{QHmin}$
$Q_3;Q_6$	$-I_{Q3Hmax}$ $-I_{Q6Hmax}$	–	540	540	µA	5.25	$V_{Q3}=V_{Q6}=V_{QHmin}$
$Q_2;Q_5$	$-I_{Q2Hmax}$ $-I_{Q5Hmax}$	–	600	600	µA	5.25	$V_{Q2}=V_{Q5}=V_{QHmin}$

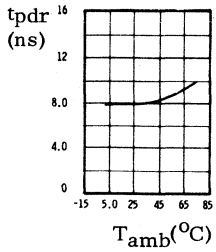
CHARACTERISTICS (continued)

		T_{amb} (°C)				V_P (V)	Conditions and references
		0	25	70			
DYNAMIC DATA							
Performance							
Rise propagation delay time							
$G_3 \rightarrow Q_1$	$t_{pdr} \leq$	–	15	–	ns	5	C_L = 15 pF
	t_{pdr} typ.	–	8.0	–	ns	5	
$G_4 \rightarrow Q_5$	$t_{pdr} \leq$	–	45	–	ns	5	C_L = 15 pF
	t_{pdr} typ.	–	28	–	ns	5	
Fall propagation delay time							
$G_3 \rightarrow Q_1$	$t_{pdf} \leq$	–	15	–	ns	5	C_L = 15 pF
	t_{pdf} typ.	–	8.0	–	ns	5	
$G_4 \rightarrow Q_5$	$t_{pdf} \leq$	–	40	–	ns	5	C_L = 15 pF
	t_{pdf} typ.	–	25	–	ns	5	

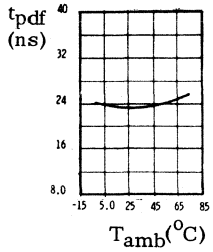
CHARACTERISTICS (continued)

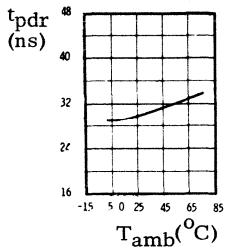
Carry delay: $G_3 \rightarrow Q_1$



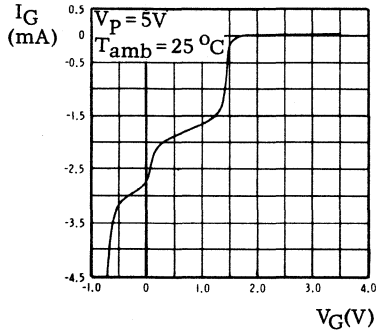


Add delay: $G_4 \rightarrow Q_5$

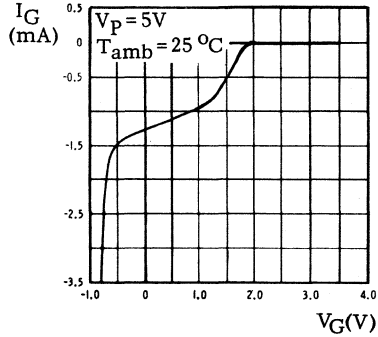




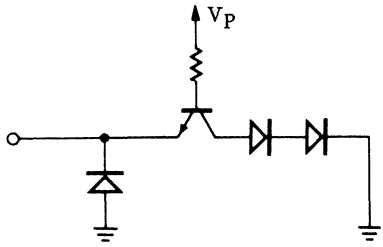
Switching time conditions: V_P = 5V; C_L = 15 pF.



Input curve for: G_1; G_2; G_3; G_5; G_7; G_8

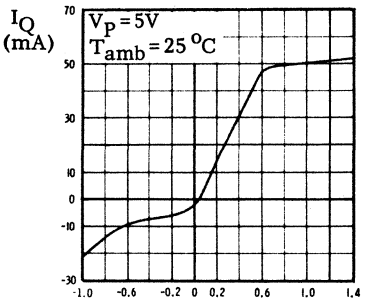


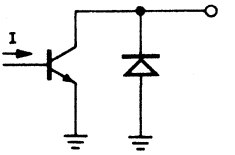
Input curve for: G_4; G_6



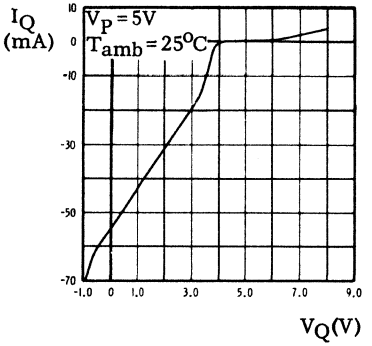
Equivalent input circuit

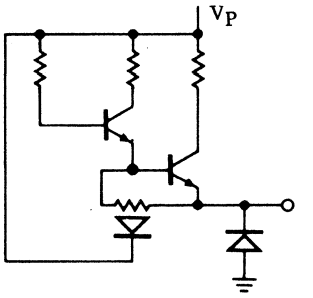
CHARACTERISTICS (continued)





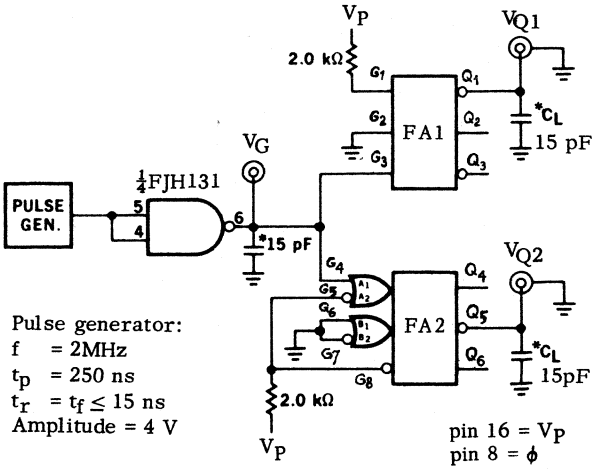
Output curve and equivalent output circuit; LOW state

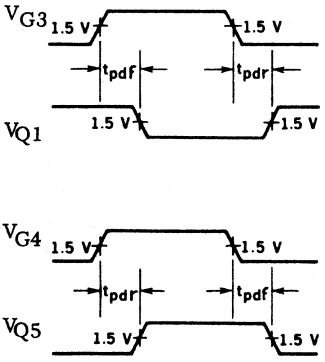




Output curve and equivalent output circuit ; HIGH state

CHARACTERISTICS (continued)



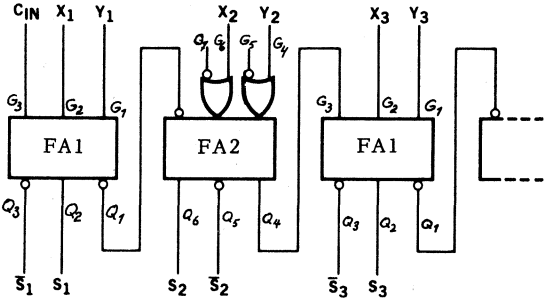


Switching time test circuit and waveforms

*) Including probe and jig capacitance.

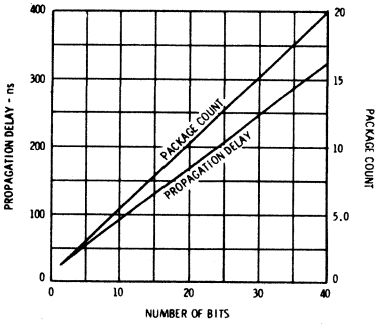
APPLICATION INFORMATION

The FJH371/9304 dual adder has been designed to be useful in a wide variety of applications such as addition, parity generation and checking, code conversion and majority gating.
The multifunctional capabilities can be seen from reference to the applications shown.



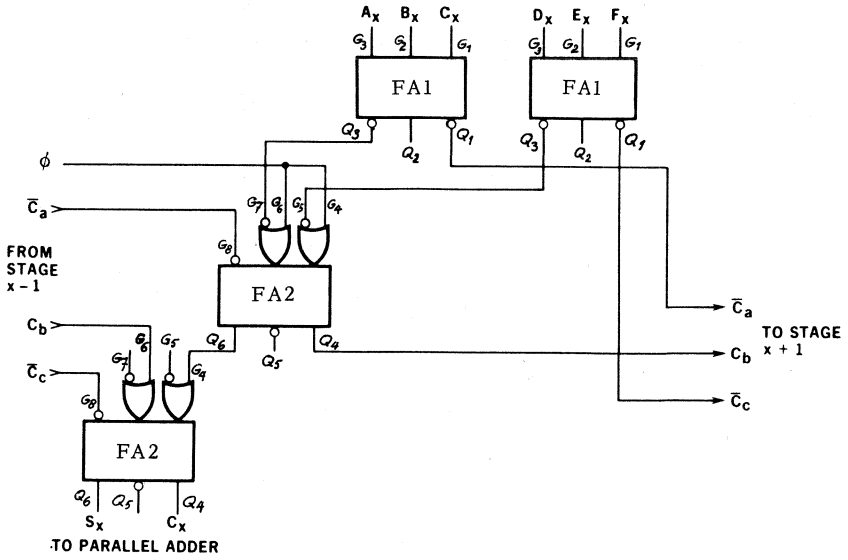
Ripple carry parallel addition

Only one AND-OR-NOT gate delay is incurred at each stage allowing a typical addition speed if (N + 1) x 8 ns, where N is the number of bits in the word. A similar scheme will work if the inverted inputs are used, and the design acts as a subtractor when the complement of one variable is provided.



The curve shows propagation delay of the ripple carry adder.
Plotted on the same diagram is a curve showing the low package count resulting from this ripple scheme.

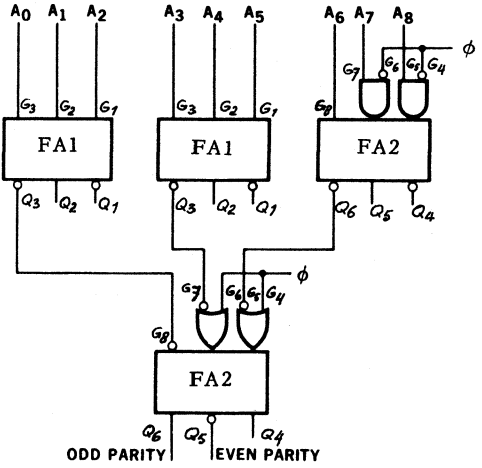
APPLICATION INFORMATION (continued)



Addition of six variables

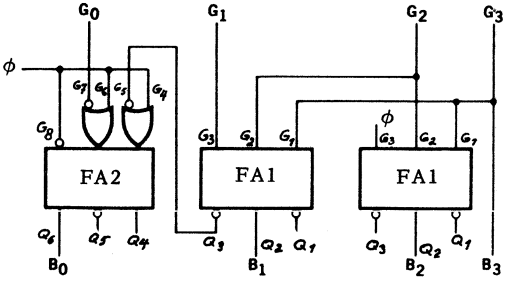
This design can be used in carry save arithmetic. Six input variables are reduced to two where they can be added in a parallel adder. Delay between inputs and outputs is typically 50 ns, allowing extremely high speed computation. Additional variables may be added or the concept can be extended to multiplication, division, and various other arithmetic operations.

APPLICATION INFORMATION (continued)



Byte parity generation or checking

The FJH371/9304 can be used for parity checking or generating.
This design uses two FJH371 /9304 to generate parity for an 8 bit byte or check parity over 9 bits. The delay from input to odd parity is typically 35 ns. Additional adder blocks can be used to generate or check parity over larger word lengths. The concept can also be used for hamming and cyclic code generation and checking.



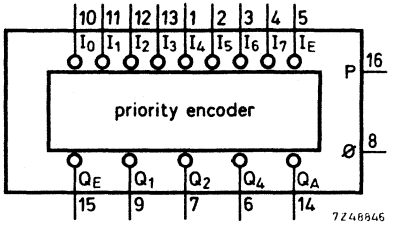
4-bit parallel grey to binary conversion

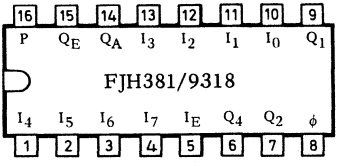
A 4-bit parallel grey to binary conversion is shown. The adders can also be used for other cyclic code manipulations.

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

SINGLE 8-INPUT PRIORITY ENCODER





QUICK REFERENCE DATA				
Supply voltage	V_P		5.0 ± 5 %	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Propagation delay time	t_{pd}	typ.	25	ns
D.C. noise margin (full temperature range)	M_L	≥	0.4	V
Total power dissipation	P_{tot}	typ.	250	mW

PACKAGE OUTLINE 16 lead plastic dual in-line (type A) (See General Section).

GENERAL DESCRIPTION

The FJH381/9318 is a multipurpose encoder which accepts 8-inputs and produces a BCD (1-2-4 code) weighted output of the highest order input. Typical uses of this multifunction device are: various code converters, multichannel D/A converter, decimal to BCD converter, and priority encoding of n bits by cascading stages.

FUNCTIONAL DESCRIPTION

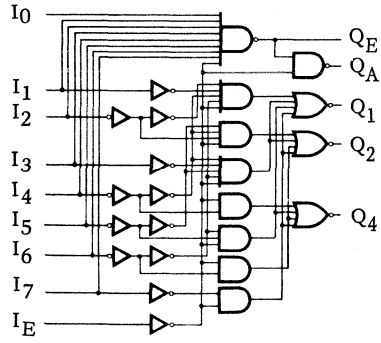
The FJH381/9318 8-input priority encoder accepts data from 8 active LOW inputs and provides a binary representation on the 3 active LOW outputs. A priority is assigned to each input so that when two or more inputs are simultaneously LOW, the input with the highest priority is represented on the output, with input I_7 having the highest priority.
A HIGH level on the input enable I_E will force all outputs to the HIGH state and allow new data to settle without producing erroneous information at the outputs.
Provided with the 3 data outputs(Q_1, Q_2 and Q_4) are a group signal output (Q_A) and an enable output (Q_E).
Q_A is LOW when any input is LOW: this indicates when any input is active. Q_E is LOW when all inputs are HIGH. Using the output enable along with the input enable allows priority encoding of N input signals. Both Q_E and Q_A are HIGH when the input enable (I_E) is HIGH.

FUNCTION TABLE

inputs									outputs				
I_E	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	Q_A	Q_1	Q_2	Q_4	Q_E
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	H	L	L	H
L	X	X	X	X	X	L	H	H	L	L	H	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	L	L	L	H	H
L	X	X	L	H	H	H	H	H	L	H	L	H	H
L	X	L	H	H	H	H	H	H	L	L	H	H	H
L	L	H	H	H	H	H	H	H	L	H	H	H	H

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

LOGIC DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134).

Supply voltage	V_P		−0.5 to +7.0	V
Input voltage	All inputs		−0.5 to +5.5	V
Output voltage (HIGH state)	V_Q		−0.5 to V_P	V
Output current (LOW state)	I_Q	max.	50	mA
Storage temperature	T_{stg}		−65 to +150	°C
Operating ambient temperature	T_{amb}		0 to +70	°C

CHARACTERISTICS

		T_{amb} (°C) 0	25	70		Conditions and references: V_P (V)	
STATIC DATA							
Voltages							
Input threshold LOW (any input)	V_{ILmax}	0.8	0.8	0.8	V		
Input threshold HIGH (any input)	V_{IHmax}	2.0	2.0	2.0	V		
Output LOW [4]	V_{QLmax}	0.4	0.4	0.4	V	5.25	$I_Q = I_{QLmax}$
	V_{QLmax}	0.4	0.4	0.4	V	4.75	$I_Q = I_{QLmax}$
Output HIGH [4]	V_{QHmin}	2.4	2.4	2.4	V	4.75	$-I_Q = -I_{QHmax}$
Currents							
Input LOW:							
I_0	$-I_{ILmax}$	1.6	1.6	1.6	mA	5.25	$V_I = V_{QLmax}$ [1]
	$-I_{ILmax}$	1.41	1.41	1.41	mA	4.75	$V_I = V_{QLmax}$ [1]
I_E; I_1 to I_7	$-I_{ILmax}$	3.2	3.2	3.2	mA	5.25	$V_I = V_{QLmax}$ [1]
	$-I_{ILmax}$	2.82	2.82	2.82	mA	4.75	$V_I = V_{QLmax}$ [1]
Input HIGH:							
I_0	I_{IHmax}	–	60	60	µA	5.25	$V_I = 4.5$ V [2]
I_E; I_1 to I_7	I_{IHmax}	–	120	120	µA	5.25	$V_I = 4.5$ V [2]
Output LOW:							
Q_E	I_{QLmax}	8.0	8.0	8.0	mA	5.25	$V_Q = V_{QLmax}$
	I_{QLmax}	7.1	7.1	7.1	mA	4.75	$V_Q = V_{QLmax}$
Q_A	I_{QLmax}	9.6	9.6	9.6	mA	5.25	$V_Q = V_{QLmax}$
	I_{QLmax}	8.5	8.5	8.5	mA	4.75	$V_Q = V_{QLmax}$
Q_1; Q_2; Q_4	I_{QLmax}	16	16	16	mA	5.25	$V_Q = V_{QLmax}$
	I_{QLmax}	14 1	14.1	14.1	mA	4.75	$V_Q = V_{QLmax}$
Output HIGH:							
Q_E	$-I_{QHmax}$	0.6	0.6	0.6	mA	4.75	$V_Q = V_{QHmin}$
Q_A	$-I_{QHmax}$	0.72	0.72	0.72	mA	4.75	$V_Q = V_{QHmin}$
Q_1; Q_2; Q_4	$-I_{QHmax}$	1.2	1.2	1.2	mA	4.75	$V_Q = V_{QHmin}$
SUPPLY DATA							
Supply current	$I_P \leq$	–	80	80	mA	5.0	3)
	I_P typ.	–	55	–	mA	5.0	3)

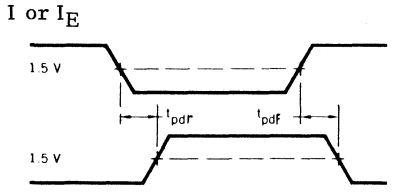
1) All other inputs $V_I = 5.5$ V
2) All other inputs to ϕ
3) I_7 and I_E to ϕ; All other terminals: HIGH
4) All outputs: Q_1, Q_2, Q_4, Q_E, Q_A.

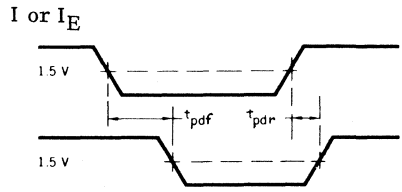
CHARACTERISTICS (continued)

		T_{amb} (°C) 0	25	70		Conditions and references V_P (V)	
DYNAMIC DATA						5.0	C_L = 15 pF
Performance						↓	↓
Rise propagation delay time							
$I \rightarrow Q_E$ [1]	$t_{pdr} \leq$	–	15	–	ns		
	$t_{pdr} \geq$	–	2	–	ns		
$I \rightarrow Q_A$ [1]	$t_{pdr} \leq$	–	45	–	ns		
	$t_{pdr} \geq$	–	12	–	ns		
$I \rightarrow Q$ [1]	$t_{pdr} \leq$	–	38	–	ns		
	$t_{pdr} \geq$	–	14	–	ns		
$I_E \rightarrow Q_E$	$t_{pdr} \leq$	–	21	–	ns		
	$t_{pdr} \geq$	–	7	–	ns		
$I_E \rightarrow Q_A$	$t_{pdr} \leq$	–	20	–	ns		
	$t_{pdr} \geq$	–	8	–	ns		
$I_E \rightarrow Q$	$t_{pdr} \leq$	–	25	–	ns		
	$t_{pdr} \geq$	–	8	–	ns		
Fall propagation delay time							
$I \rightarrow Q_E$ [1]	$t_{pdf} \leq$	–	40	–	ns		
	$t_{pdf} \geq$	–	5	–	ns		
$I \rightarrow Q_A$ [1]	$t_{pdf} \leq$	–	30	–	ns		
	$t_{pdf} \geq$	–	12	–	ns		
$I \rightarrow Q$ [1]	$t_{pdf} \leq$	–	38	–	ns		
	$t_{pdf} \geq$	–	15	–	ns		
$I_E \rightarrow Q_E$	$t_{pdf} \leq$	–	45	–	ns		
	$t_{pdf} \geq$	–	18	–	ns		
$I_E \rightarrow Q_A$	$t_{pdf} \leq$	–	31	–	ns		
	$t_{pdf} \geq$	–	14	–	ns		
$I_E \rightarrow Q$	$t_{pdf} \leq$	–	30	–	ns		
	$t_{pdf} \geq$	–	10	–	ns		

[1]) I stands for I_0 to I_7

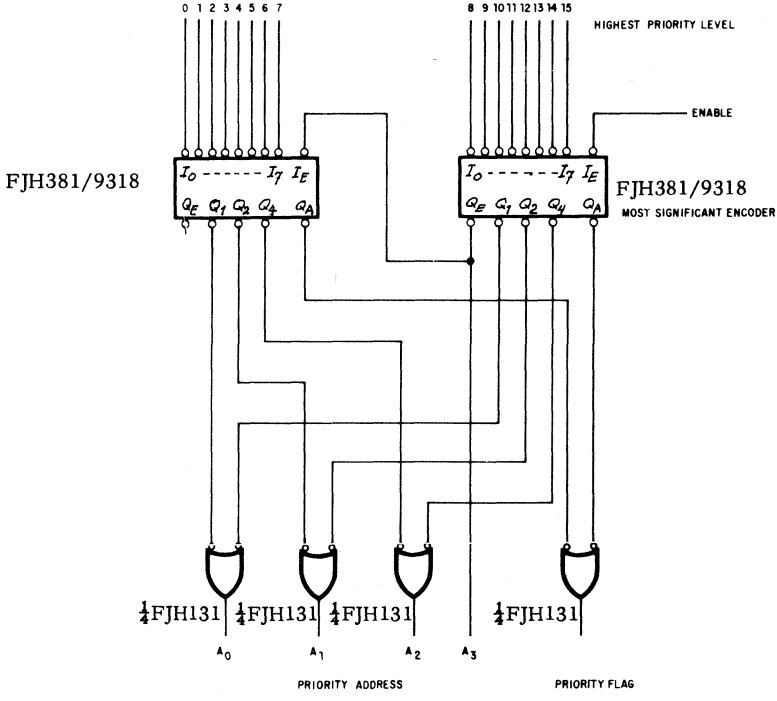
CHARACTERISTICS (continued)





Waveforms illustrating the measurement of t_{pdr} and t_{pdf}

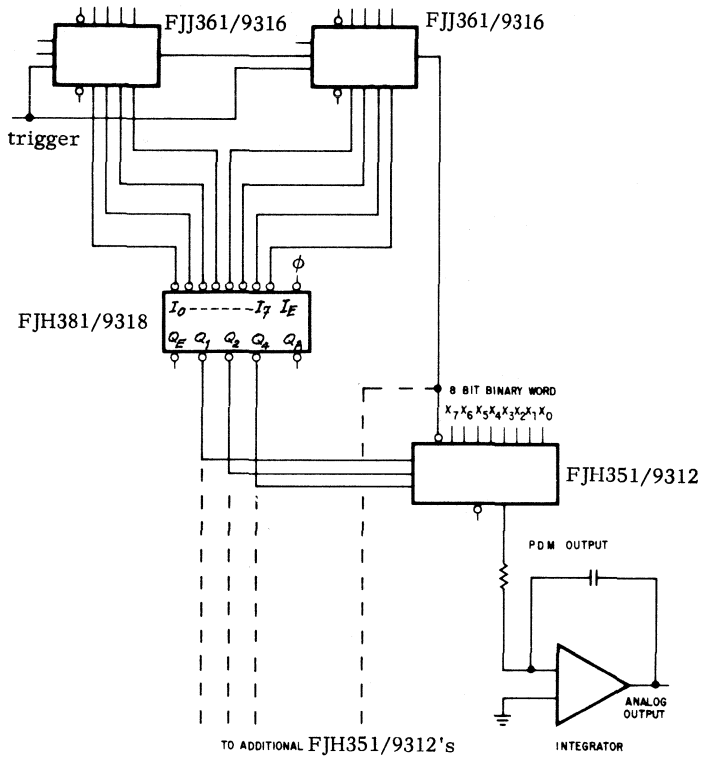
APPLICATION INFORMATION



16 input priority encoder

The number of priority levels can be increased by cascading FJH381/9318 encoders. This may be accomplished by connecting the most significant encoder's enable output Q_E to the next most significant encoder's enable input I_E.

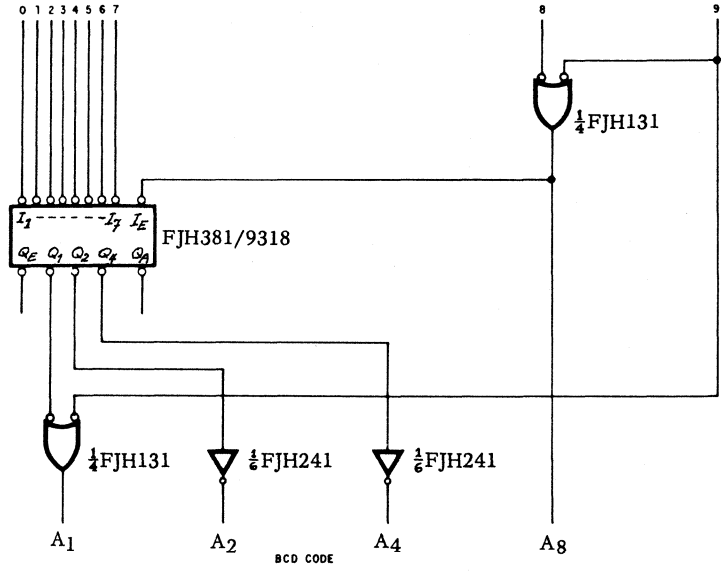
APPLICATION INFORMATION (continued)



Multiple channel D/A converter

The FJH381/9318 supplies a code sequence to the multiplexer, such that the most significant binary input is sampled for 50 % of the count cycle, the next most significant input is sampled for 25 % of the cycle, and so on.
This sampling produces a PDM output which can be integrated or in many cases, such as panel meters, motors, or audio speakers, fed directly to the analog output device. For each additional channel, a multiplexer and integrator are required.

APPLICATION INFORMATION (continued)



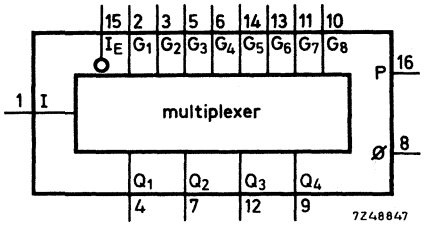
Decimal to BCD converter

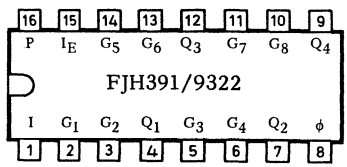
The converter produces a BCD code corresponding to the most significant active LOW decimal input.

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

QUADRUPLE 2-INPUT DIGITAL MULTIPLEXER



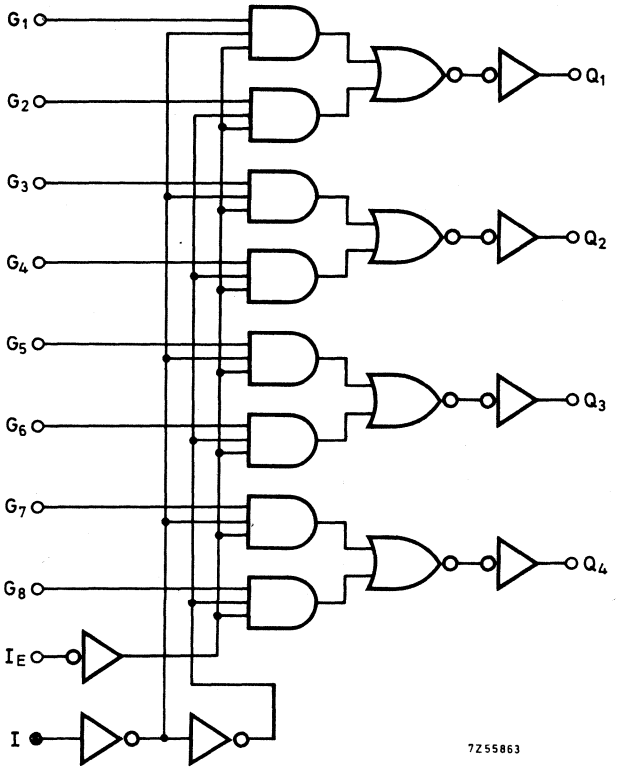


QUICK REFERENCE DATA				
Supply voltage	V_P		5.0 ± 5 %	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Propagation delay time	t_{pd}	typ.	20	ns
D.C. noise margin (full temperature range)	M_L	≥	0.4	V
Average power consumption	P_{av}	typ.	150	mW

The FJH391/9322 is a high speed digital multiplexer. It consists of four 2-input multiplexing circuits with common select and enable logic, each circuit consists of two inputs and one output. Each output is fully buffered.

PACKAGE OUTLINE 16 lead plastic dual in line (type A) (See General Section).

LOGIC DIAGRAM



LOGIC FUNCTIONS

$Q_1 = I_E \cdot (G_2 \cdot I + G_1 \cdot \bar{I})$ $\quad Q_3 = I_E \cdot (G_6 \cdot I + G_5 \cdot \bar{I})$

$Q_2 = I_E \cdot (G_4 \cdot I + G_3 \cdot \bar{I})$ $\quad Q_4 = I_E \cdot (G_8 \cdot I + G_7 \cdot \bar{I})$

FUNCTIONAL DESCRIPTION

The FJH391/9322 allows the selection of four bits of either data or control from two sources in one package. Information is passed from input to output when input I_E is LOW. When I_E is switched to HIGH, all outputs are LOW regardless of the state of the other inputs. The logic function is that of a four-pole two-position switch, where the position of the switch is set by the logic level supplied to the I-input. A common use of the multiplexer would be the moving of data from a group of registers to four common output lines. The particular register from which the data came would be determined by the state of the I-input. The FJH391/9322 can also be used as a function generator. For example, it is able to generate four functions of two variables with one variable in common.

FUNCTION TABLE (identical for each multiplexer)

ENABLE input	SELECT input	DATA inputs		Output
$\bar{I}_E$	I	G_1	G_2	Q_1
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

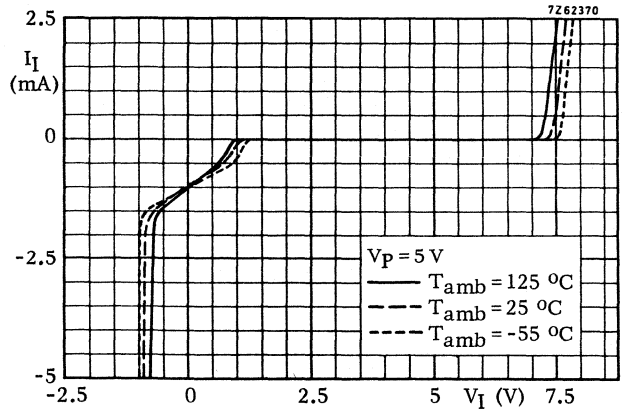
Supply voltage	V_p	−0.5 to +7.0	V
Input voltage (all inputs)	V_I	−0.5 to +5.5	V [1]
Input current (all inputs)	I_I	−30 to +5.0	mA [1]
Output voltage (output in HIGH state)	V_Q	−0.5 to V_P	V
Output current (output in LOW state)	I_Q	max. 30	mA
Storage temperature	T_{stg}	−65 to +150	°C
Operating ambient temperature	T_{amb}	0 to +70	°C

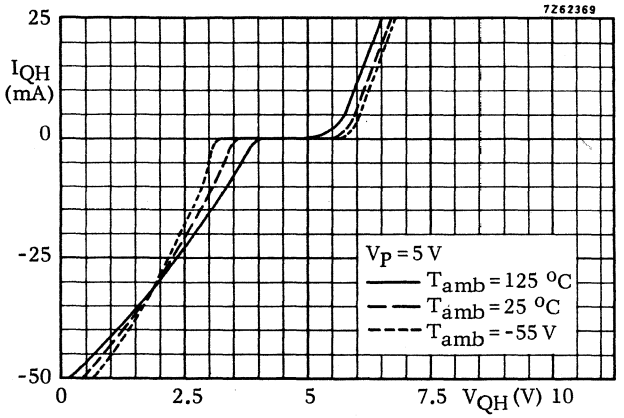
[1]) Either input voltage or input current limit is sufficient to protect the inputs.

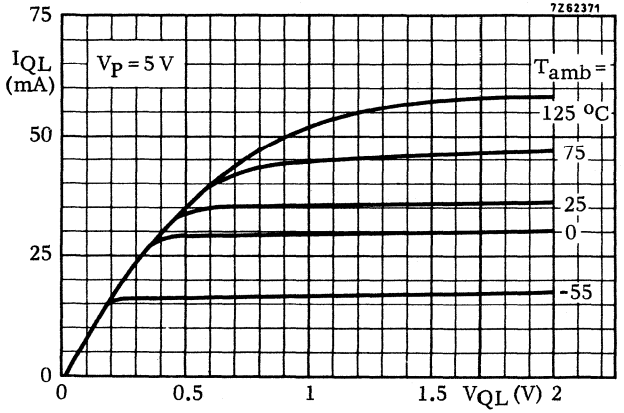
CHARACTERISTICS

		T_{amb} (°C) 0	25	70	Conditions and references V_P (V)	
STATIC DATA						
Voltages						
Input threshold LOW (any input)	V_{ILmax}	0.8	0.8	0.8 V		
Input threshold HIGH (any input)	V_{IHmin}	2.0	2.0	2.0 V		
Output LOW	V_{QLmax}	0.4	0.4	0.4 V	4.75 5.25	$I_{QL} = I_{QLmax}$ [1]
Output HIGH	V_{QHmin}	2.4	2.4	2.4 V	4.75	$-I_{QH} = -I_{QHmax}$ [1]
Currents						
Input LOW (all inputs)	$-I_{ILmax}$ $-I_{ILmax}$	1.41 1.6	1.41 1.6	1.41 mA 1.6 mA	4.75 5.25	$V_I = V_{QLmax}$
Input HIGH (all inputs)	I_{IHmax}	60	60	60 µA	5.25	V_I = 4.5 V
Output LOW	I_{QLmax} I_{QLmax}	14.1 16.0	14.1 16.0	14.1 mA 16.0 mA	4.75 5.25	
Output HIGH	$-I_{QHmax}$	1.2	1.2	1.2 mA	4.75	
SUPPLY DATA						
Supply current	I_P typ. I_P <	— 45	30 45	— mA 45 mA	5.0 5.0	
DYNAMIC DATA						
Rise propagation delay time I → Q	t_{pdr} typ. t_{pdr} <	— —	17 30	— ns — ns	5.0 5.0	C_L = 15 pF
Fall propagation delay time I → Q	t_{pdf} typ. t_{pdf} <	— —	20 31	— ns — ns	5.0 5.0	C_L = 15 pF

[1]) Inputs at threshold voltage (V_{ILmax} or V_{IHmin}) as shown in the function table on page 3.

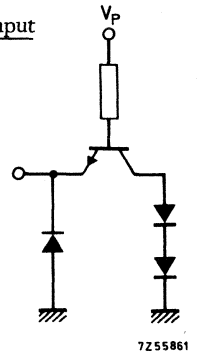




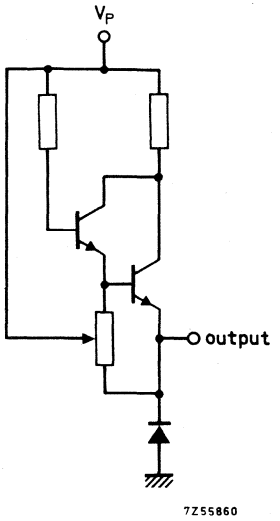


Equivalent circuit

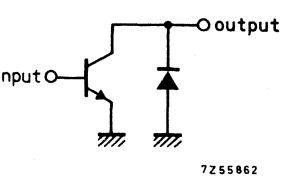
Input



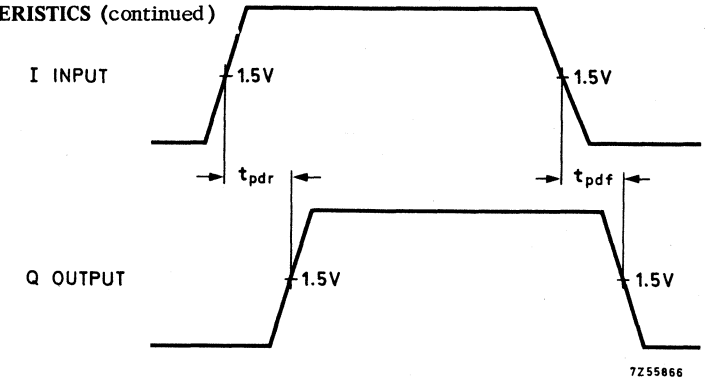
Output HIGH



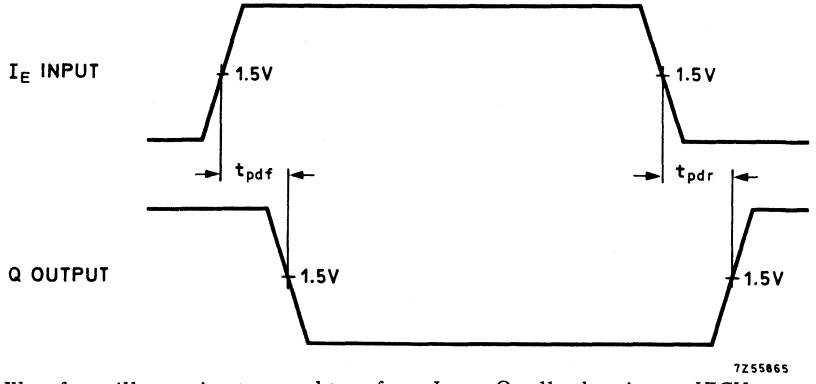
Output LOW



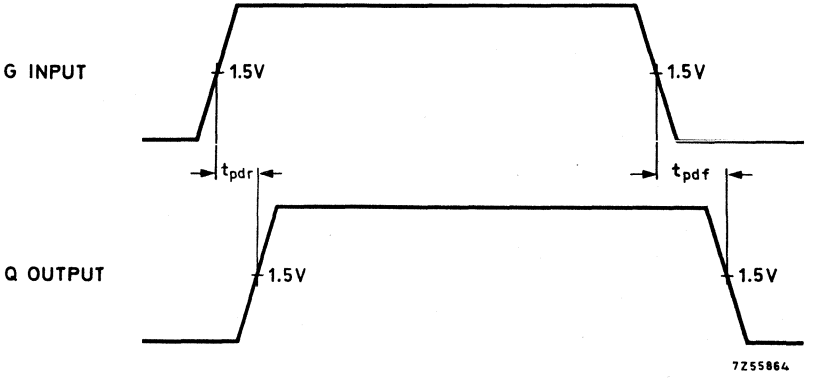
CHARACTERISTICS (continued)



Waveform illustrating t_{pdr} and t_{pdf} from I→Q; pins 2 and 15 = ϕ; pin 3 = V_P

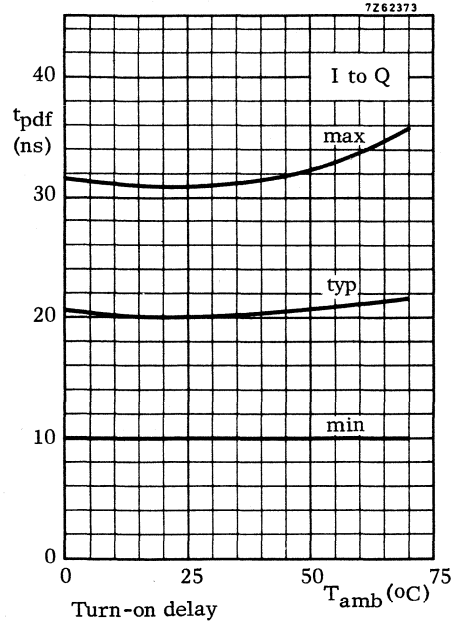


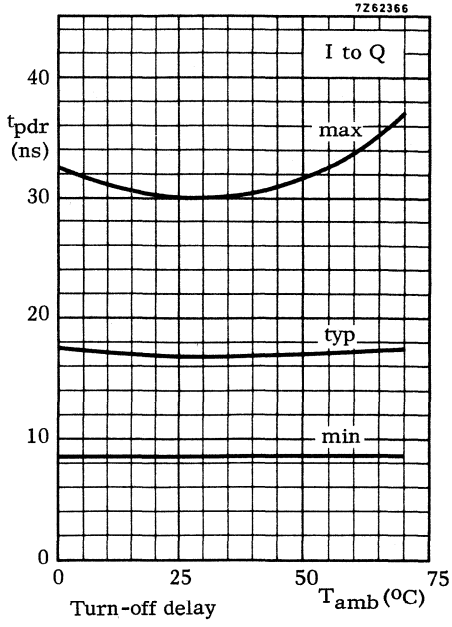
Waveform illustrating t_{pdr} and t_{pdf} from I_E→Q; all other inputs HIGH

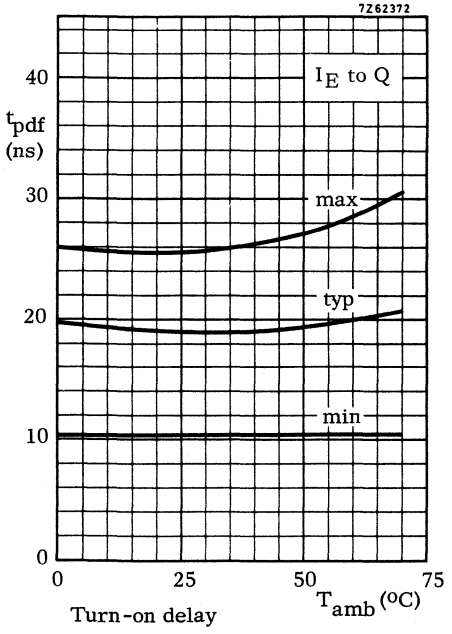


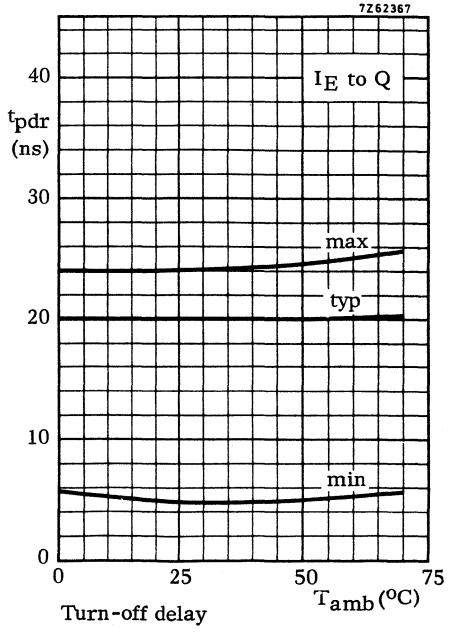
Waveform illustrating t_{pdr} and t_{pdf} from G→Q; pins 1 and 15 = ϕ

CHARACTERISTICS (continued)

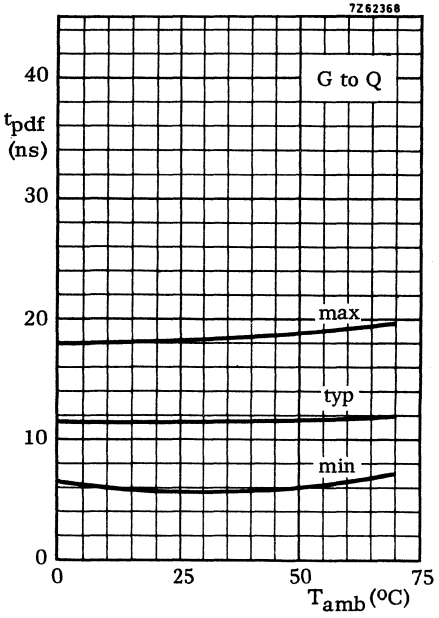




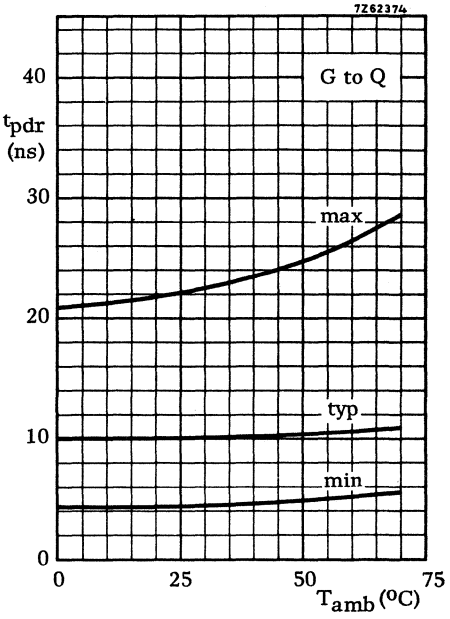




CHARACTERISTICS (continued)

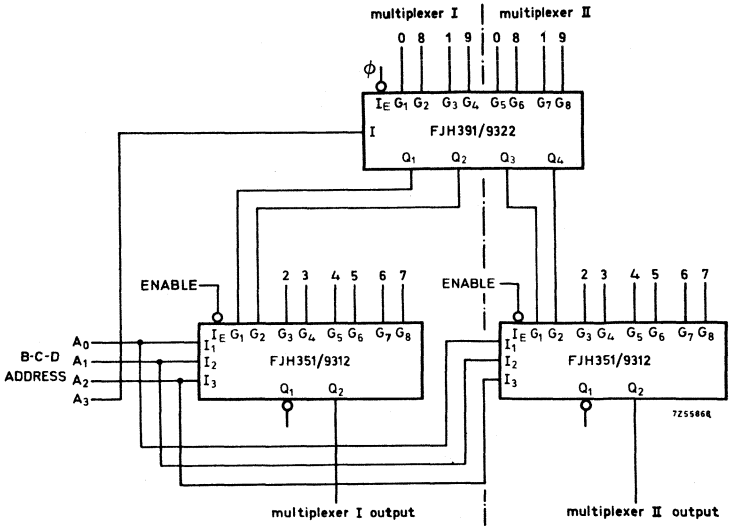


Turn-on delay

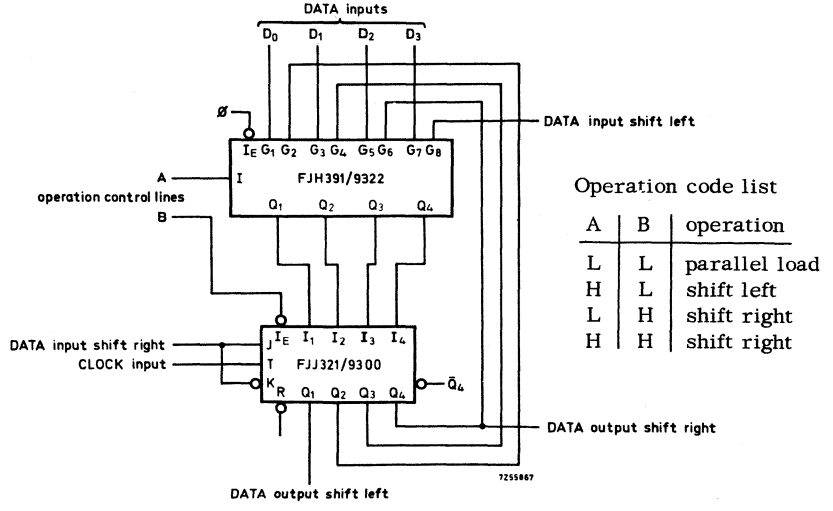


Turn-off delay

APPLICATION INFORMATION



Dual 10-input multiplexer



Operation code list

A	B	operation
L	L	parallel load
H	L	shift left
L	H	shift right
H	H	shift right

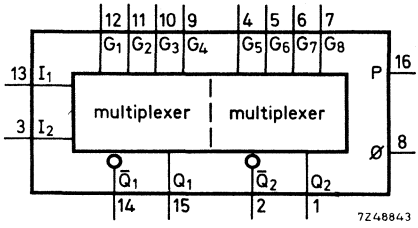
Shift left, shift right, parallel load register

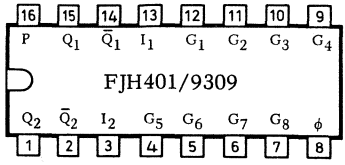
This register will shift left, shift right, and load 4-bits of parallel data according to the operation code applied to A and B.

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

DUAL 4-INPUT MULTIPLEXER





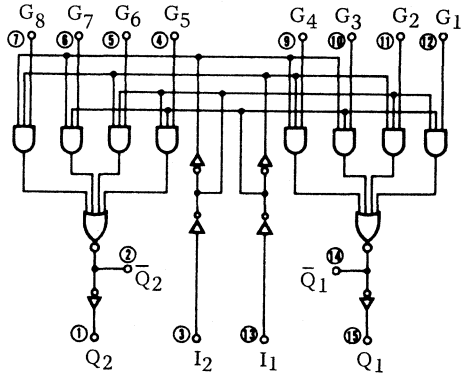
QUICK REFERENCE DATA				
Supply voltage	V_P		5.0 ± 5 %	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Propagation delay time	t_{pd}	typ.	24	ns
Available d.c. fan-out	N_a	≥	10	
D.C. noise margin (full temperature range)	M_L	≥	0.4	V
Average power dissipation (total)	P_{av}	typ.	150	mW

PACKAGE OUTLINE 16 lead plastic dual in-line (type A) (See General Section).

GENERAL DESCRIPTION

The FJH401/9309 is a monolithic, high speed, dual four-input digital multiplexer, consisting of two multiplexing circuits with common input select logic. Each circuit contains four inputs and fully buffered complementary outputs. In addition to operating as a multiplexer, the FJH401/9309 can generate any two functions of three variables. Active pull-ups in the outputs ensure high drive and high speed performance. Because of its high speed performance and on-chip select decoding, the device may be cascaded to multiple levels so that any number of lines can be multiplexed onto a single output terminal.

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The FJH401/9309 provides the possibility in one package, of selecting two bits of either data or control information from up to four sources. This device is the logical implementation of a two-pole four-position switch; the switch position is determined by the logic levels applied to the two select inputs (I). Complementary outputs are provided for both multiplexers.
The logic equations for the outputs are:

$$Q_1 = G_1 \cdot \bar{I}_1 \cdot \bar{I}_2 + G_2 \cdot \bar{I}_1 \cdot I_2 + G_3 \cdot I_1 \cdot \bar{I}_2 + G_4 \cdot I_1 \cdot I_2$$

$$Q_2 = G_5 \cdot \bar{I}_1 \cdot \bar{I}_2 + G_6 \cdot \bar{I}_1 \cdot I_2 + G_7 \cdot I_1 \cdot \bar{I}_2 + G_8 \cdot I_1 \cdot I_2$$

A common use of the FJH401/9309 would be the moving of data from a group of registers to a common output terminal. The particular register from which the data came would be determined by the state of the select inputs.

FUNCTION TABLE

inputs						outputs	
I_1	I_2	G_1	G_2	G_3	G_4	Q_1	$\overline{Q_1}$
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	H	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L
I_1	I_2	G_5	G_6	G_7	G_8	Q_2	$\overline{Q_2}$
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	H	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P		−0.5 to +7.0	V
Input voltage [1])	All inputs		−0.5 to +5.5	V
Input current [1])	All inputs		−30 to +5.0	mA
Output voltage (HIGH state)	V_Q		0 to V_P	V
Output current (LOW state)	I_Q	max.	30	mA
Storage temperature	T_{stg}		- 65 to +150	°C
Operating ambient temperature	T_{amb}		0 to +70	°C

[1]) Either input voltage or input current limit is sufficient to protect the inputs.

CHARACTERISTICS

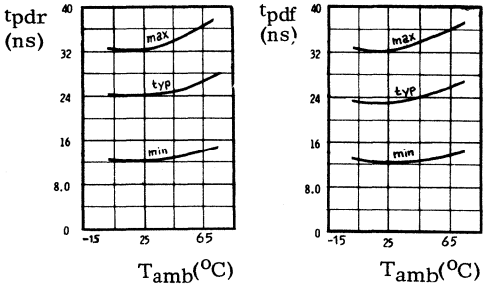
		T_{amb} (°C)				Conditions and references	
		0	25	70		V_P (V)	
STATIC DATA							
Voltages [1]							
Input threshold LOW (any input)	V_{GLmax}	0.8	0.8	0.8	V		
Input threshold HIGH (any input)	V_{GHmin}	2.0	2.0	2.0	V		
Output LOW:							
Q_1; Q_2	V_{QLmax}	0.4	0.4	0.4	V	5.25	$I_{QL} = I_{QLmax}$
$\overline{Q}_1$; $\overline{Q}_2$	$V_{\overline{Q}Lmax}$	0.4	0.4	0.4	V	5.25	$I_{\overline{Q}L} = I_{\overline{Q}Lmax}$
Output HIGH;							
Q_1; Q_2	V_{QHmin}	2.4	2.4	2.4	V	4.75	$-I_{QH} = -I_{QHmax}$
$\overline{Q}_1$; $\overline{Q}_2$	$V_{\overline{Q}Hmin}$	2.4	2.4	2.4	V	4.75	$-I_{QH} = -I_{\overline{Q}Hmax}$
Currents							
Input LOW	$-I_{GLmax}$	1.6	1.6	1.6	mA	5.25	$V_G = V_{QLmax}$
Input HIGH	I_{GHmax}	–	60	60	µA	5.25	$V_G = 4.5$ V
Output LOW:							
Q_1; Q_2	I_{QLmax}	16	16	16	mA	5.25	$V_Q = V_{QLmax}$
$\overline{Q}_1$; $\overline{Q}_2$	$I_{\overline{Q}Lmax}$	14.4	14.4	14.4	mA	5.25	$V_{\overline{Q}} = V_{\overline{Q}Lmax}$
Output HIGH:							
Q_1; Q_2	$-I_{QHmax}$	–	1.2	1.2	mA	4.75	$V_Q = V_{QHmin}$
$\overline{Q}_1$; $\overline{Q}_2$	$-I_{\overline{Q}Hmax}$	–	1.08	1.08	mA	4.75	$V_{\overline{Q}} = V_{\overline{Q}Hmin}$
SUPPLY DATA							
Supply current	$I_P \leq$	43	43	43	mA	5.0	
	I_P typ.	–	30	–	mA	5.0	

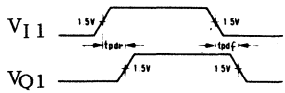
[1] Input voltages at threshold (either V_{GHmin} or V_{GLmax})

CHARACTERISTICS (continued)

		T_{amb} (°C)				Conditions and references	
		0	25	70		V_P (V)	
DYNAMIC DATA							
Performance							
Rise propagation delay time							
I → Q	t_{pdr} ≤	–	32	–	ns	5	C_L = 15 pF
	t_{pdr} typ.	–	24	–	ns	5	
I → $\overline{Q}$	t_{pdr} typ.	–	16	–	ns	5	
G → $\overline{Q}$	t_{pdr} typ.	–	8	–	ns	5	
Fall propagation delay time							
I → Q	t_{pdf} ≤	–	32	–	ns	5	C_L = 15 pF
	t_{pdf} typ.	–	24	–	ns	5	
I → $\overline{Q}$	t_{pdf} typ.	–	16	–	ns	5	
G → $\overline{Q}$	t_{pdf} typ.	–	9	–	ns	5	

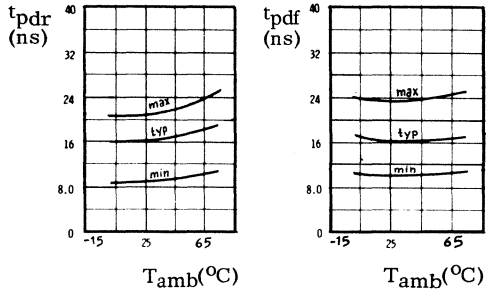
CHARACTERISTICS (continued) at V_P = 5 V; C_L = 15 pF

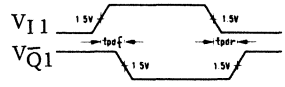




$I_2 = G_1 = \phi$
$G_2 = P$

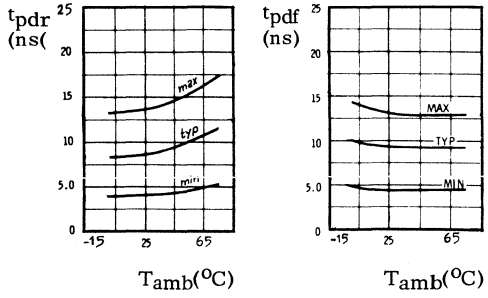
Switching curves and waveforms from $I_1 \rightarrow Q_1$

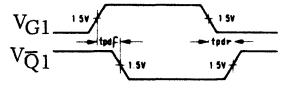




$I_2 = G_1 = \phi$
$G_2 = P$

Switching curves and waveforms from $I_1 \rightarrow \overline{Q}_1$

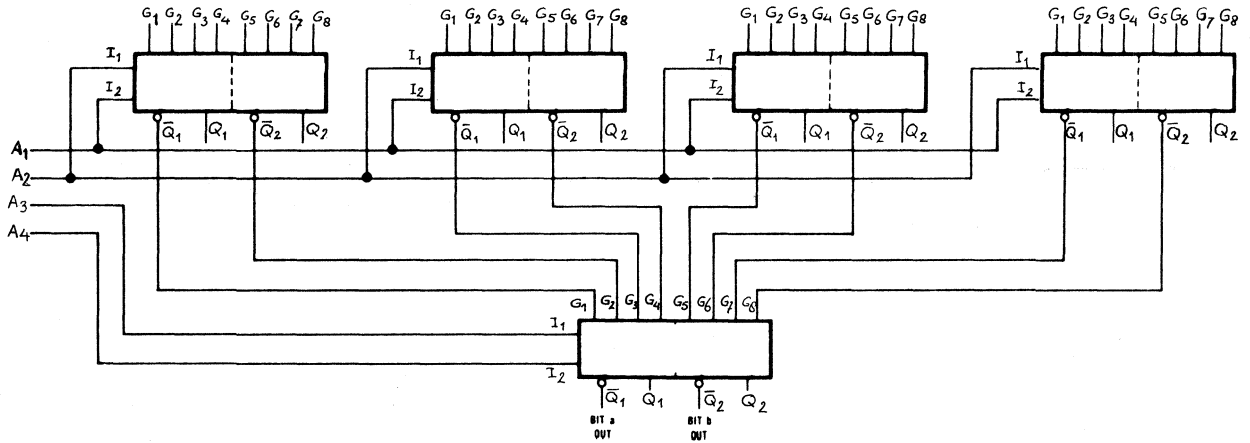




$I_1 = I_2 = \phi$

Switching curves and waveforms from $G_1 \rightarrow \overline{Q}_1$

APPLICATION INFORMATION



Multiplexing two bits from sixteen sources

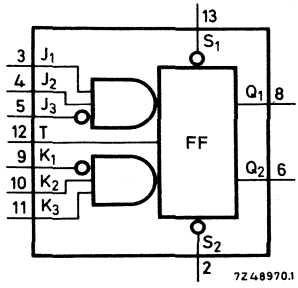
This diagram shows the interconnection of five FJH401/9309 dual four bit multiplexers to provide switching of two bits of data from one of sixteen words into a two bit data terminal. The selection of which word will be transferred to the terminal is made by the address supplied to the A_1, A_2, A_3 and A_4 inputs.

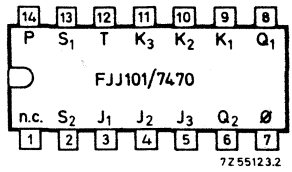
As an example: if twelve bit words are to be transferred to a twelve bit terminal, the above diagram would be repeated six times. Notice that the inverted outputs are used at both levels resulting in the positive output at a higher speed due to the fact that the through delay is less on the inverted output. If the word selecting address is held in four FJ flip-flops (two packages) enough load capability is available to select between sixteen, sixteen bit words.

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

SINGLE JK FLIP-FLOP (AND INPUTS)



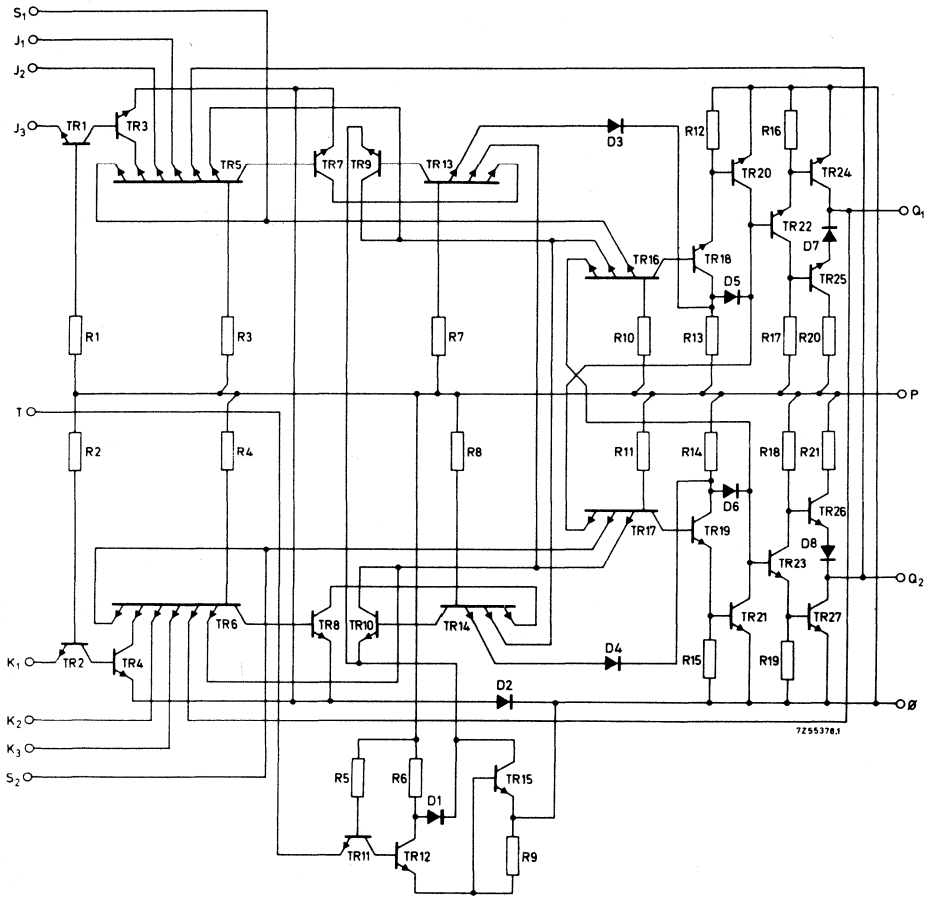


QUICK REFERENCE DATA				
Supply voltage	V_P	$5.0 \pm 5\%$		V
Operating ambient temperature range	T_{amb}	0 to +70		°C
Available d.c. fan-out (full temperature range)	N_a	≥	10	
Max. operating frequency; T_{amb} = 25 °C	f		20	MHz
Average power consumption; T_{amb} = 25 °C	P_{av}	typ.	70	mW

The FJJ101/7470 is a monolithic, edge-triggered JK flip-flop with gated inputs, direct S_1 and S_2 inputs, and complementary Q_1 and Q_2 outputs. It is suited for medium and high speed applications. In systems where input gating is required, its use can lead to a lower package count and reduced system power dissipation. Input information is transferred to the outputs in time with the positive-going edge of the trigger pulse. Direct-coupled input triggering occurs as soon as the trigger pulse reaches a fixed threshold voltage; thereafter the gated inputs are locked out.

PACKAGE OUTLINE: 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAM



FUNCTION TABLE

t_n		t_{n+1}
J*	K**	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q_n}$

* $J = J_1 \cdot J_2 \cdot \overline{J_3}$

** $K = \overline{K_1} \cdot K_2 \cdot K_3$

S_1 and S_2 function can only occur when T is LOW.

H=HIGH state (the more positive voltage)

L=LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	7.0 V
Input voltage	V_J, V_K, V_T, V_S	max.	5.5 V[1]
Peak negative input voltage (J, K, T, S)	$-V_M$	max.	2 V[2]
Storage temperature	T_{stg}		-65 to +150 °C
Operating ambient temperature	T_{amb}		0 to +70 °C

[1] In addition the input voltage between any two J inputs or between any two K inputs: max. 5.5 V.

[2] Pulse duration t_p = 20 ns; repetition frequency f = 5 MHz; source resistance $R_S \geq 75\ \Omega$.

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references	
		0	25	70		V_P (V)	
STATIC DATA							
Voltages							
Input threshold LOW (any input)	V_{ILmax}	0.8	0.8	0.8	V		
Input threshold HIGH (any input)	V_{IHmin}	2.0	2.0	2.0	V		
Output LOW	V_{QLmax}	0.4	0.4	0.4	V	4.75	$I_Q=I_{QLmax}$
Output HIGH	V_{QHmin}	2.4	2.4	2.4	V	4.75	$-I_Q=-I_{QHmax}$
Currents							
Input LOW (T, J, K)	$-I_{ILmax}$	1.6	1.6	1.6	mA	5.25	$V_I=V_{QLmax}$; $I_Q=0$
Input HIGH (T, J, K)	I_{IHmax}	40	40	40	µA	5.25	$V_I=V_{QHmin}$; $I_Q=0$
Input LOW (S)	$-I_{SLmax}$	3.2	3.2	3.2	mA	5.25	$V_S=V_{QLmax}$; $I_Q=0$
Input HIGH (S)	I_{SHmax}	80	80	80	µA	5.25	$V_S=V_{QHmin}$; $I_Q=0$
Output LOW	I_{QLmax}	16	16	16	mA		
Output HIGH	$-I_{QHmax}$	0.4	0.4	0.4	mA		
Output short circuited see note 1	$-I_{Qscmin}$	18	18	18	mA	5.25	$V_I=0$; $V_Q=0$
	$-I_{Qscmax}$	57	57	57	mA	5.25	

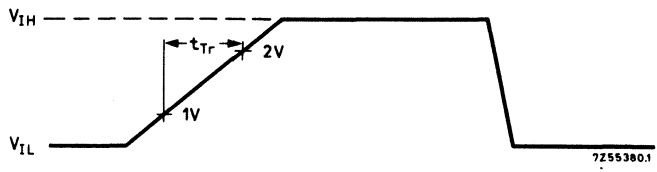
1) Not more than one output should be short circuited at a time.

CHARACTERISTICS (continued)

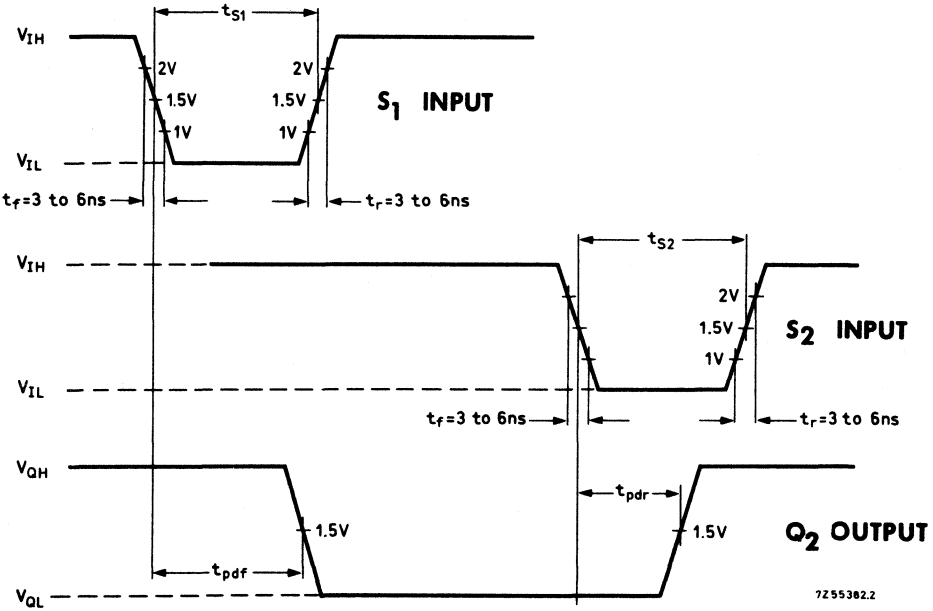
			T_{amb} (°C)				Conditions and references	
			0	25	70		V_P (V)	
SUPPLY DATA								
Supply current	I_P	typ.	-	13	-	mA	5.0	I_Q=0
		<	26	26	26	mA	5.25	
DYNAMIC DATA								
Signal requirements								
Rise time (T input)	t_{Tr}	<	-	150	-	ns	5.0	
Pulse duration (T input)	t_{TH}	>	-	20	-	ns	5.0	
Pulse duration (S input)	t_{SL}	>	-	25	-	ns	5.0	
Performance								
Rise propagation delay time (S→Q)	t_{pdr}	<	-	50	-	ns	5.0	N=10
Fall propagation delay time (S→Q)	t_{pdf}	<	-	50	-	ns	5.0	N=10
Rise propagation delay time (T→Q)	t_{pdr}	>	-	10	-	ns	5.0	N=10
	t_{pdr}	typ.	-	27	-	ns	5.0	
	t_{pdr}	<	-	50	-	ns	5.0	
Fall propagation delay time (T→Q)	t_{pdf}	>	-	10	-	ns	5.0	N=10
	t_{pdf}	typ.	-	18	-	ns	5.0	
	t_{pdf}	<	-	50	-	ns	5.0	
Set-up time (J_3, K_1)	$t_{su\,min}$	<	-	20	-	ns		
Hold time (J_1, J_2, K_2, K_3)	$t_{hold\,min}$	<	-	5	-	ns		
Preset time (S_1)	t_{S1}	>	-	25	-	ns		
Clear time (S_2)	t_{S2}	>	-	25	-	ns		
Maximum operating frequency	f	>	-	20	-	MHz	5.0	N=10
	f	typ.	-	35	-	MHz		

CHARACTERISTICS (continued)

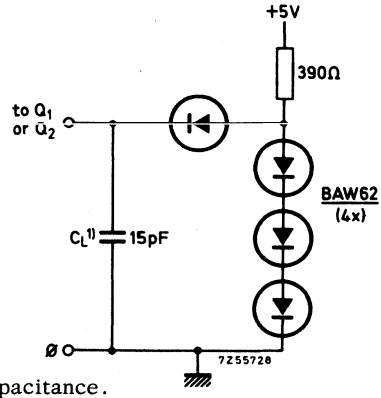
DYNAMIC DATA



Waveform illustrating trigger signal rise time



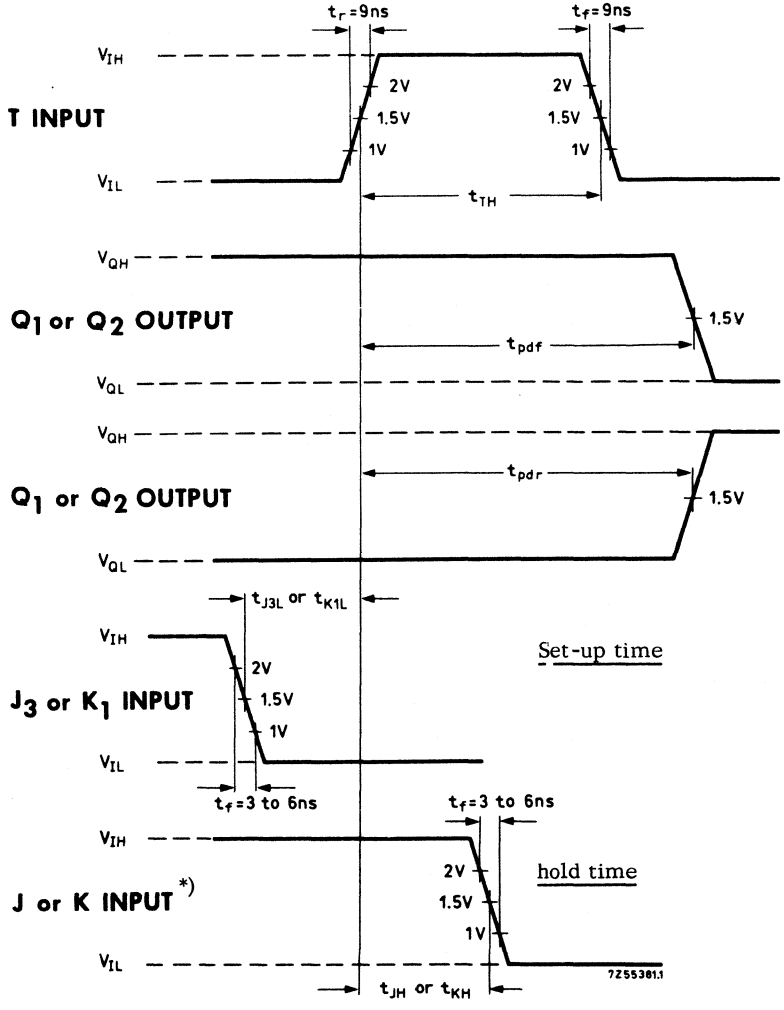
Waveforms illustrating measurement of t_{pdr} and t_{pdf}.



1) Including probe and jig capacitance.

CHARACTERISTICS (continued)

DYNAMIC DATA



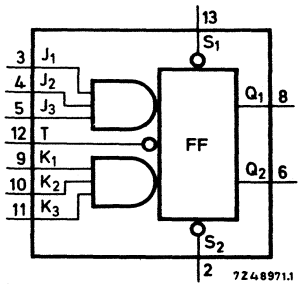
Waveform illustrating switching times.

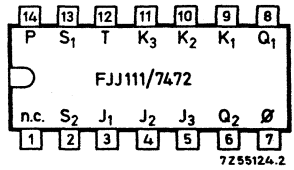
*) J = J_1 or J_2
K = K_2 or K_3

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

SINGLE JK MASTER-SLAVE FLIP-FLOP (AND INPUTS)



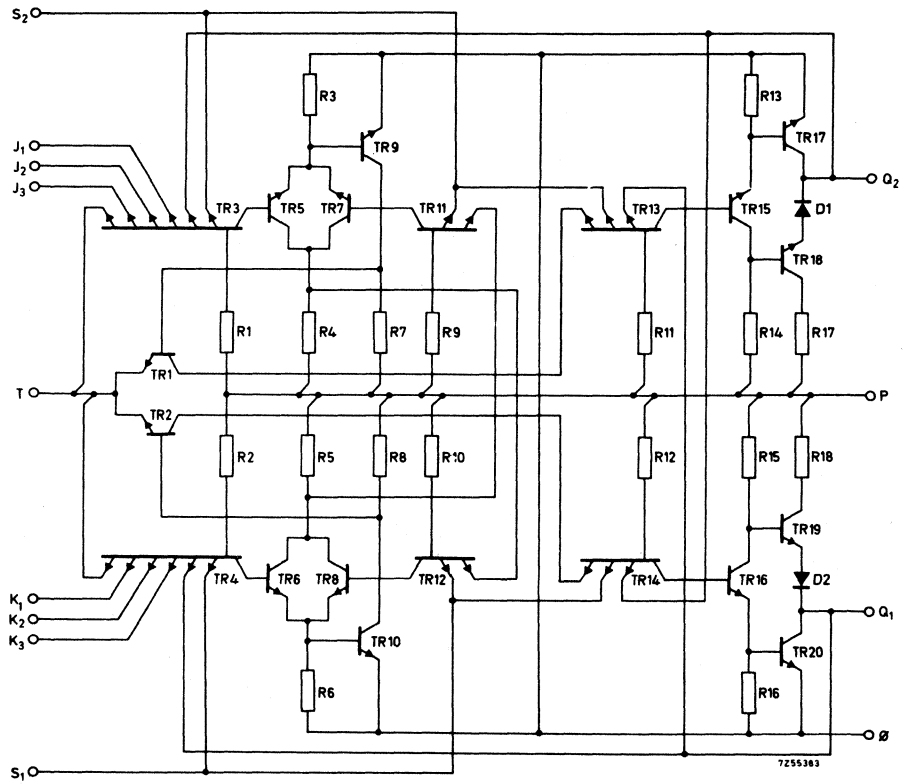


QUICK REFERENCE DATA			
Supply voltage	V_P	5.0 ± 5%	V
Operating ambient temperature range	T_{amb}	0 to +70	°C
Available d.c. fan-out (full temperature range)	N_a	≥ 10	
Max. operating frequency; T_{amb} = 25 °C	f	20	MHz
Average power consumption; T_{amb} = 25 °C	P_{av}	typ. 40	mW

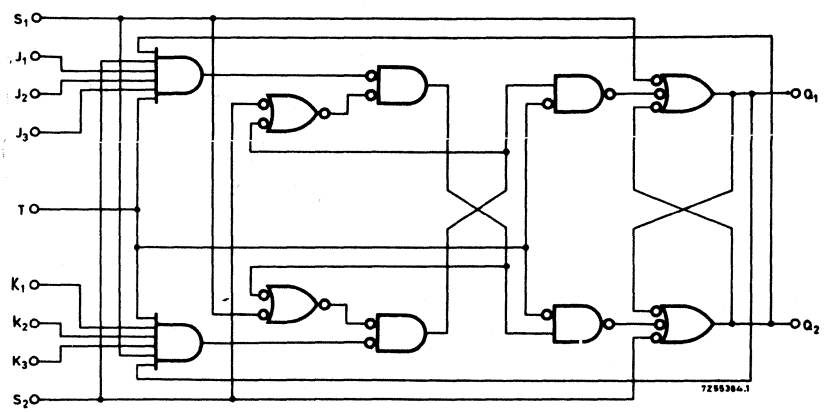
The FJJ111/7472 is a master-slave flip-flop having three J and three K input (AND function). The circuit operates at a frequency up to 15 MHz (typ.). The information at the J and K input enters the master when T is HIGH. Afterwards, when T is LOW, the information is transferred from the master to the slave and appears at the outputs.

PACKAGE OUTLINE: 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAM



LOGIC DIAGRAM



FUNCTION TABLE

t_n		t_{n+1}
J*	K**	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q_n}$

* $J = J_1 \cdot J_2 \cdot J_3$

** $K = K_1 \cdot K_2 \cdot K_3$

S_1 and S_2 functions are independent of T.

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134

Supply voltage	V_P	max.	7.0	V
Input voltage	V_J, V_K, V_T, V_S	max.	5.5	V [1]
Peak negative input voltage (J, K, T, S)	$-V_M$	max.	2	V [2]
Storage temperature	T_{stg}	-65 to +150		°C
Operating ambient temperature	T_{amb}	0 to +70		°C

[1] In addition the voltage between any two J inputs, or between any two K inputs: max. 5.5 V.

[2] Pulse duration t_p = 20 ns; repetition frequency f = 5 MHz; source resistance $R_S \geq 75\ \Omega$.

CHARACTERISTICS

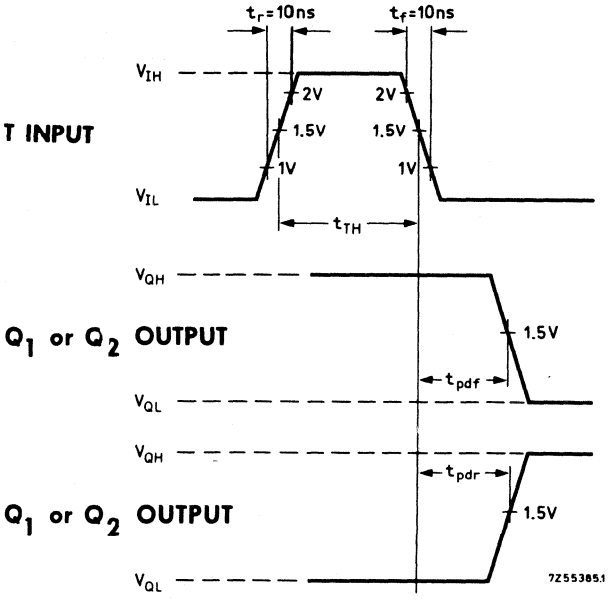
		T_{amb} (°C)				Conditions and references	
		0	25	75		V_P (V)	
STATIC DATA							
Voltages							
Input threshold LOW (any input)	V_{ILmax}	0.8	0.8	0.8	V		
Input threshold HIGH (any input)	V_{IHmin}	2.0	2.0	2.0	V		
Output LOW	V_{QLmax}	0.4	0.4	0.4	V	4.75	$I_Q = I_{QLmax}$
Output HIGH	V_{QHmin}	2.4	2.4	2.4	V	4.75	$-I_Q = -I_{QHmax}$
Currents							
Input LOW (J, K)	$-I_{JLmax}$ $-I_{KLmax}$	1.6	1.6	1.6	mA	5.25	$V_{JK}=V_{QLmax}$; $I_Q=0$
Input HIGH (J, K)	I_{JHmax} I_{KHmax}	40	40	40	μA	5.25	$V_{JK}=V_{QHmin}$; $I_Q=0$
Input LOW (S, T)	$-I_{SLmax}$ $-I_{TLmax}$	3.2	3.2	3.2	mA	5.25	$V_{ST}=V_{QLmax}$; $I_Q=0$
Input HIGH (S, T)	I_{SHmax} I_{THmax}	80	80	80	μA	5.25	$V_{ST}=V_{QHmin}$; $I_Q=0$
Output LOW	I_{QLmax}	16	16	16	mA		
Output HIGH	$-I_{QHmax}$	0.4	0.4	0.4	mA		
Output short circuited	$-I_{Qscmin}$	18	18	18	mA	5.25	$V_I=0$; $V_Q=0$
	$-I_{Qscmax}$	57	57	57	mA		

CHARACTERISTICS (continued)

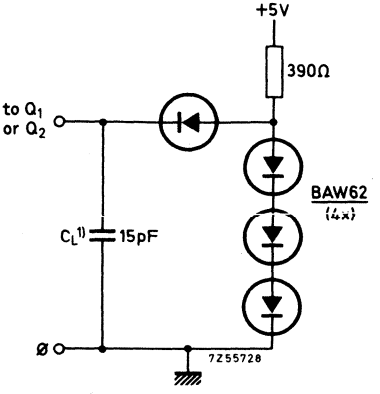
			T_{amb} (°C)				Conditions and references	
			0	25	70		V_P (V)	
SUPPLY DATA								
Supply current	I_P	typ.	-	8	-	mA	5.0	
		<	20	20	20	mA	5.25	
DYNAMIC DATA								
Signal requirements								
Pulse duration (T input)	t_{TH}	>	-	20	-	ns	5.0	
Pulse duration (S input)	t_{SL}	>	-	25	-	ns	5.0	
Performance								
Rise propagation delay time (S→Q)	t_{pdr}	typ.	-	16	-	ns	5.0	N = 10
	t_{pdr}	<	-	25	-	ns		
Fall propagation delay time (S→Q)	t_{pdf}	typ.	-	25	-	ns	5.0	N = 10
	t_{pdf}	<	-	40	-	ns		
Rise propagation delay time (T→Q)	t_{pdr}	>	-	10	-	ns	5.0	N = 10
	t_{pdr}	typ.	-	16	-	ns		
	t_{pdr}	<	-	25	-	ns		
Fall propagation delay time (T→Q)	t_{pdf}	>	-	10	-	ns	5.0	N = 10
	t_{pdf}	typ.	-	25	-	ns		
	t_{pdf}	<	-	40	-	ns		
Set-up time	t_{su}	>	-	20	-	ns		
Clear time	t_c	>	-	0	-	ns		
Maximum operating frequency	f	typ	-	10	-	MHz	5.0	N = 10
		<	-	15	-	MHz		

CHARACTERISTICS (continued)

DYNAMIC DATA



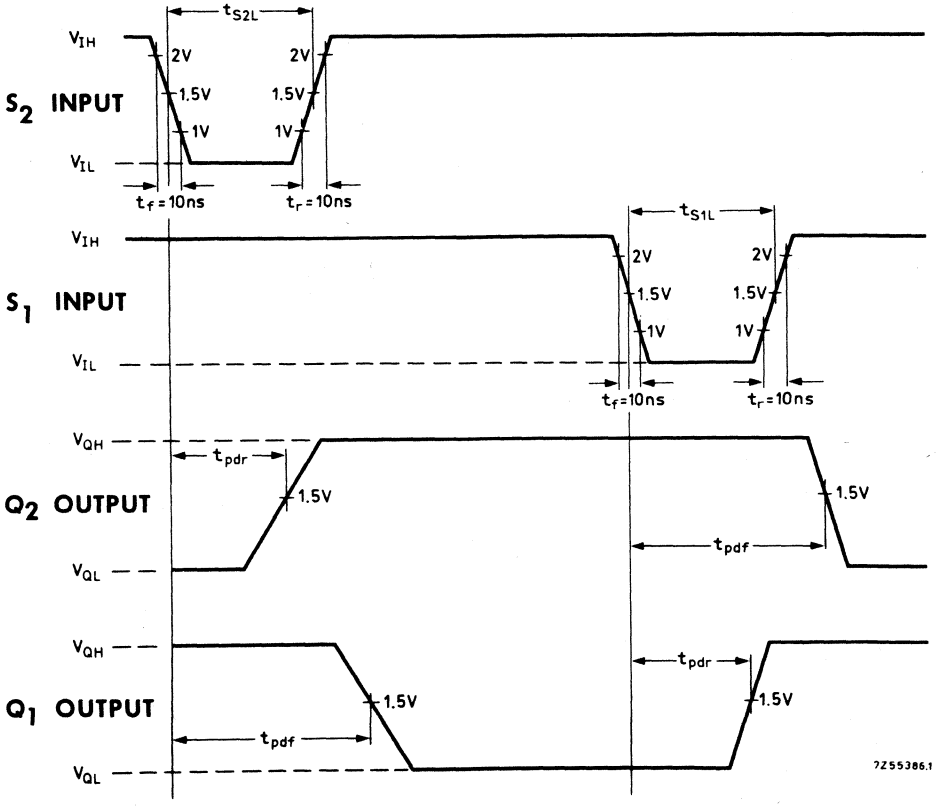
Waveforms illustrating measurement of t_{pdr} and t_{pdf}.



[1]) Including probe and jig capacitance

CHARACTERISTICS (continued)

DYNAMIC DATA

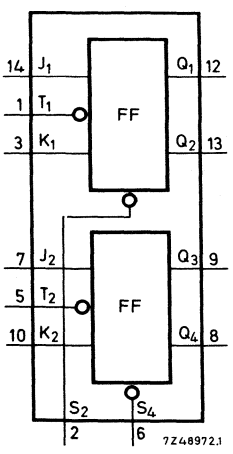


Waveforms illustrating switching times.

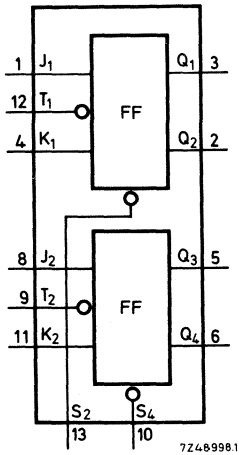
The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

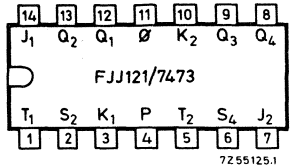
DUAL JK MASTER-SLAVE FLIP-FLOP

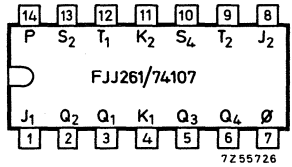


FJJ121/7473



FJJ261/74107



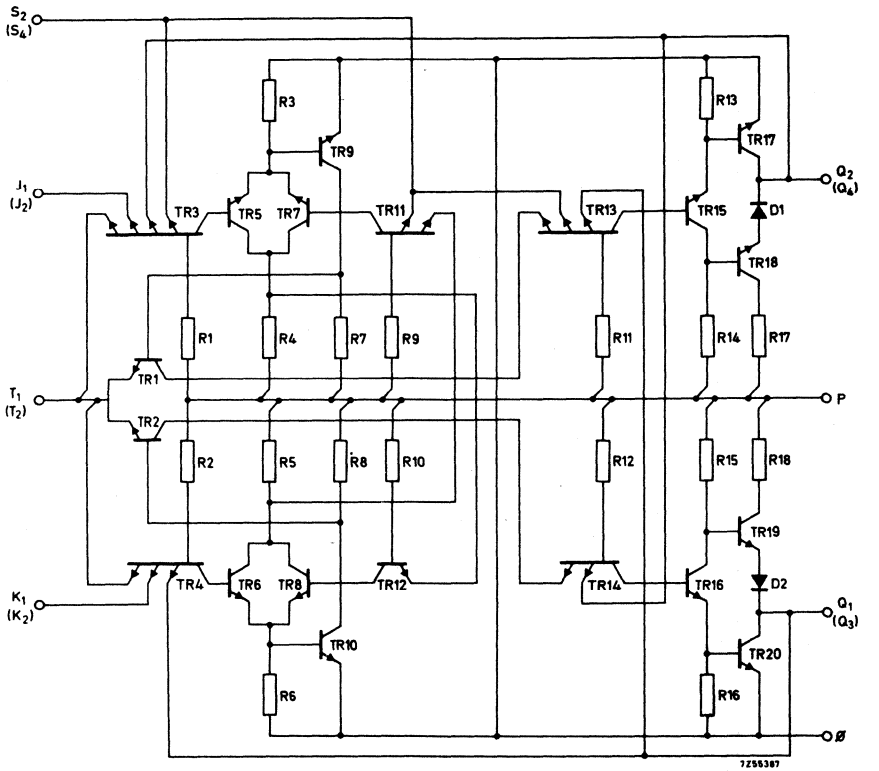


QUICK REFERENCE DATA				
Supply voltage	V_P	5.0 ± 5%		V
Operating ambient temperature range	T_{amb}	0 to +70		°C
Available d.c. fan-out (full temperature range)	N_a	≥	10	
Max. operating frequency; T_{amb} = 25 °C	f		15	MHz
Average power consumption; T_{amb} = 25 °C (per flip-flop)	P_{av}	<	40	mW

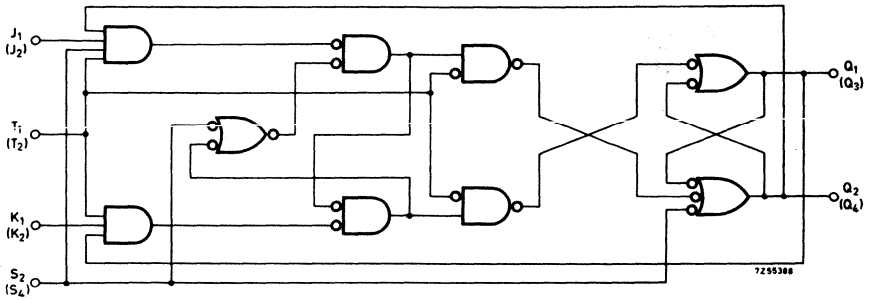
The FJJ121/7473 comprises two independent flip-flops, each provided with one J and one K input and based on the master-slave principle. The circuits operate at a frequency up to 15 MHz (typ.). The information at the J and K inputs enters the master when T is HIGH. Afterwards, when T is LOW, the information is transferred from the master to the slave and appears at the outputs. The FJJ261/74107 is electrically identical to the FJJ121/7473 but has power supply and ground on corner pins. (7 and 14)

PACKAGE OUTLINE: 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAM



LOGIC DIAGRAM



FUNCTION TABLE

t_n		t_{n+1}
J	K	Q_1 (Q_3)
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q_n}$

S_2 and S_4 functions are independent of T_1 and T_2.

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	7.0	V
Input voltage	V_J, V_K, V_S, V_T	max.	5.5	V
Peak negative input voltage (J, K, T, S)	$-V_M$	max.	2	V [1]
Storage temperature	T_{stg}	-65 to	+150	°C
Operating ambient temperature	T_{amb}	0 to	+70	°C

[1] Pulse duration t_p = 20 ns; repetition frequency f = 5 MHz; source resistance $R_S \geq 75\ \Omega$.

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references	
		0	25	70		V_P (V)	
STATIC DATA							
Voltages							
Input threshold LOW (any input)	V_{ILmax}	0.8	0.8	0.8	V		
Input threshold HIGH (any input)	V_{IHmin}	2.0	2.0	2.0	V		
Output LOW	V_{QLmax}	0.4	0.4	0.4	V	4.75	$I_Q = I_{QLmax}$
Output HIGH	V_{QHmin}	2.4	2.4	2.4	V	4.75	$-I_Q = -I_{QHmax}$
Currents							
Input LOW (J, K)	$-I_{JLmax}$ $-I_{KLmax}$	1.6	1.6	1.6	mA	5.25	$V_{JK}=V_{QLmax}; I_Q=0$
Input HIGH (J, K) 1)	I_{JHmax} I_{KHmax}	40	40	40	μA	5.25	$V_{JK}=V_{QHmin}; I_Q=0$
Input LOW (S, T)	$-I_{SLmax}$ $-I_{TLmax}$	3.2	3.2	3.2	mA	5.25	$V_{ST}=V_{QLmax}; I_Q=0$
Input HIGH (S, T) 2)	I_{SLmax} I_{TLmax}	80	80	80	μA	5.25	$V_{ST}=V_{QHmin}; I_Q=0$
Output LOW	I_{QLmax}	16	16	16	mA		
Output HIGH	$-I_{QHmax}$	0.4	0.4	0.4	mA		
Output short circuited see note 3	$-I_{Qscmin}$	18	18	18	mA	5.25	$V_I=0; V_Q=0$
	$-I_{Qscmax}$	57	57	57	mA	5.25	$V_I=0; V_Q=0$

1) I_{JHmax}; I_{KHmax} : 1 mA at V_P = 5.25 V and V_{JK} = 5.5 V.

2) I_{SLmax}; I_{TLmax} : 1 mA at V_P = 5.25 V and V_{ST} = 5.5 V.

3) Not more than one output should be short circuited at a time.

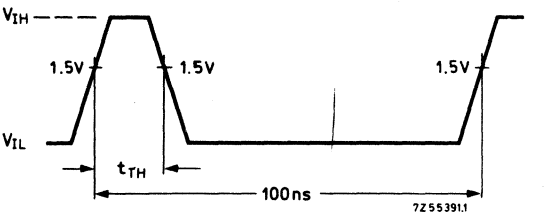
CHARACTERISTICS (continued)

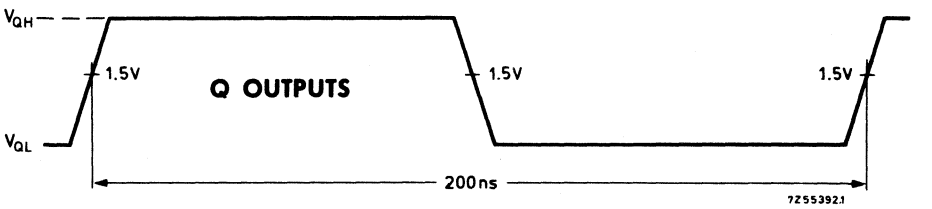
			T_{amb} (°C)				Conditions and references	
			0	25	70		V_P (V)	
SUPPLY DATA								
Supply current	I_P	typ.	–	16	–	mA	5.0	V_I = 5 V
		<	40	40	40	mA	5.25	
DYNAMIC DATA								
Signal requirements								
Pulse duration (T input)	t_{TH}	>	–	20	–	ns	5.0	
Pulse duration (S input)	t_{SL}	>	–	25	–	ns	5.0	
Performance								
Rise propagation delay time (S→Q)	t_{pdr}	typ.	–	16	–	ns	5.0	N = 10
	t_{pdr}	<	–	25	–	ns		
Fall propagation delay time (S→Q)	t_{pdf}	typ.	–	25	–	ns	5.0	N = 10
	t_{pdf}	<	–	40	–	ns		
Rise propagation delay time (T→Q)	t_{pdr}	>	–	10	–	ns	5.0	N = 10
	t_{pdr}	typ.	–	16	–	ns		
	t_{pdr}	<	–	25	–	ns		
Fall propagation delay time (T→Q)	t_{pdf}	>	–	10	–	ns	5.0	N = 10
	t_{pdf}	typ.	–	25	–	ns		
	t_{pdf}	<	–	40	–	ns		
Set-up time	t_{su}	>	–	20	–	ns		
Hold time	t_{hold}	>	–	0	–	ns		
Maximum operating frequency	f	>	–	15	–	MHz	5.0	N = 10
		typ.	–	20	–	MHz		

CHARACTERISTICS (continued)

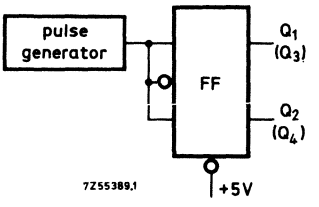
DYNAMIC DATA

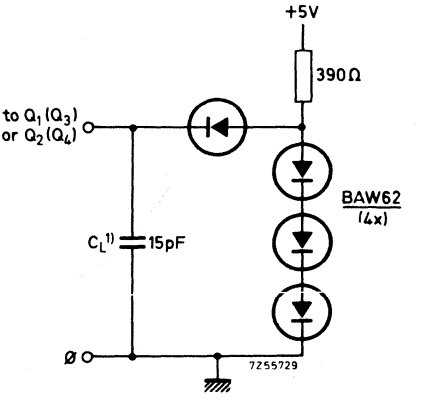
T, J, and K INPUTS





Waveforms illustrating in- and output pulses.



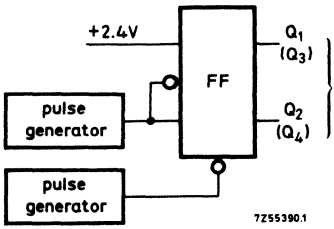


Equivalent load for N = 10

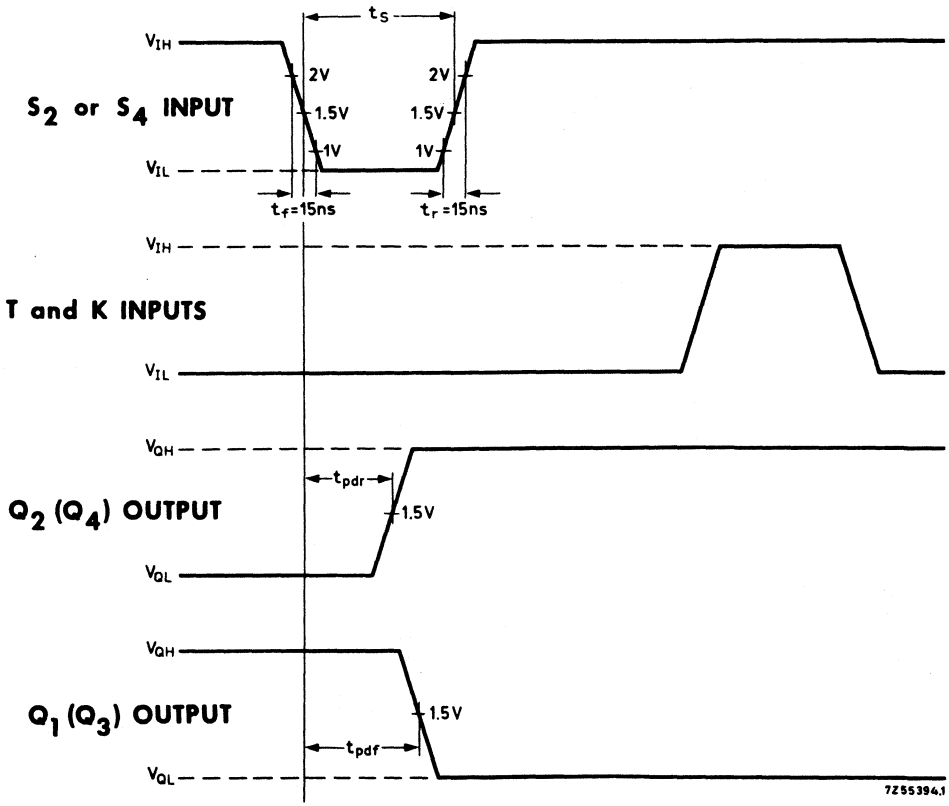
[1]) Including probe and jig capacitance

CHARACTERISTICS (continued)

DYNAMIC DATA



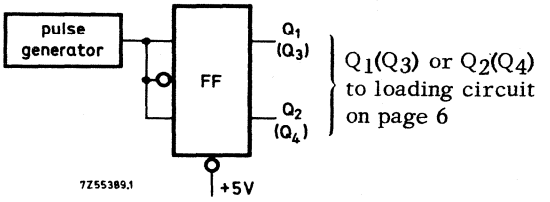
$Q_1(Q_3)$ or $Q_2(Q_4)$ to loading circuit on page 6

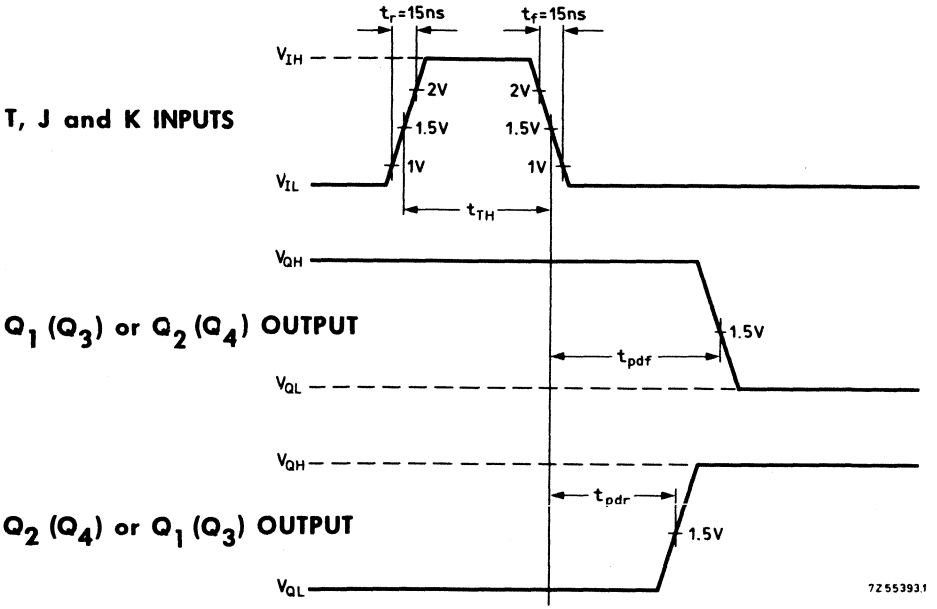


Waveforms illustrating measurement of t_{pdr} and t_{pdf}. (S→Q)

CHARACTERISTICS (continued)

DYNAMIC DATA



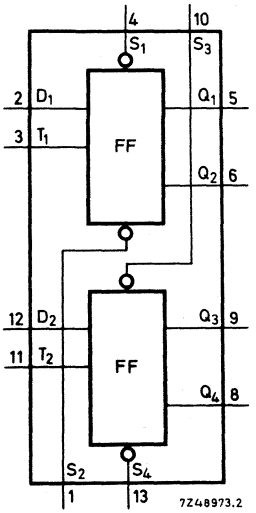


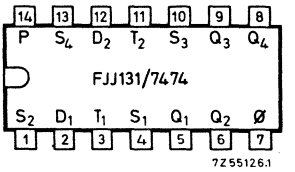
Waveforms illustrating measurement of t_{pdr} and t_{pdf}. (T→Q)

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOP



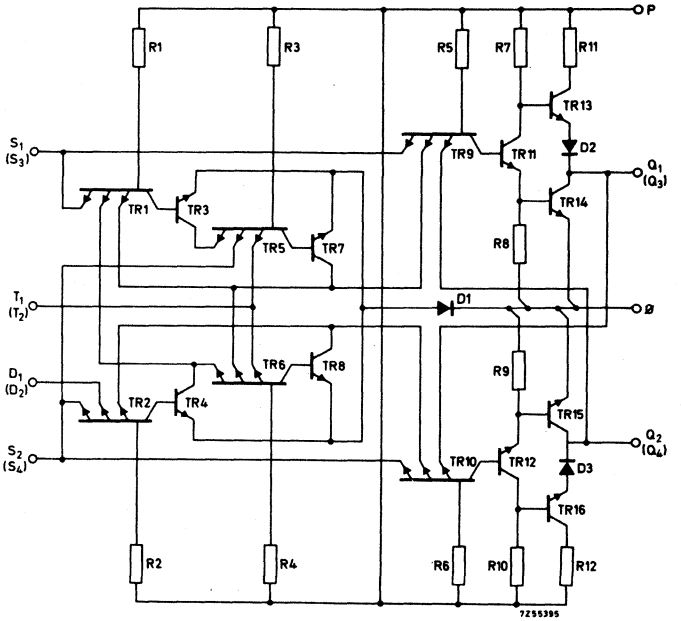


QUICK REFERENCE DATA				
Supply voltage	V_P		5.0 ± 5%	V
Operating ambient temperature range	T_{amb}		0 to + 70	°C
Available d.c. fan-out (full temperature range)	N_a	≥	10	
Max. operating frequency; T_{amb} = 25 °C	f	>	15	MHz
Average power consumption; T_{amb} = 25 °C (per flip-flop)	P_{av}	<	42.5	mW

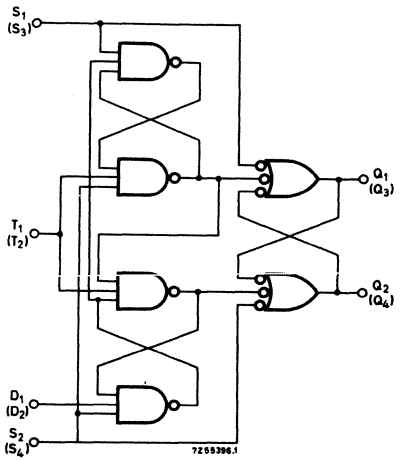
The FJJ131/7474 is an edge-triggered dual D-type flip-flop with direct SET inputs and complementary outputs. On the positive going edge of the clock pulse the information on the D input is transferred to Q_1 (or resp. Q_3).

PACKAGE OUTLINE: 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAM



LOGIC DIAGRAM



FUNCTION TABLE

t_n	t_{n+1}	
D	Q_1	Q_2
L	L	H
H	H	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	7.0	V
Output voltage	V_Q	max.	5.5	V
Input voltage	V_D, V_S, V_T	max.	5.5	V
Peak negative input voltage (D, S, T)	$-V_M$	max.	2	V [1]
Storage temperature	T_{stg}	-65 to	+150	°C
Operating ambient temperature	T_{amb}	0 to	+70	°C

[1]) Pulse duration t_p = 20 ns; repetition frequency f = 5 MHz; source resistance $R_S \geq 75\ \Omega$.

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references	
		0	25	70		V_P (V)	
STATIC DATA							
Voltages							
Input threshold LOW (any input)	V_{ILmax}	0.8	0.8	0.8	V		
Input threshold HIGH (any input)	V_{IHmin}	2.0	2.0	2.0	V		
Output LOW	V_{QLmax}	0.4	0.4	0.4	V	4.75	$I_Q = I_{QLmax}$
Output HIGH	V_{QHmin}	2.4	2.4	2.4	V	4.75	$-I_Q = -I_{QHmax}$
Currents							
Input LOW (S_1,D_1)	$-I_{S1Lmax}$ $-I_{D1Lmax}$	1.6	1.6	1.6	mA	5.25	$V_{S1}, V_{D1} = V_{QLmax}$
Input LOW (S_2,T_1)	$-I_{S2Lmax}$ $-I_{T1Lmax}$	3.2	3.2	3.2	mA	5.25	$V_{S2}, V_{T1} = V_{QLmax}$
Input HIGH (D) 1)	I_{DHmax}	40	40	40	µA	5.25	$V_D = V_{QHmin}$
Input HIGH (S_1,T_1) 2)	I_{S1Hmax} I_{T1Hmax}	80	80	80	µA	5.25	$V_{S1}, V_{T1} = V_{QHmin}$
Input HIGH (S_2) 3)	I_{S2Hmax}	120	120	120	µA	5.25	$V_{S2} = V_{QHmin}$
Output LOW	I_{QLmax}	16	16	16	mA		
Output HIGH	$-I_{QHmax}$	0.4	0.4	0.4	mA		
Output short circuited see note 4	$-I_{Qscmin}$	18	18	18	mA	5.25	$V_Q = 0$
	$-I_{Qscmax}$	57	57	57	mA	5.25	$V_Q = 0$

1) I_{DHmax} = 1 mA at V_P = 5.25 V and V_D = 5.5 V.

2) I_{S1Hmax} ; I_{T1Hmax} : 1 mA at V_P = 5.25 V and $V_{S1} = V_{T1}$ = 5.5 V.

3) I_{S2Hmax} = 1 mA at V_P = 5.25 V and V_{S2} = 5.5 V.

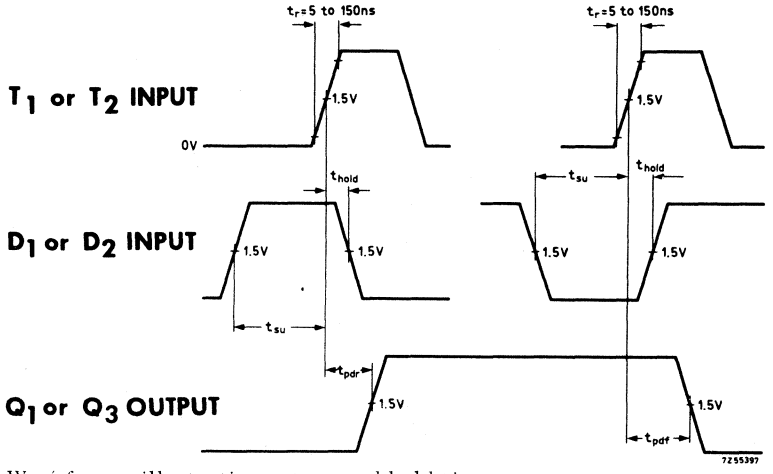
4) Not more than one output should be short circuited at a time.

CHARACTERISTICS (continued)

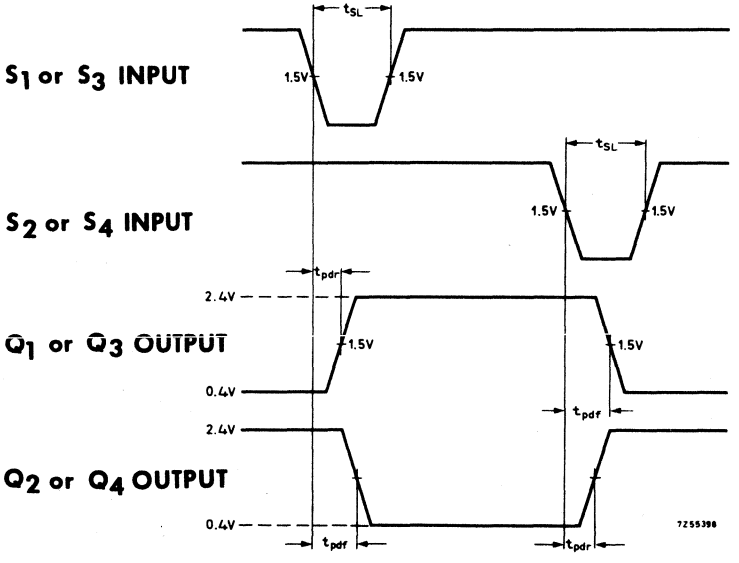
			T_{amb} (°C)				Conditions and references	
			0	25	70		V_P (V)	
SUPPLY DATA								
Supply current	I_P	typ.	-	17	-	mA	5.0	V_I = 5.0 V
		<	30	30	30	mA	5.25	
DYNAMIC DATA								
Signal requirement								
Pulse duration (S, T input)	t_{SL}, t_{TL}	>	30	30	30	ns	5.0	
Performance								
Rise propagation delay time (S→Q)	t_{pdr}	<	-	25	-	ns	5.0	N = 10
Fall propagation delay time (S→Q)	t_{pdf}	<	-	40	-	ns	5.0	N = 10
Rise propagation delay time (T→Q)	t_{pdr}	>	-	10	-	ns	5.0	N = 10
		typ.	-	14	-	ns		
		<	-	25	-	ns		
Fall propagation delay time (T→Q)	t_{pdf}	>	-	10	-	ns	5.0	N = 10
		typ.	-	20	-	ns		
		<	-	40	-	ns		
Set-up time	t_{su}	>	-	20	-	ns		
Hold time	t_{hold}	>	-	5	-	ns		
Maximum operating frequency	f	>	-	15	-	MHz	5.0	N = 10
		typ.	-	25	-	MHz		

CHARACTERISTICS (continued)

DYNAMIC DATA



Waveforms illustrating set-up and hold times.



Waveforms illustrating measurement of t_{pdr} and t_{pdf} (S→Q)

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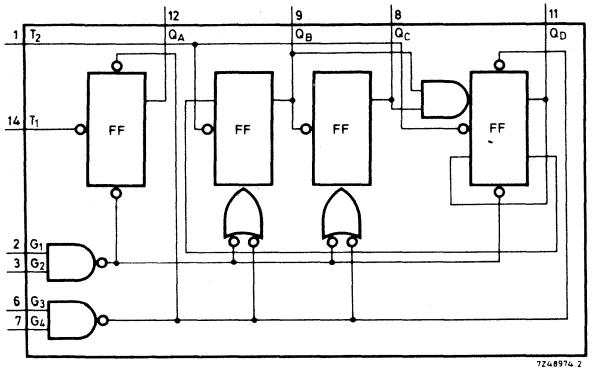
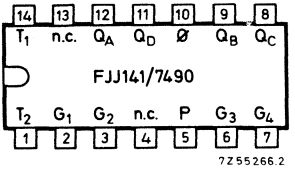
Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

BCD DECADE COUNTER



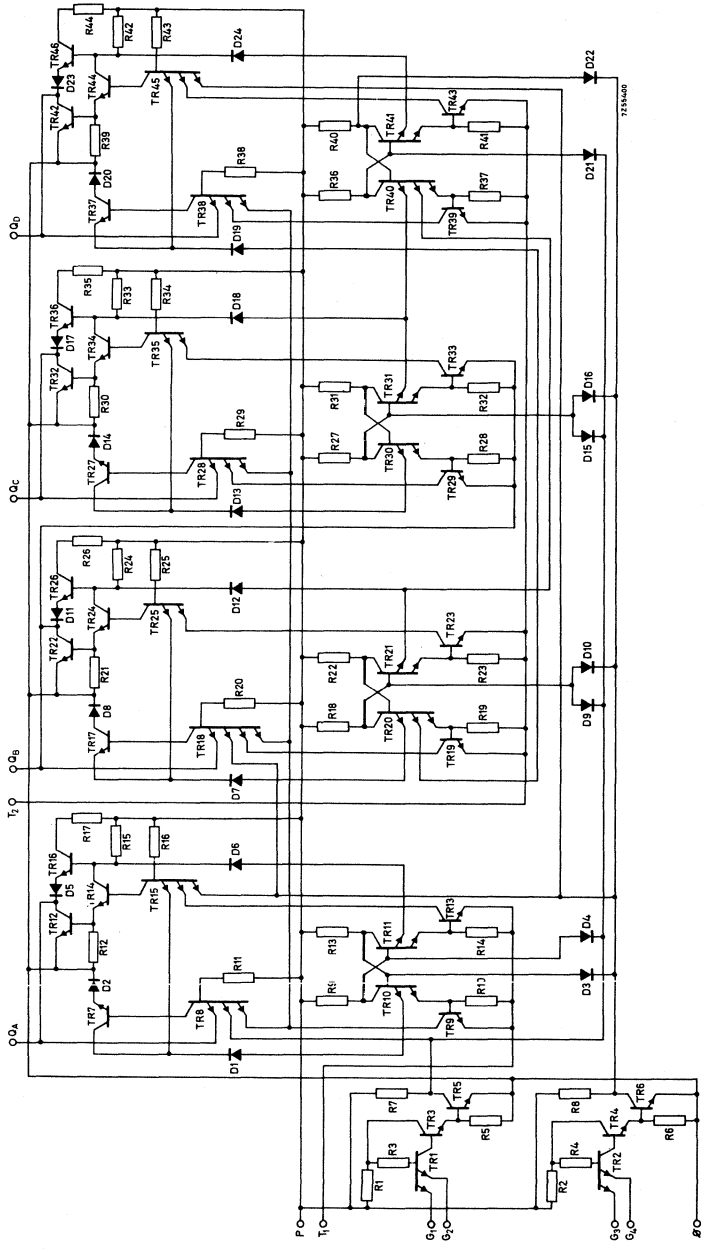


QUICK REFERENCE DATA			
Supply voltage	V_P	5.0 ± 5%	V
Operating ambient temperature	T_{amb}	0 to +70	°C
Max. operating frequency; T_{amb} = 25°C	f_c	≥ 10	MHz
Available d.c. fan-out (full temperature range)	N_a	≥ 10	
Average power consumption T_{amb} = 25 °C	P_{av}	typ. 160	mW

The FJJ141/7490 is a high speed decade counter, consiting of 4 master-slave flip-flops. Gated direct reset lines are provided to inhibit count inputs and return all outputs to a logical zero (inputs G_1, G_2) or to a binary coded (BCD) count of nine (inputs G_3, G_4).

PACKAGE OUTLINE : 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAM



LOGIC FUNCTION

As the output Q_A from the first flip-flop is not internally connected to the succeeding stages, the counter can be used in three different modes.

1. Binary coded decimal decade counter: the T_2 input must be externally connected to the Q_A output. T_1 is then the counter input.
2. Symmetrical divide-by-ten counter for frequency synthesizer or other applications requiring division of a binary count by the power of ten: the Q_D output must be connected to the T_1 input. In this case T_2 becomes counter input and a divide-by-ten square wave is obtained at output Q_A.
3. Divide-by-two counter and a divide-by-five counter: no external interconnections are required.

FUNCTION TABLES

BCD count sequence (output Q_A connected to input T_2)

Count	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

Reset/count

RESET INPUTS				OUTPUTS			
G_1	G_2	G_3	G_4	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	L	H	H	H	L	L	H
L	X	H	H	H	L	L	H
X	L	X	L	no change			
L	X	L	X	no change			
L	X	X	L	no change			
X	L	L	X	no change			

H=HIGH state (the more positive voltage)
L=LOW state (the less positive voltage)
X=state is immaterial

G_1 and G_2 are "preset 0" inputs (reset all Q outputs to LOW)
G_3 and G_4 are "preset 9" inputs (set Q_A and Q_D to HIGH and reset Q_B and Q_C to LOW to provide BCD 9 count for nine complement applications)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	7.0	V
T input voltage	V_T	max.	5.5	V
G input voltage	V_G	max.	5.5	V
Peak negative input voltage (T, G)	$-V_I$	**max.**	2	V [1]
Storage temperature	T_{stg}	-65 to	+150	°C
Operating ambient temperature	T_{amb}	0 to	+70	°C

[1] Pulse duration t_p = 20 ns; repetition frequency f = 5 MHz; source resistance $R_S \geq 75\ \Omega$.

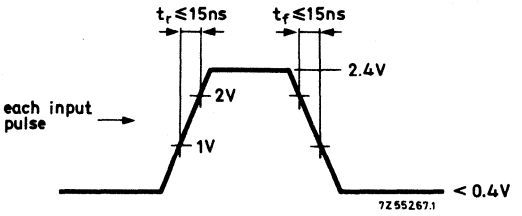
CHARACTERISTICS

		T_{amb} (°C)				Conditions and References	
		0	25	75		V_P (V)	
STATIC DATA							
Voltages							
Input threshold LOW (any input)	V_{ILmax}	0.8	0.8	0.8	V		
Input threshold HIGH all inputs except T_2	V_{IHmin}	2.0	2.0	2.0	V		
T_2 input	V_{T2Hmin}	2.2	2.2	2.2	V		
Output LOW	V_{QLmax}	0.4	0.4	0.4	V	4.75	$I_Q = I_{QLmax}$
Output HIGH	V_{QHmin}	2.4	2.4	2.4	V	4.75	$-I_Q = -I_{QHmax}$
Currents							
Input LOW (G input)	$-I_{GLmax}$	1.6	1.6	1.6	mA	5.25	$V_I = 0.4$ V
Input HIGH (G input)	I_{GHmax}	40	40	40	µA	5.25	$V_I = 2.4$ V 3)
Input LOW (T_1 input)	$-I_{T1Lmax}$	3.2	3.2	3.2	mA	5.25	$V_I = 0.4$ V
Input HIGH (T_1 input)	I_{T1Hmax}	80	80	80	µA	5.25	$V_I = 2.4$ V 3)
Input LOW (T_2 input)	$-I_{T2Lmax}$	6.4	6.4	6.4	mA	5.25	$V_I = 0.4$ V
Input HIGH (T_2 input)	I_{T2Hmax}	160	160	160	µA	5.25	$V_I = 2.4$ V 3)
Output LOW	I_{QLmax}	**16**	**16**	16	**mA**		
Output HIGH	$-I_{QHmax}$	**0.4**	**0.4**	**0.4**	**mA**		
Output short-circuited 1)	$-I_{Qscmin}$	**18**	**18**	**18**	**mA**	**5.25**	$V_Q = 0$
	$-I_{Qscmax}$	**57**	**57**	**57**	**mA**	**5.25**	$V_Q = 0$
SUPPLY DATA							
Supply current	I_P typ.	–	32	–	mA	5.0	$V_I = 4.5$ V
	<	53	53	53	mA	**5.25**	$V_I = 4.5$ V
DYNAMIC DATA							
Signal requirements							
Pulse duration (G inputs)	t_{GH} >	–	50	–	ns	5.0	
	t_{GL} >	–	50	–	ns	5.0	
Pulse duration (T inputs)	t_{TH} >	–	50	–	ns	5.0	
	t_{TL} >	–	50	–	ns	5.0	
Performance							
Rise propagation 2) delay time ($T_1 \rightarrow Q_C$)	t_{pdr} typ.	–	60	–	ns	5.0	
	<	–	100	–	ns	5.0	
Fall propagation 2) delay time ($T_1 \rightarrow Q_C$)	t_{pdf} typ.	–	60	–	ns	5.0	
	<	–	100	–	ns	5.0	
Maximum counting frequency	f >	–	10	–	MHz	5.0	
	typ.	–	18	–	MHz	5.0	

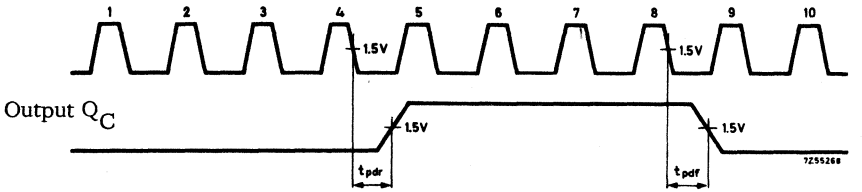
1) Do not short circuit more than one output at a time.
2) All four outputs loaded, Q_A output connected to T_2 input, delay from T_1 input to Q_C output. (see also waveforms page 6).
3) All input currents 1 mA at $V_I = 5.5$ V.

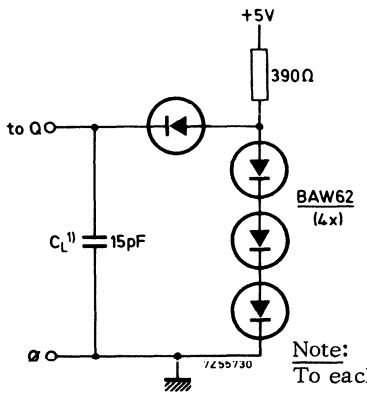
CHARACTERISTICS (continued)

Input pulse



Input T_1 (Q_A output connected to T_2)





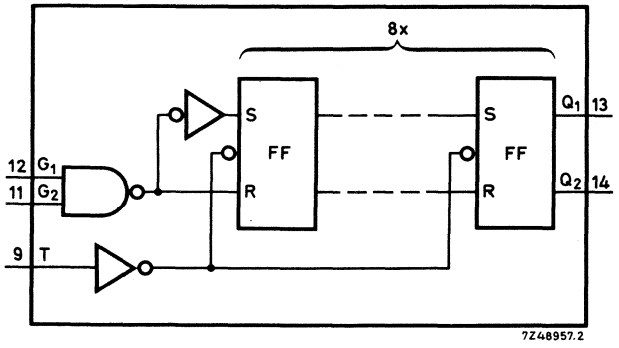
Note:
To each output the same loading circuit

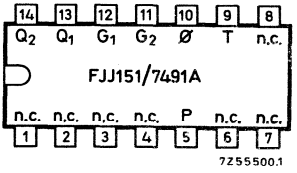
1) Including probe and jig capacitance

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices * it corresponds to the 74Nseries TTL.

8 BIT SHIFT REGISTER

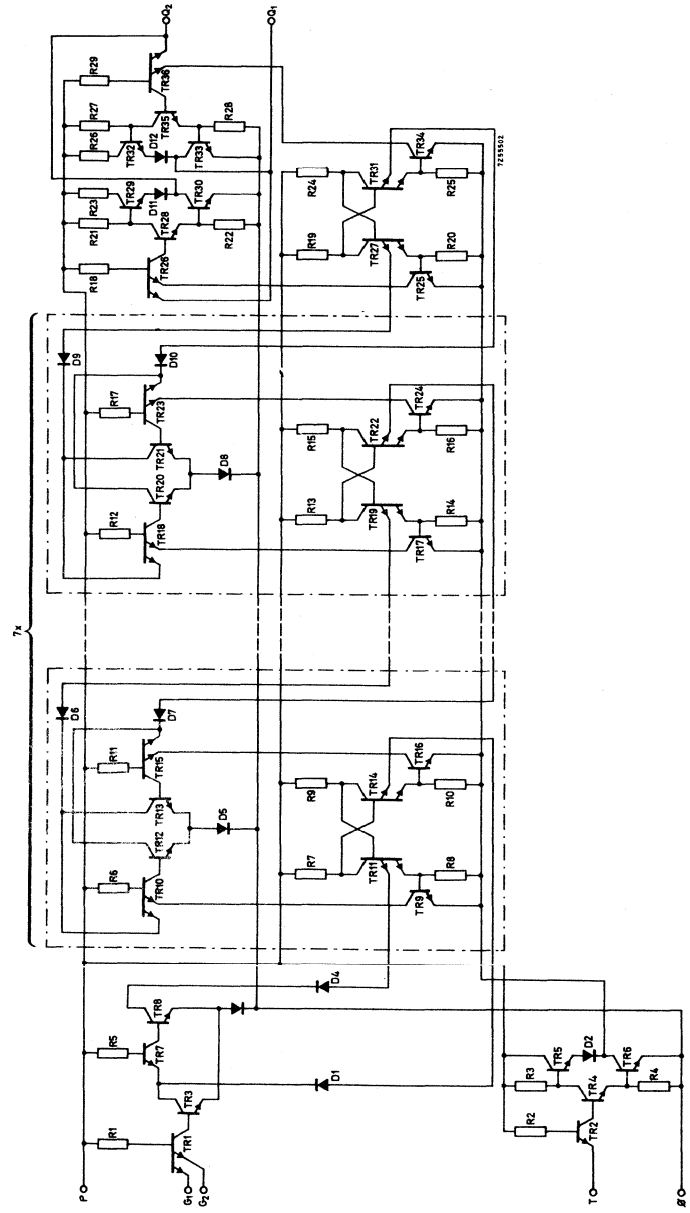




QUICK REFERENCE DATA			
Supply voltage	V_P	5.0 ±5%	V
Operating ambient temperature	T_{amb}	0 to +70	°C
Max. shift frequency	f	10	MHz
Available d.c. fan-out (full temperature range)	N_a	10	
D.C. noise margin (full temperature range)	M_L	> 0.4 typ. 1.0	V V
Total power dissipation	P_{tot}	typ. 175	mW

PACKAGE OUTLINE : 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAM



The FJJ151 is a serial input, serial-ouput 8-bit shift register with complementary outputs. It consists of eight RS master-slave flip-flops, a two-input NAND gate, and a clock driver. Inputs G_1 and G_2 go to an AND gate; either one or both inputs may be used. If only one is used, the other must be kept in the HIGH state.
When the T input is HIGH, information at the input of each stage is shifted to the next; thus, information at the G_1 or G_2 input is transferred to the Q_1 or Q_2 output after 8 clock pulses.
The FJJ151 corresponds to the SN7491AN.

LOGIC FUNCTION

Function table

t_n		t_{n+8}
G_1	G_2	Q_1
L	L	L
L	H	L
H	L	L
H	H	H

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
t_n = bit time before trigger pulse
t_{n+8} = bit time after 8 trigger pulses

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltages	V_P	max.	7.0	V
Input voltages	V_{G1}; V_{G2}; V_T	max.	5.5	V [1]
Peak negative input voltage (G_1, G_2, T)	$-V_M$	max.	2	V [2]
Storage temperature	T_{stg}	−65 to	+150	°C
Operating ambient temperature	T_{amb}	0 to	+70	°C

[1]) In addition the voltage between any two inputs must not exceed 5.5 V.
[2]) Pulse duration t_p = 20 ns; repetition frequency f = 5 MHz; source resistance $R_S \geq 75\ \Omega$.

CHARACTERISTICS

		T_{amb} (°C) 0	25	70	V_P (V)	Conditions and References
STATIC DATA						
Voltages						
Input threshold LOW (any input)	V_{ILmax}	0.8	0.8	0.8 V		
Input threshold HIGH (any input)	V_{IHmin}	2.0	2.0	2.0 V		
Output LOW	V_{QLmax}	0.4	0.4	0.4 V	4.75	$I_Q = I_{QLmax}$
Output HIGH	V_{QHmin}	2.4	2.4	2.4 V	4.75	$-I_Q = -I_{QHmax}$
Currents						
Input LOW; G_1	$-I_{G1Lmax}$	1.6	1.6	1.6 mA	5.25	$V_I = 0.4$ V
G_2	$-I_{G2Lmax}$	1.6	1.6	1.6 mA	5.25	
T	$-I_{TLmax}$	1.6	1.6	1.6 mA	5.25	
Input HIGH; G_1	I_{G1Hmax}	40	40	40 μA	5.25	$V_I = 2.4$ V
G_2	I_{G2Hmax}	40	40	40 μA	5.25	
T	I_{THmax}	40	40	40 μA	5.25	
G_1	I_{G1Hmax}	1.0	1.0	1.0 mA	5.25	$V_I = 5.5$ V
G_2	I_{G2Hmax}	1.0	1.0	1.0 mA	5.25	
T	I_{THmax}	1.0	1.0	1.0 mA	5.25	
Output LOW	I_{QLmax}	16	16	16 mA		$V_Q = V_{QLmax}$
Output HIGH	$-I_{QHmax}$	0.4	0.4	0.4 mA		$V_Q = V_{QHmin}$
Output short circuited (see note 1)	$-I_{Qscmin}$	18.0	18.0	18.0 mA	5.25	$V_Q = 0$
	$-I_{Qscmax}$	57.0	57.0	57.0 mA	5.25	
SUPPLY DATA						
Supply current; HIGH input G_1; G_2; T	I_{PH} typ.	-	35	- mA	5.0	
	I_{PH} <	60	60	60 mA	5.25	

Note 1: Not more than one output should be short circuited at a time.

CHARACTERISTICS

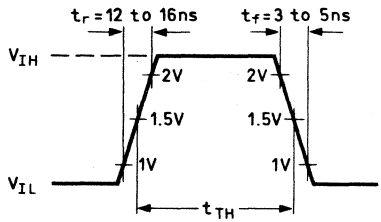
		T_{amb} (°C) 0	25	70		Conditions and References V_P (V)	
DYNAMIC DATA							
Performance							
Rise propagation delay time (T►Q)	t_{pdr} typ.	–	24	–	ns	5.0	
(see note 1)	t_{pdr} ≤	–	40	–	ns	5.0	
Fall propagation delay time (T►Q)	t_{pdf} typ.	–	27	–	ns	5.0	
(see note 1)	t_{pdf} ≤	–	40	–	ns	5.0	
Signal requirements							
Set-up time for G_1; G_2 inputs HIGH	t_{suH} ≥	–	25	–	ns	5.0	
LOW	t_{suL} ≥	–	25	–	ns	5.0	
Clock pulse width	t_{TH} >	–	25	–	ns	5.0	
G_1; G_2 input width	t_{GH} >	–	25	–	ns	5.0	
Hold time	t_{hold} ≥	–	0	–	ns	5.0	
Maximum operating shift frequency	f ≥	–	10	–	MHz	5.0	
	f typ	–	18	–	MHz	5.0	

Note 1: Refers to propagation delay from seventh bit to output stage.

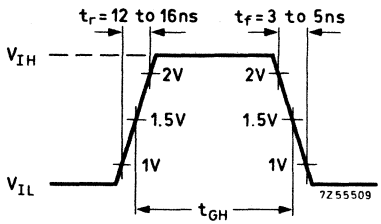
CHARACTERISTICS (continued)

DYNAMIC DATA

T INPUT



$G_1 \cdot G_2$ INPUT

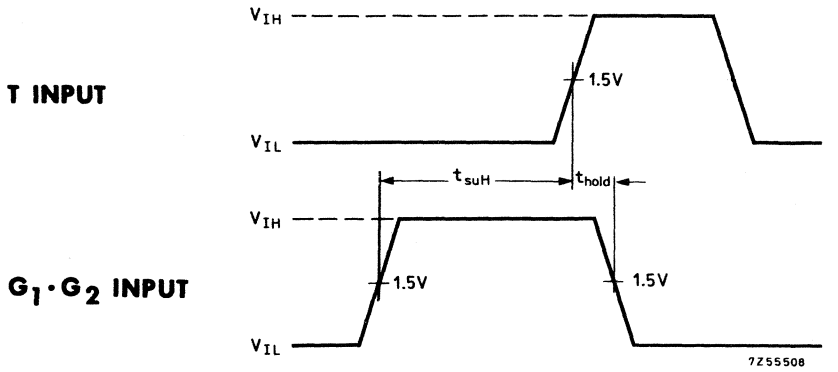


Waveforms illustrating input signals

CHARACTERISTICS (continued)

DYNAMIC DATA

In general case

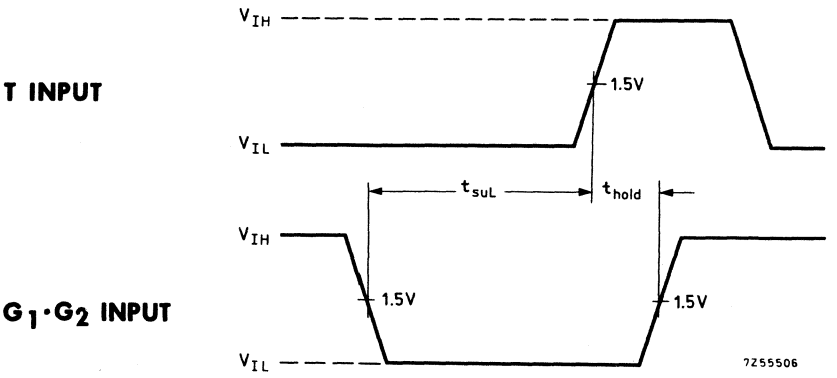


Waveforms illustrating measurement of set-up and hold times to **guarantee** shifting operation, for HIGH logic level.

CHARACTERISTICS (continued)

DYNAMIC DATA

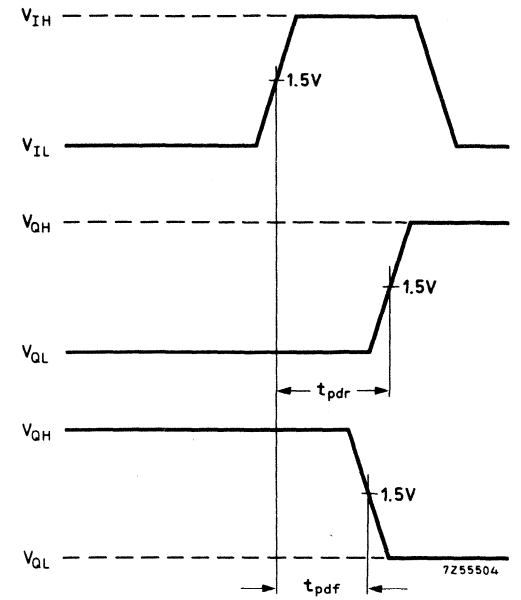
In general case



Waveforms illustrating measurement of set-up and hold times to guarantee shifting operation, for LOW logic level.

CHARACTERISTICS (continued)

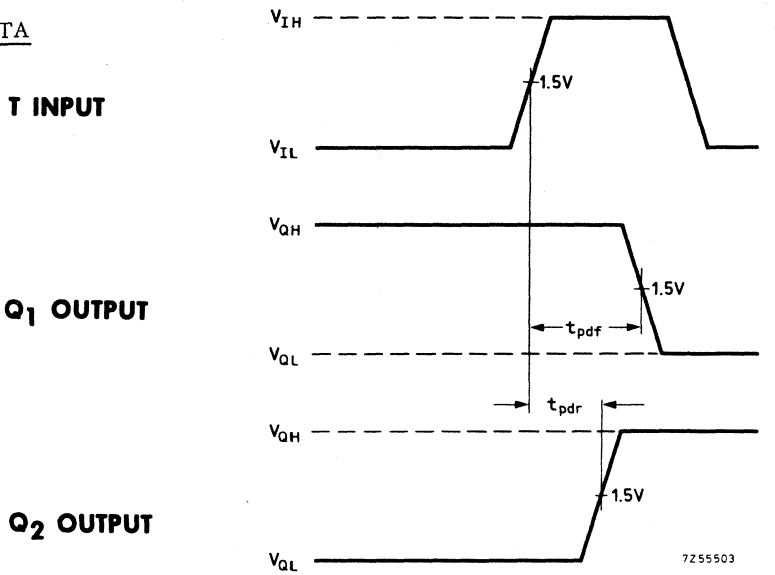
DYNAMIC DATA



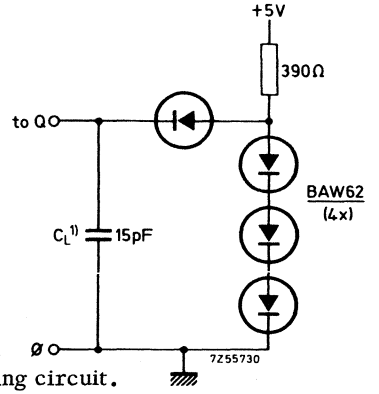
Waveforms illustrating measurement of t_{pdr} and t_{pdf} if S input of eight bit at logic HIGH level is 25 ns prior to rising edge of T input. (t_{hold} = 0 ns)

CHARACTERISTICS (continued)

DYNAMIC DATA



Waveforms illustrating measurement of t_{pdr} and t_{pdf} if S input of eight bit at logic LOW level is 25 ns prior to rising edge of T input (t_{hold} = 0 ns).

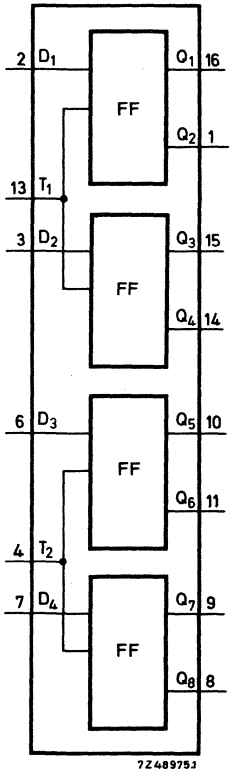


To output Q_2 the same loading circuit.

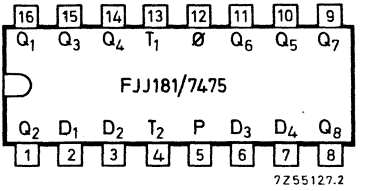
1) Including probe and jig capacitance

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.



QUADRUPLE LATCH D FLIP-FLOP

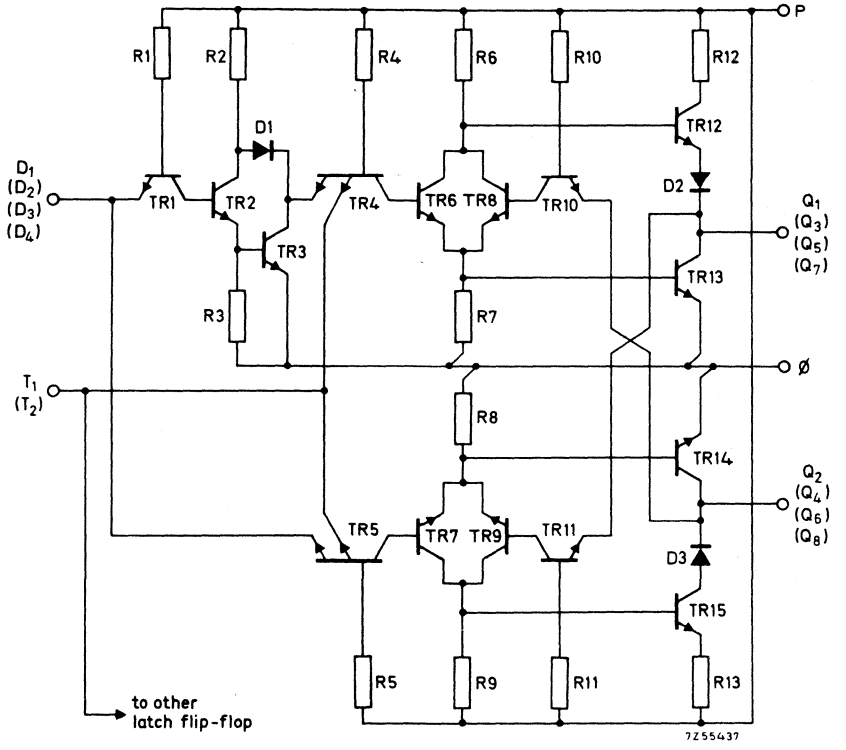


PACKAGE OUTLINE:

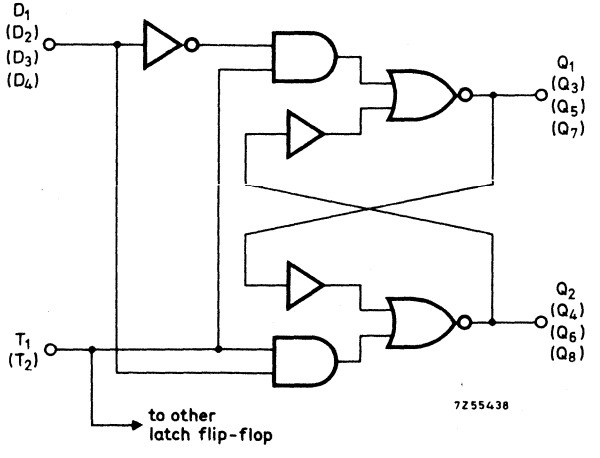
16 lead plastic dual in-line (type A) (See General Section)

QUICK REFERENCE DATA			
Supply voltage	V_P	5.0 ±5%	V
Operating ambient temperature range	T_{amb}	0 to +70	°C
Available d.c. fan-out (full temperature range)	N_a	≥ 10	
D.C. noise margin (full temperature range)	M_L	> 0.4 typ. 1.0	V V
Average power consumption (total) T_{amb} = 25 °C	P_{av}	typ. 160	mW

CIRCUIT DIAGRAM



LOGIC DIAGRAM



LOGIC FUNCTION

Information present at a data input is transferred to the Q output. For so long as the trigger input is HIGH, the Q output will follow the data input. When the trigger goes LOW, the information present at the data input at the time of transition is retained at the Q output until the trigger again goes HIGH.

Function table (each gate)

t_n data input	t_{n+1} output Q
L	L
H	H

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
t_n = bit time before trigger pulse
t_{n+1} = bit time after rising edge of trigger pulse

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	7.0	V
Input voltage	V_D, V_T	max.	5.5	V [1]
Peak negative input voltage (D, T)	$-V_M$	max.	2	V [2]
Storage temperature	T_{stg}	-65 to	+150	°C
Operating ambient temperature	T_{amb}	0 to	+70	°C

1) In addition the voltage between any two input must not exceed 5.5 V.
2) Pulse duration t_p = 20 ns; repetition frequency f = 5 MHz; source resistance $R_S \geq 75\ \Omega$.

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references	
		0	25	70		V_P (V)	
STATIC DATA							
Voltages							
Input threshold LOW (any input)	V_{ILmax}	0.8	0.8	0.8	V		
Input threshold HIGH (any input)	V_{IHmin}	2.0	2.0	2.0	V		
Output LOW	V_{QLmax}	0.4	0.4	0.4	V	4.75	$I_Q = I_{QLmax}$
Output HIGH	V_{QHmin}	2.4	2.4	2.4	V	4.75	$-I_Q = -I_{QHmax}$
Currents							
Input LOW (D)	$-I_{DLmax}$	3.2	3.2	3.2	mA	5.25	$V_D = V_{QLmax}$; $I_Q = 0$
Input HIGH (D) 1)	I_{DHmax}	80	80	80	µA	5.25	$V_D = V_{QHmin}$; $I_Q = 0$
Input LOW (T)	$-I_{TLmax}$	6.4	6.4	6.4	mA	5.25	$V_T = V_{QLmax}$; $I_Q = 0$
Input HIGH (T) 2)	I_{THmax}	160	160	160	µA	5.25	$V_T = V_{QHmin}$; $I_Q = 0$
Output LOW	**I_{QLmax}**	**16**	**16**	**16**	**mA**		
Output HIGH	**$-I_{QHmax}$**	**0.4**	**0.4**	**0.4**	**mA**		
Output short circuited 3)	$-I_{Qscmin}$	18	18	18	mA	5.25	$V_Q = 0$
	$-I_{Qscmax}$	57	57	57	mA		
SUPPLY DATA							
Supply current (total)	I_P typ.	–	–	–	mA	5.0	$V_T = V_D = 0$ V
	I_P <	53	53	53	mA	5.25	

1) I_{DHmax} = 1 mA at V_P = 5.25 V and V_D = 5.5 V.

2) I_{THmax} = 1 mA at V_P = 5.25 V and V_T = 5.5 V.

3) Not more than one output should be short circuited at a time.

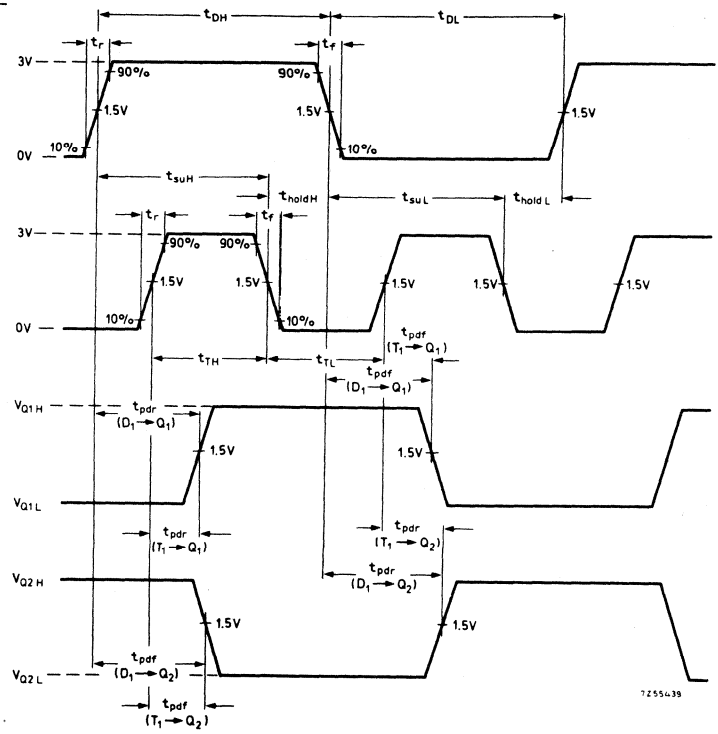
CHARACTERISTICS

		T_{amb} (°C)	Conditions and References	
		0 25 70	V_p (V)	All these times at N = 10
DYNAMIC DATA				C_L = 15 pF; R_L = 400 Ω
Performance				
Minimum set-up time				
D inputs:				
HIGH	t_{suH} typ.	- 7 - ns	5	
	t_{suH} <	- 20 - ns	5	
LOW	t_{suL} typ.	- 14 - ns	5	
	t_{suL} <	- 20 - ns	5	
Maximum hold time 1)				
D inputs:				
HIGH	$t_{hold\ H}$ typ.	- 15 - ns	5	
LOW	$t_{hold\ L}$ typ.	- 6 - ns	5	
Propagation delay times:				
Rise D→Q_1(Q_3; Q_5; Q_7)	t_{pdr} <	- 30 - ns	5	
Fall D→Q_1(Q_3; Q_5; Q_7)	t_{pdf} <	- 25 - ns	5	
Rise D→Q_2(Q_4; Q_6; Q_8)	t_{pdr} <	- 40 - ns	5	
Fall D→Q_2(Q_4; Q_6; Q_8)	t_{pdf} <	- 15 - ns	5	
Rise T_1→Q_1(Q_3) T_2→Q_5(Q_7)	t_{pdr} <	- 30 - ns	5	
Fall T_1→Q_1(Q_3) T_2→Q_5(Q_7)	t_{pdf} <	- 15 - ns	5	
Rise T_1→Q_2(Q_4) T_2→Q_6(Q_8)	t_{pdr} <	- 30 - ns	5	
Fall T_1→Q_2(Q_4) T_2→Q_6(Q_8)	t_{pdf} <	- 15 - ns	5	

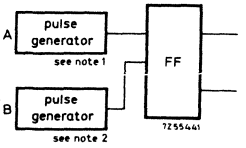
1) These times indicate that period prior to the fall of the clock pulse below 1.5 V when the input data will still be recognized and stored.

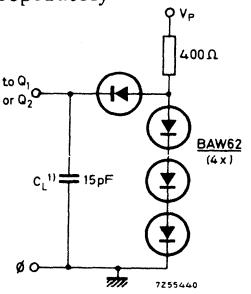
CHARACTERISTICS (continued)

DYNAMIC DATA



Waveforms inllustrating measurement of t_{pdr} and t_{pdf}.
Each latch D flip-flop is tested seperately





1) C_L includes probe and jig capacitance

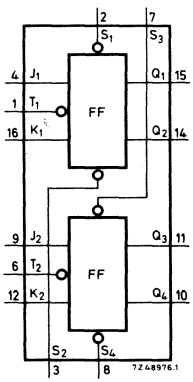
Notes:

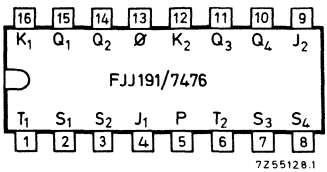
1. Pulse generator A: V_A = 3V; $t_r \leq 10$ ns; $t_f \leq 10$ ns; R_S = 50 Ω; $t_{DH} = t_{DL}$ = 1 μs; f = 500 kHz
2. Pulse generator B; V_B = 3 V; $t_r \leq 10$ ns; $t_f \leq 10$ ns; R_S = 50 Ω; $t_{TH} = t_{TL}$ = 500 ns; f = 1 MHz

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

DUAL JK MASTER-SLAVE FLIP-FLOP



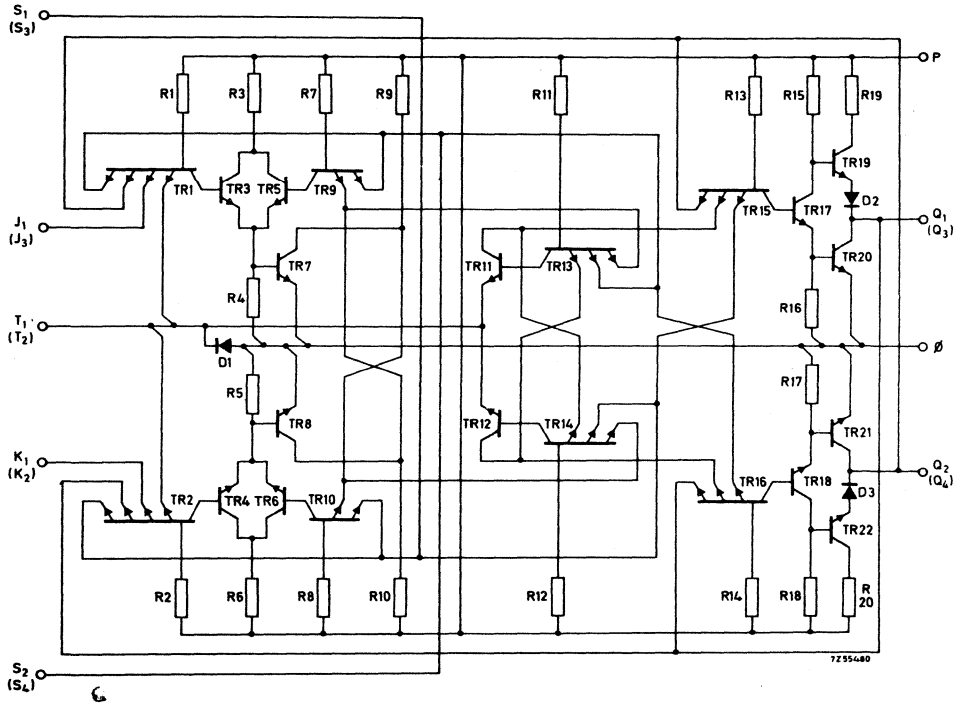


QUICK REFERENCE DATA			
Supply voltage	V_P	5.0 ± 5%	V
Operating ambient temperature range	T_{amb}	0 to +70	°C
Maximum operating frequency	f	15	MHz
Available d.c. fan-out (full temperature range)	N_a	≥ 10	
D.C. noise margin (full temperature range)	M_L	> 0.4 typ. 1.0	V V
Average power consumption (total) T_{amb} = 25 °C	P_{av}	typ. 80	mW

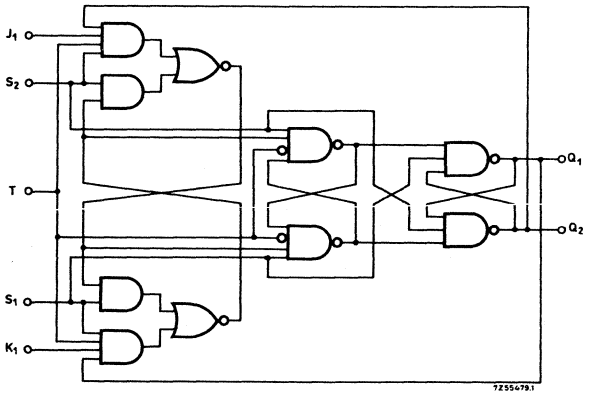
The FJJ191/7476 is a dual JK master-slave flip-flop having one J and one K input per flip-flop. The circuits operate at a frequency up to 15 MHz The information at the J and K inputs enters the master when T is HIGH. Afterwards, when T is LOW, the information is transferred from the master to the slave and appears at the outputs. The SET signals on S_1 and S_2 (S_3 and S_4) which override any other inputs, are active at the LOW level.

PACKAGE OUTLINE: 16 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAM



LOGIC DIAGRAM



LOGIC FUNCTION

LOW input to $S_1(S_3)$ sets $Q_1(Q_3)$ to HIGH
LOW input to $S_2(S_4)$ sets $Q_1(Q_3)$ to LOW
} independent of trigger pulse

Function table for J and K inputs

t_n		t_{n+1}
J	K	Q_1
L	L	Q_{1n}
L	H	L
H	L	H
H	H	$\overline{Q_{1n}}$

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
t_n = bit time before trigger pulse
t_{n+1} = bit time after trigger pulse

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	7.0	V
Input voltage	V_J, V_K, V_T, V_S	max.	5.5	V [1]
Peak negative input voltage (J, K, T, S)	$-V_M$	max.	2	V [2]
Storage temperature	T_{stg}	-65 to	+125	°C
Operating ambient temperature	T_{amb}	0 to	+70	°C

[1]) In addition the voltage between any two inputs must not exceed 5.5 V.
[2]) Pulse duration t_p = 20 ns; repetition frequency f = 5 MHz; source resistance $R_S \geq 75\,\Omega$.

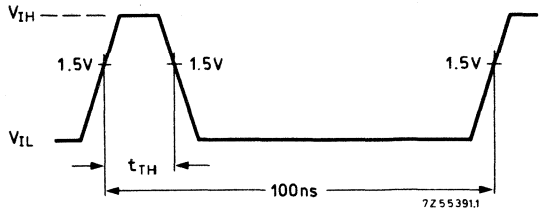
CHARACTERISTICS

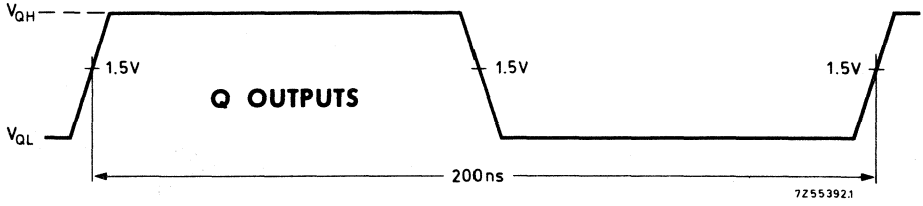
		T_{amb} (°C)			Conditions and references	
		0	25	75	V_P (V)	
STATIC DATA						
Voltages						
Input threshold LOW (any input)	V_{ILmax}	0.8	0.8	0.8 V		
Input threshold HIGH (any input)	V_{IHmin}	2.0	2.0	2.0 V		
Output LOW	V_{QLmax}	0.4	0.4	0.4 V	4.75	$I_Q = I_{QLmax}$
Output HIGH	V_{QHmin}	2.4	2.4	2.4 V	4.75	$-I_Q = -I_{QHmax}$
Currents						
Input LOW (J, K)	$-I_{ILmax}$	1.6	1.6	1.6 mA	5.25	$V_I = V_{QLmax}$; $I_Q = 0$
Input HIGH (J, K)	I_{IHmax}	40	40	40 μA	5.25	$V_I = V_{QHmin}$; $I_Q = 0$
Input LOW (S, T)	$-I_{SLmax}$	3.2	3.2	3.2 mA	5.25	$V_{S,T} = V_{QLmax}$; $I_Q = 0$
	$-I_{TLmax}$	3.2	3.2	3.2 mA		
Input HIGH (S, T)	I_{SHmax}	80	80	80 μA	5.25	$V_{S,T} = V_{QHmin}$; $I_Q = 0$
	I_{THmax}	80	80	80 μA		
Output LOW	I_{QL}	16	16	16 mA		
Output short circuited	$-I_{Qscmin}$	18	18	18 mA	5.25	$V_I = 0$; $V_Q = 0$
	$-I_{Qscmax}$	57	57	57 mA	5.25	
SUPPLY DATA						
Supply current (total)	I_P typ.	-	20	- mA	5.0	
	<	40	40	40 mA	5.25	
DYNAMIC DATA						
Signal requirements						
Pulse duration (T input)	t_{TH} >	-	20	- ns	5.0	
Pulse duration (S input)	t_{SL} >	-	25	- ns	5.0	
Performance						
Rise propagation delay time (S→Q)	t_{pdr} typ.	-	16	- ns	5.0	N = 10; C_L = 15 pF
	t_{pdr} <	-	25	- ns	5.0	
Fall propagation delay time (S→Q)	t_{pdr} typ.	-	25	- ns	5.0	N = 10; C_L = 15 pF
	t_{pdf} <	-	40	- ns	5.0	
Rise propagation delay time (T→Q)	t_{pdr} >	-	10	- ns	5.0	
	t_{pdr} typ.	-	16	- ns	5.0	N = 10; C_L = 15 pF
	t_{pdr} <	-	25	- ns	5.0	
Fall propagation delay time (T Q)	t_{pdf} >	-	10	- ns	5.0	
	t_{pdf} typ.	-	25	- ns	5.0	N = 10; C_L = 15 pF
	t_{pdf} <	-	40	- ns	5.0	
Maximum operating frequency	f >	-	15	- MHz	5.0	N = 10; C_L = 15 pF
	f typ.	-	20	- MHz		

CHARACTERISTICS (continued)

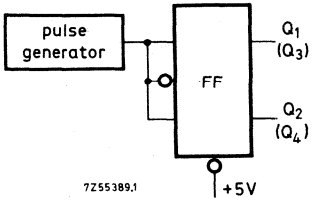
DYNAMIC DATA

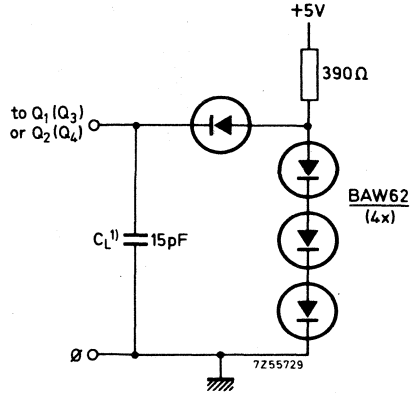
T, J and K INPUTS





Waveforms illustrating in- and output pulses



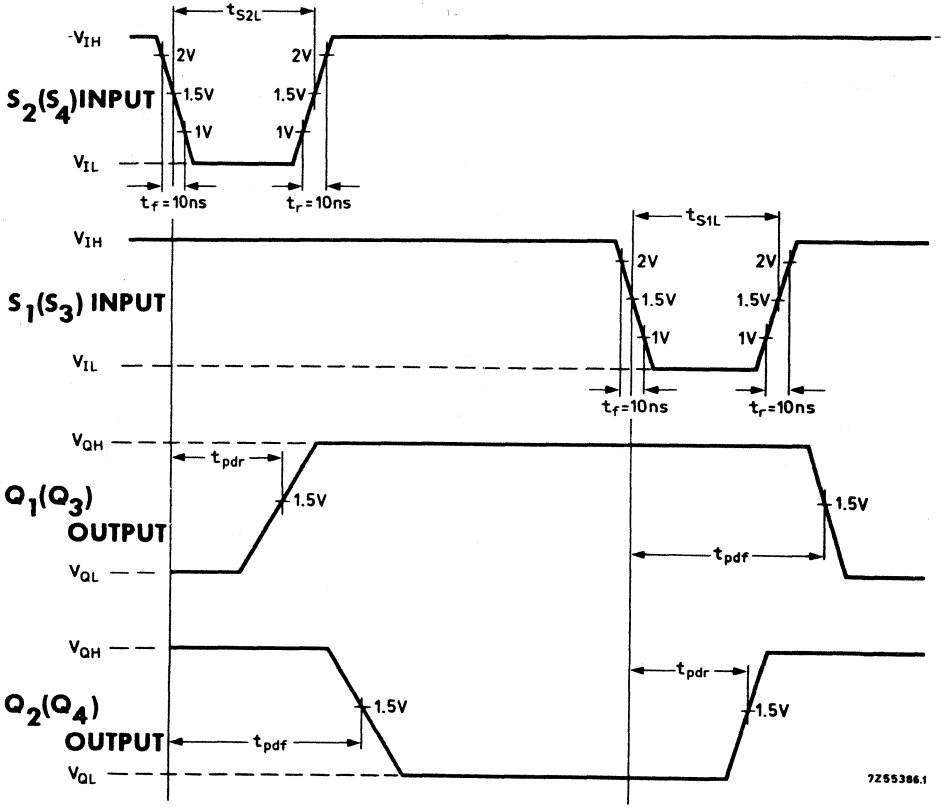


[1]) Including probe and jig capacitance

Equivalent load for N = 10

CHARACTERISTICS (continued)

DYNAMIC DATA

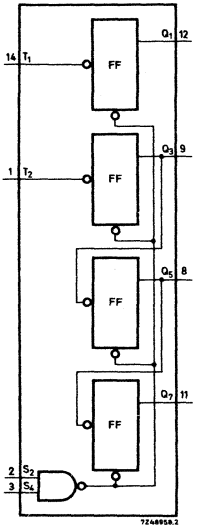


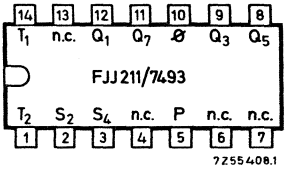
Waveforms illustrating switching times

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

SINGLE ASYNCHRONOUS 4-BIT BINARY COUNTER

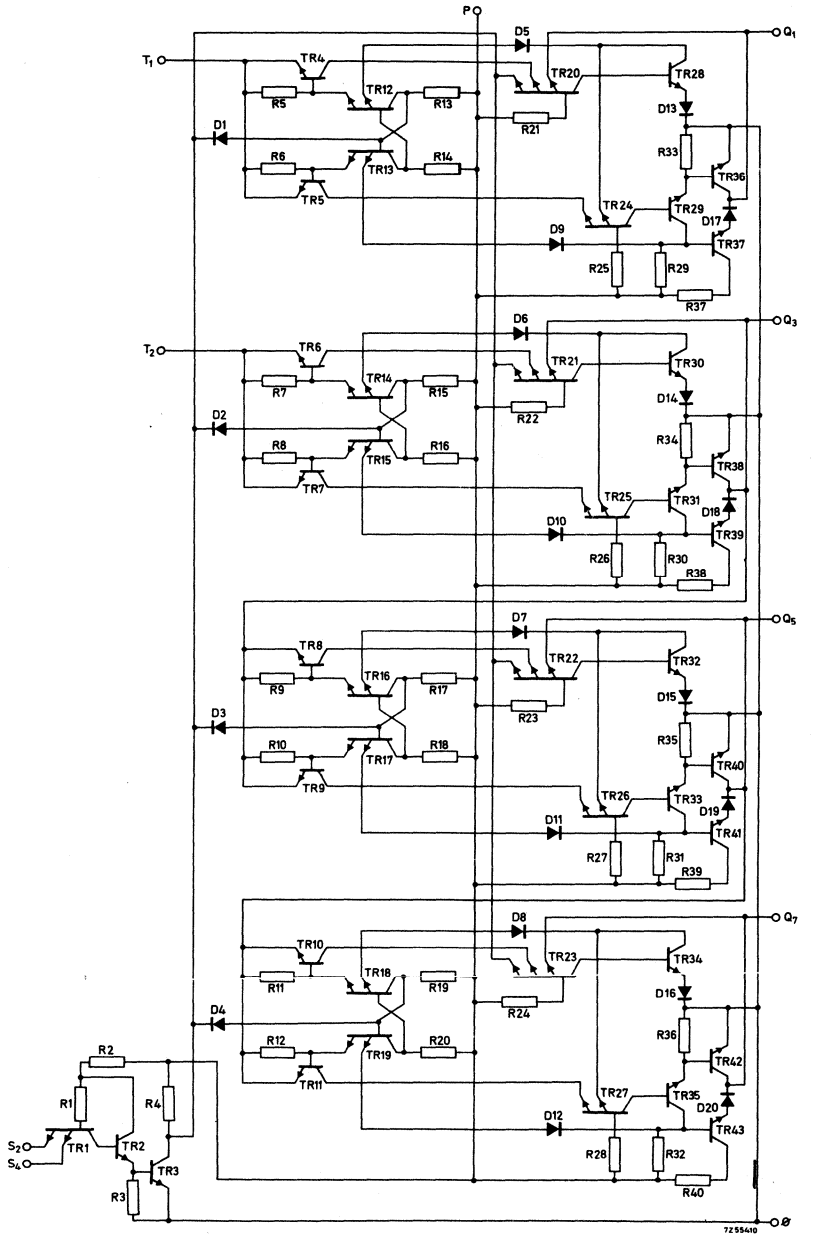




QUICK REFERENCE DATA			
Supply voltage	V_P	5.0 ± 5%	V
Operating ambient temperature	T_{amb}	0 to +70	°C
Maximum operating frequency	f	≥ 10	MHz
Available d.c. fan-out (full temperature range)	N_a	≥ 10	
D.C. noise margin (full temperature range)	M_L	> 0.4 typ. 1.0	V V
Average power consumption (total) T_{amb} = 25 °C	P_{av}	typ. 128	mW

PACKAGE OUTLINE: 14 lead plastic dual in-line (type A) (See General Section)

CIRCUIT DIAGRAM



The FJJ211/7493 is a high-speed asynchronous 4-bit binary counter with four master-slave flip-flops which are internally connected to provide a divide-by-two and a divide-by-eight counter. By using an external connection a count of sixteen can be obtained. A gated line, direct reset inhibits the count and simultaneously all flip-flop outputs return to the LOW state.

For use as a 4-bit ripple-through counter, externally connect Q_1 to T_2; apply the count pulses to T_1. As shown by the function table below, the outputs at Q_1, Q_3, Q_5 and Q_7 represent division by 2, 4, 8 and 16 respectively.

For use as 3-bit ripple-through counter, apply the count pulses to T_2.

Simultaneous divisions by 2, 4 and 8 are available at the outputs Q_3, Q_5 and Q_7. The first flip-flop (T_1 and Q_1) can be used independently if the reset function (S_2 and S_4) coincides with reset of the 3-bit ripple-through counter.

FUNCTION TABLES

count	outputs			
	Q_1	Q_3	Q_5	Q_7
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

Notes:
1. Q_1 connected to T_2
2. To reset all outputs in the LOW state, S_2 and S_4 inputs must be HIGH.
3. Either S_2 or S_4 (or both) must be LOW to count.

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	7.0	V
Input voltage	V_T;V_S	max.	5.5	V [1]
Peak negative input voltage (T, S)	$-V_M$	max.	2	V [2]
Storage temperature	T_{stg}		-65 to +150	°C
Operating ambient temperature	T_{amb}		0 to +70	°C

1) In addtion the input voltage between any two T inputs or between any two S inputs: max. 5.5 V.
2) Pulse duration t_p = 20 ns; repetition frequency f = 5 MHz; source resistance $R_S \geq 75\,\Omega$.

CHARACTERISTICS

		T_{amb} (°C) 0	25	70	Conditions and References: V_P (V)	
STATIC DATA						
Voltages						
Input threshold LOW						
S_2; S_4; T_1	V_{S2Lmax} V_{S4Lmax} V_{T1Lmax}	0.8	0.8	0.8 V	4.75	
T_2	V_{T2Lmax}	0.6	0.6	0.6 V	4.75	
Input threshold HIGH						
S_2; S_4; T_1	V_{S2Hmin} V_{S4Hmin} V_{T1Hmin}	2.0	2.0	2.0 V	4.75	
T_2	V_{T2Hmin}	2.2	2.2	2.2 V	4.75	
Output LOW						
Q_1; Q_3; Q_5; Q_7	V_{Q1Lmax} V_{Q3Lmax} V_{Q5Lmax} V_{Q7Lmax}	0.4	0.4	0.4 V	4.75	Q_1 connected to T_2; $I_Q = I_{QLmax}$
Output HIGH						
Q_1; Q_3; Q_5; Q_7	V_{Q1Hmin} V_{Q3Hmin} V_{Q5Hmin} V_{Q7Hmin}	2.4	2.4	2.4 V	4.75	Q_1 connected to T_2; $I_Q = -I_{QHmax}$
Currents						
Input LOW: S_2 S_4	$-I_{S2Lmax}$ $-I_{S4Lmax}$	1.6	1.6	1.6mA	5.25	$V_S = V_{QLmax}$
T_1 T_2	$-I_{T1Lmax}$ $-I_{T2Lmax}$	3.2	3.2	3.2 mA	5.25	$V_T = V_{QLmax}$
Input HIGH: S_2 S_4	I_{S2Hmax} I_{S4Hmax}	40	40	40 μA	5.25	$V_S = V_{QHmin}$ 1)
T_1	I_{T1Hmax}	80	80	80 μA	5.25	$V_T = V_{QHmin}$ 2)
T_2	I_{T2Hmax}	160	160	160 μA	5.25	$V_T = V_{QHmin}$ 2)
Output LOW						
Q_1; Q_3; Q_5; Q_7	I_{Q1Lmax} I_{Q3Lmax} I_{Q5Lmax} I_{Q7Lmax}	16	16	16 mA	4.75	

1) Input current 1 mA at V_S = 5.5 V.
2) Input current 1 mA at V_T = 5.5 V.

CHARACTERISTICS (continued)

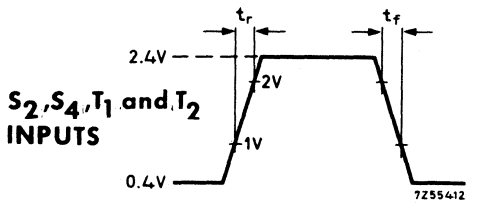
		T_{amb} (°C)				Conditions and References	
		0	25	70		V_P (V)	
STATIC DATA (continued)							
Output HIGH							
Q_1; Q_3; Q_5; Q_7	$-I_{Q1H}$ max $-I_{Q3H}$ max $-I_{Q5H}$ max $-I_{Q7H}$ max	400	400	400	µA	4.75	
Output short circuited							
Q_1; Q_3; Q_5; Q_7 (See note 2)	$-I_{Q1scmin}$ $-I_{Q3scmin}$ $-I_{Q5scmin}$ $-I_{Q7scmin}$	18	18	18	mA	5.25	$V_Q = 0$; $V_S = V_T = 0$
	$-I_{Q1scmax}$ $-I_{Q3scmax}$ $-I_{Q5scmax}$ $-I_{Q7scmax}$	57	57	57	mA	5.25	$V_Q = 0$; $V_S = V_T = 0$
SUPPLY DATA							
Supply current	I_P typ.	–	32	–	mA	5.0	All inputs and outputs open
	<	53	53	53	mA	5.25	
DYNAMIC DATA							
Rise propagation	t_{pdr} typ.	–	75	–	ns	5.0	C_L = 15 pF; R_L = 390 Ω
delay time (note 1)	t_{pdr} <	–	135	–	ns	5.0	
Fall propagation	t_{pdf} typ.	–	75	–	ns	5.0	C_L = 15 pF; R_L = 390 Ω
delay time (note 1)	t_{pdf} <	–	135	–	ns	5.0	
Rise time	t_r <	–	10	–	ns	5.0	f = 1 MHz; duty cycle: 0.5
Fall time	t_f <	–	10	–	ns	5.0	
Trigger time HIGH	t_{T1H}; t_{T2H} <	–	50	–	ns	5.0	
Trigger time LOW	t_{T1L}; t_{T2L} <	–	50	–	ns	5.0	
Width of pulse							
S_2 and S_4	t_{S2L}; t_{S4L} >	–	50	–	ns	5.0	
T_1	t_{T1} >	–	50	–	ns	5.0	

Note 1:
All four outputs loaded. Output Q_1 connected to input T_2. ($T_1 \rightarrow Q_7$)

Note 2:
Not more than one output should be short circuited at a time.

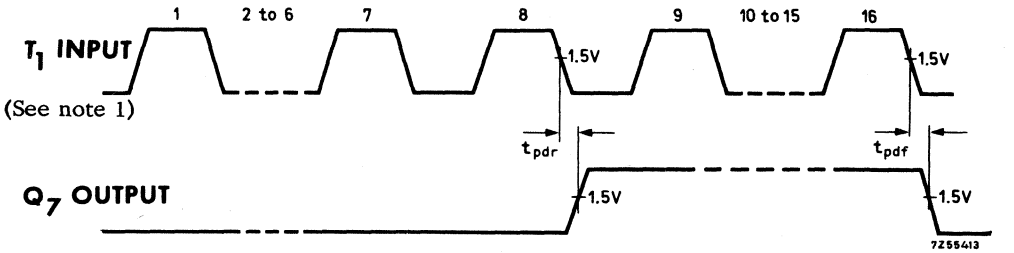
CHARACTERISTICS (continued)

DYNAMIC DATA



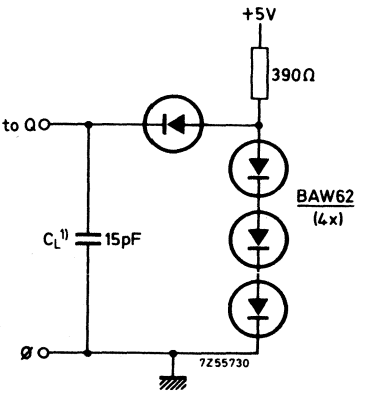
Pulse generator:

t_r < 10 ns
t_f < 10 ns
f = 1 MHz
duty cycle δ = 0.5



Waveforms inllustrating measurement of t_{pdr} and t_{pdf}

Note 1:
T_1 input (Q_1 output connected to T_2 input)



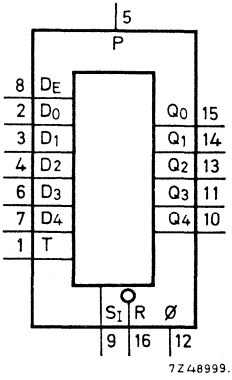
To outputs Q_3, Q_5 and Q_7 the same loading circuit.

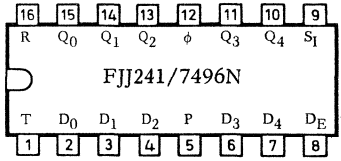
1) Including probe and jig capacitance.

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

5-BIT SHIFT REGISTER

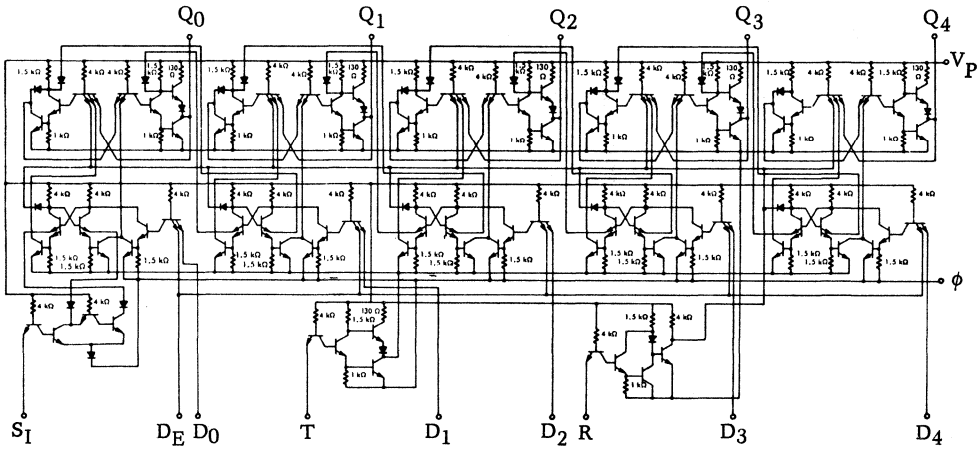




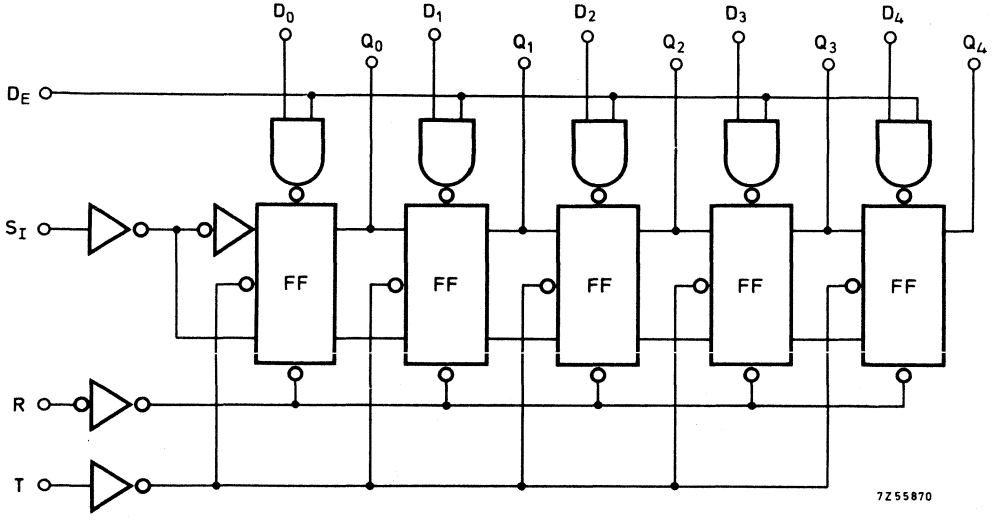
QUICK REFERENCE DATA				
Supply voltage	V_P		5.0 ± 5 %	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Maximum shift frequency	f		10	MHz
Available d.c. fan-out (full temperature range)	N_a	≥	10	
D.C. noise margin (full temperature range)	M_L	>	0.4	V
		typ.	1.0	V
Average power consumption	P_{av}	typ.	240	mW

PACKAGE OUTLINE : 16 lead plastic dual in-line (type A) (See General Section).

CIRCUIT DIAGRAM



LOGIC DIAGRAM



GENERAL DESCRIPTION

The FJJ241/7496N consists of five RS master-slave flip-flops connected as a shift register to perform parallel-to-serial or serial-to-parallel conversion of binary data. Since both inputs and outputs to all flip-flops are accessible, parallel-in / parallel--out or serial-in / serial-out operation may be performed.
All flip-flops are simultaneously set to the LOW state by applying a LOW level voltage to the CLEAR input. This condition may be applied independently of the state of the CLOCK input.
The flip-flops may be independently set to the HIGH state by applying a HIGH level voltage to both the PRESET input of the specific flip-flop and the common PRESET input. The common PRESET input is provided to allow the flexibility of either setting each flip-flop independently or setting two or more flip-flops simultaneously. PRESET is independent of the state of the CLOCK input. Transfer of information to the output pins occurs when the CLOCK input goes from LOW to HIGH. Since the flip-flops are RS master-slave circuits, the proper information must appear at the RS-inputs of each flip-flop prior to the rising edge of the CLOCK input voltage waveform. The serial input provides this information to the first flip-flop, while the outputs of the subsequent flip-flops provide information for the remaining RS-inputs. The CLEAR input must be HIGH and the PRESET input must be LOW when clocking occurs.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	7.0	V
Input voltages	V_I	max.	5.5	V [1]
Peak negative input voltage	$-V_{IM}$	max.	2	V [2]
Storage temperature	T_{stg}		−65 to +150	°C
Operating ambient temperature	T_{amb}		0 to +70	°C

[1] In addition, the voltage between any two inputs must not exceed 5.5 V.
[2] Pulse duration t_p = 20 ns; repetition frequency f = 5 MHz; source resistance $R_S \geq 75\,\Omega$.

CHARACTERISTICS

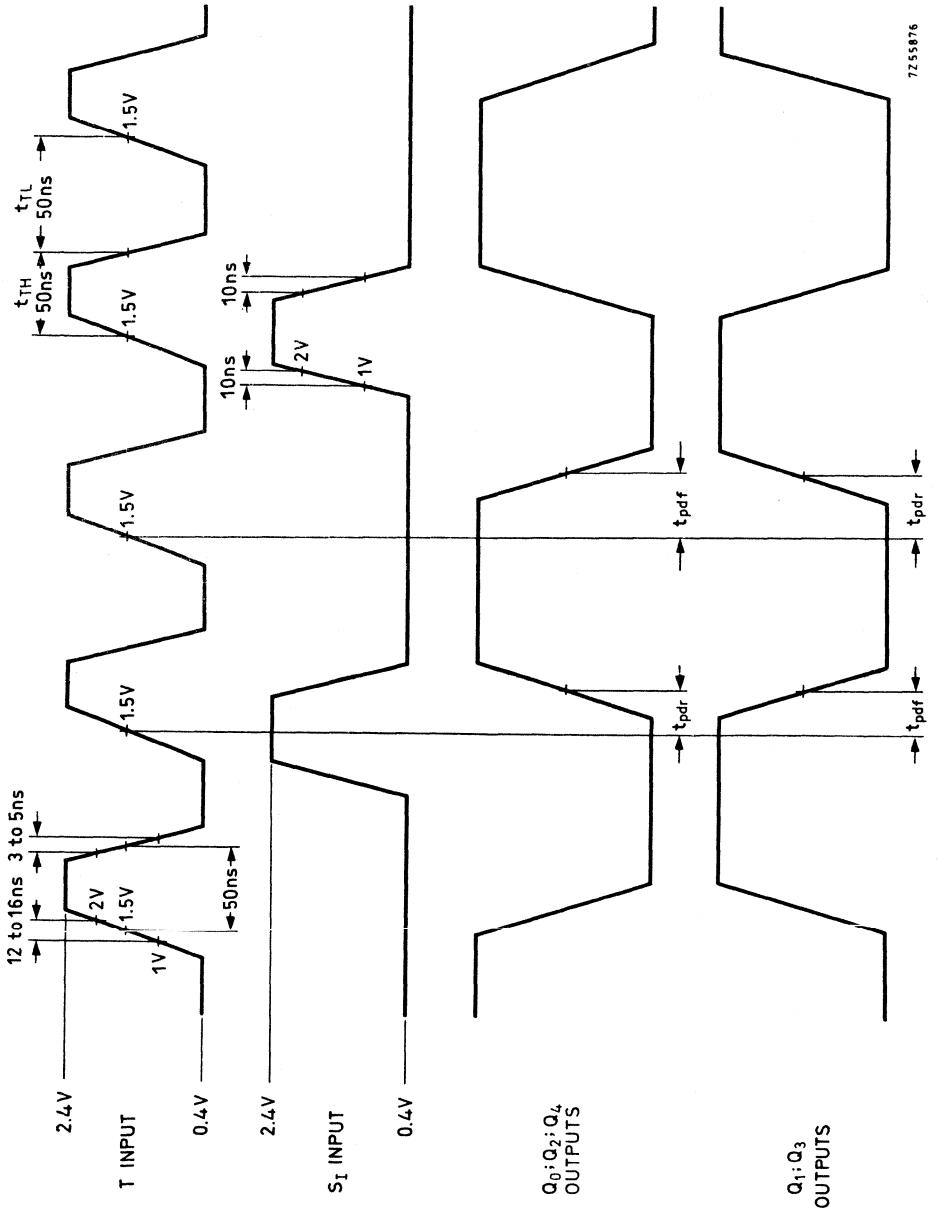
		T_{amb} (°C)			Conditions and References	
		0	25	70	V_P (V)	
STATIC DATA						
Voltages						
Input threshold LOW (any input)	V_{ILmax}	0.8	0.8	0.8 V		
Input threshold HIGH (any input)	V_{IHmin}	2.0	2.0	2.0 V		
Output LOW	V_{QLmax}	0.4	0.4	0.4 V	4.75	$I_Q = I_{QLmax}$
Output HIGH	V_{QHmin}	2.4	2.4	2.4 V	4.75	$-I_Q = -I_{QHmax}$
Currents						
Input LOW						
All inputs except D_E	$-I_{ILmax}$	1.6	1.6	1.6 mA	5.25	$V_G = V_{QLmax}$
input D_E	$-I_{ILmax}$	8.0	8.0	8.0 mA	5.25	$V_G = V_{QLmax}$
Input HIGH						
All inputs except D_E	I_{IHmax}	40	40	40 µA	5.25	$V_G = V_{QHmin}$
input D_E	I_{IHmax}	200	200	200 µA	5.25	$V_G = V_{QHmin}$
All inputs except D_E	I_{IHmax}	1.0	1.0	1.0 mA	5.25	$V_G = 5.5$ V
Output LOW	I_{QLmax}	16	16	16 mA		$V_Q = V_{QLmax}$
Output HIGH	$-I_{QHmax}$	0.4	0.4	0.4 mA		$V_Q = V_{QHmin}$
Output short circuited (see note 1)	$-I_{Q\,sc\,min}$	18.0	18.0	18.0 mA	5.25	$V_Q = 0$
	$-I_{Q\,sc\,max}$	57.0	57.0	57.0 mA	5.25	$V_Q = 0$
SUPPLY DATA						
Supply current; HIGH input	I_{PH} typ.	–	48	– mA	5.0	
	I_{PH} <	79	79	79 mA	5.25	

Note 1: Not more than one output should be short circuited at a time.

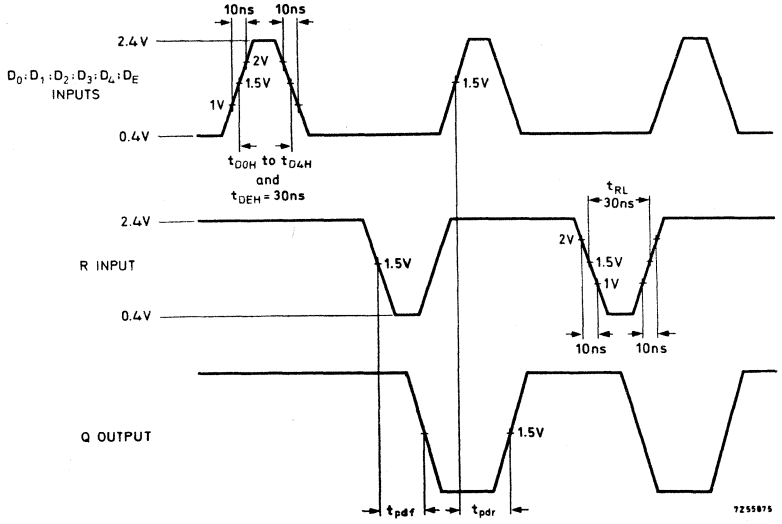
CHARACTERISTICS (continued)

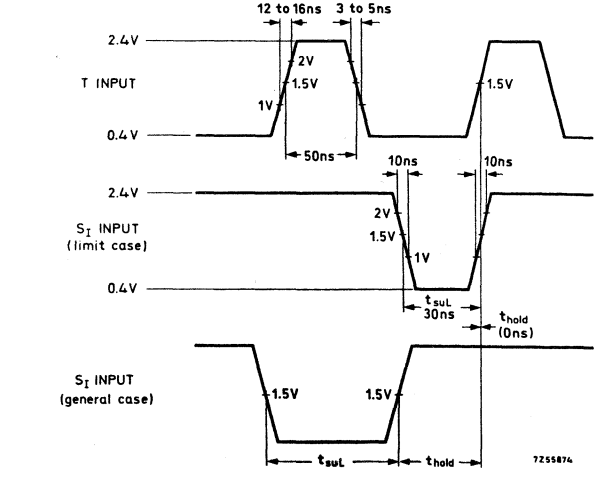
		T_{amb} (°C)			Conditions and References	
		0	25	70	V_P (V)	
DYNAMIC DATA						All conditions N = 10 C_L = 15 pF
Performance						
Rise Propagation delay time (T → Q)	t_{pdr} typ.		– 25 –	ns	5.0	
	t_{pdr} ≤		– 40 –	ns	5.0	
Fall propagation delay time (T → Q)	t_{pdf} typ.		– 25 –	ns	5.0	
	t_{pdf} ≤		– 40 –	ns	5.0	
Rise Propagation delay time (D_E → Q)	t_{pdr} ≤		– 35 –	ns	5.0	
Fall Propagation delay time (R → Q)	t_{pdf} ≤		– 55 –	ns	5.0	
Signal requirements						
Set up time for S_I (LOW and HIGH)	t_{su} ≥		– 30 –	ns	5.0	
Hold time for S_I (LOW and HIGH)	t_{hold} ≥		– 0 –	ns	5.0	
Clock pulse width (HIGH)	t_{TH} >		– 35 –	ns	5.0	
Clear pulse width (LOW)	t_{RL} >		– 30 –	ns	5.0	
Preset pulse width (all inputs; HIGH)	t_{IH} >		– 30 –	ns	5.0	
Maximum operating shift frequency	f ≥		– 10 –	MHz	5.0	

CHARACTERISTICS (continued)

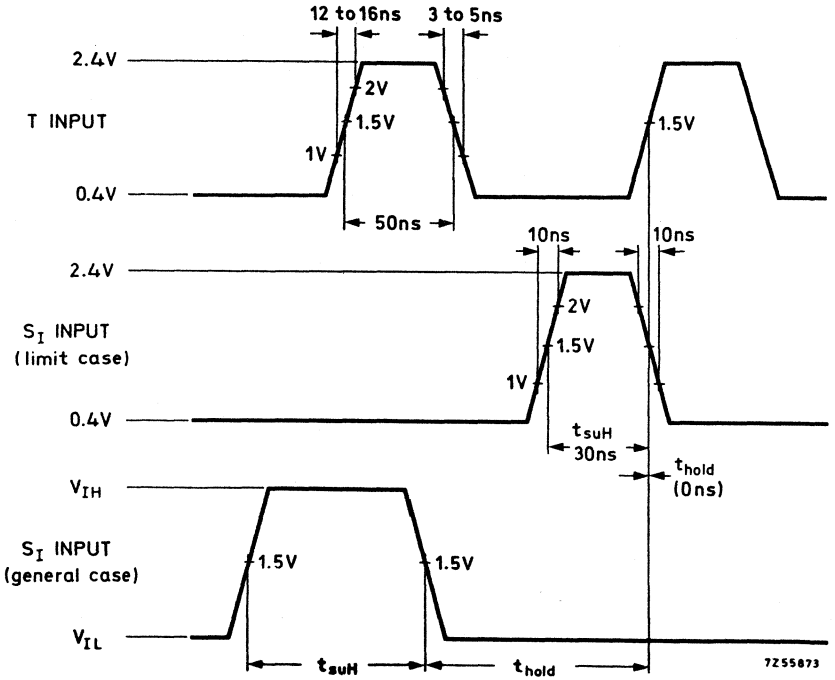


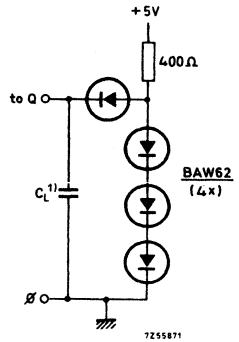
CHARACTERISTICS (continued)





CHARACTERISTICS (continued)





1) C_L includes probe and jig capacitance

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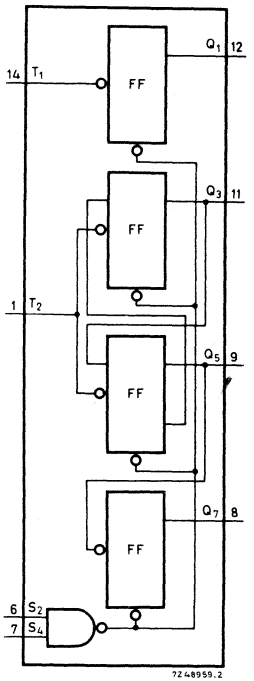
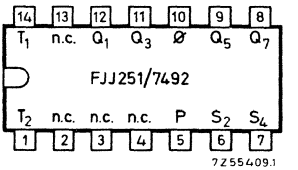


SINGLE ASYNCHRONOUS 4-BIT BINARY COUNTER

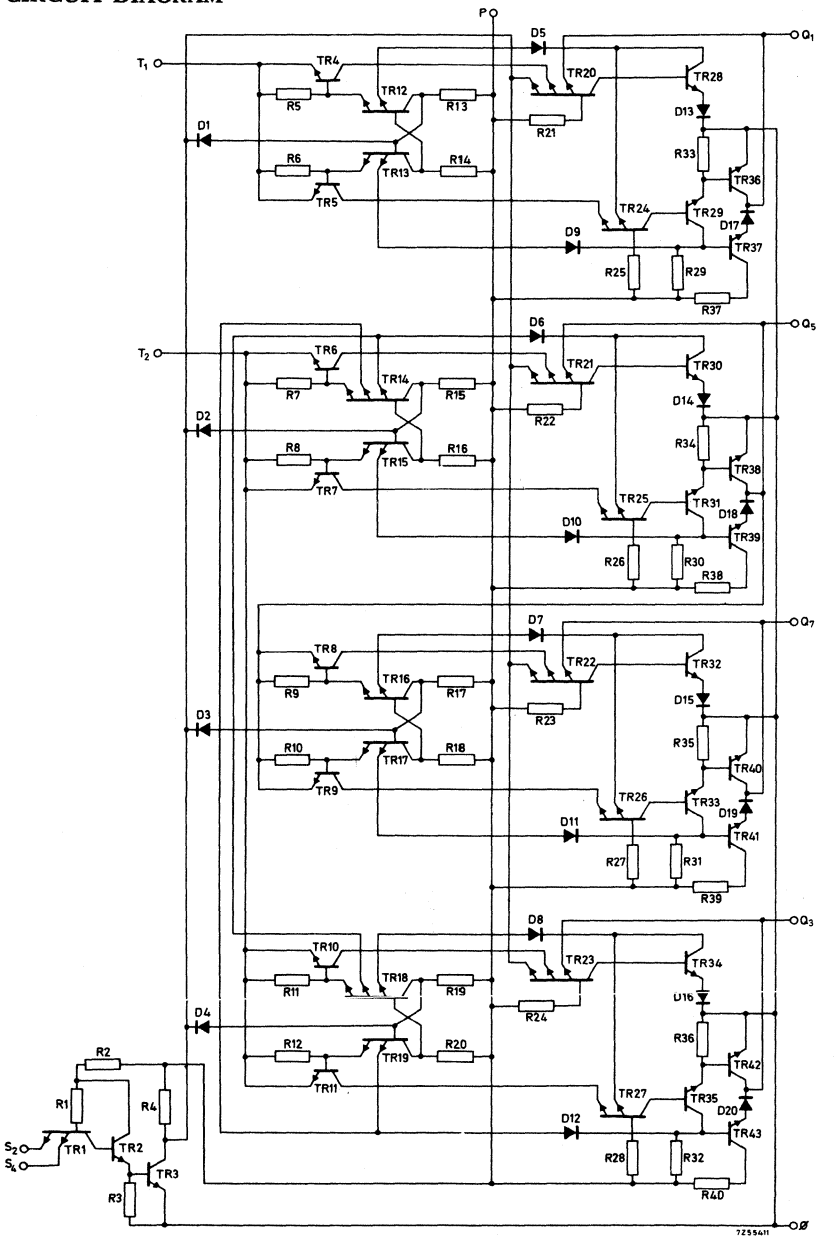


PACKAGE OUTLINE:

14 lead plastic dual in-line (type A)
(See General Section)

QUICK REFERENCE DATA			
Supply voltage	V_P	5.0 ± 5%	V
Operating ambient temperature	T_{amb}	0 to +70	°C
Maximum operating frequency	f	10	MHz
Available d.c. fan-out (full temperature range)	N_a	≥ 10	
D.C. noise margin (full temperature range)	M_L	> 0.4 typ. 1.0	V V
Average power consumption (total) T_{amb} = 25 °C	P_{av}	typ. 155	mW

CIRCUIT DIAGRAM



The FJJ251/7492 is a high-speed asynchronous 4-bit binary counter with four master-slave flip-flops which are internally connected to provide a divide-by-two and a divide-by-six counter. By using an external connection a count of twelve can be obtained. A gated line, direct reset inhibits the count and simultaneously all flip-flop outputs return to the LOW state.

For use as a divide-by-twelve counter, externally connect Q_1 to T_2; apply the count pulses to T_1.

Simultaneous divisions by 2, 6 and 12 are available at the outputs Q_1, Q_5 and Q_7 as shown in the function table below. For use as a divide-by-six counter, apply the count pulses to T_2.

Simultaneous divisions by 3 and 6 are available at the outputs Q_5 and Q_7.

The first flip-flop (T_1 and Q_1) can be used independently if the reset function coincides with reset of the divide-by-six counter.

FUNCTION TABLE

count	outputs			
	Q_1	Q_3	Q_5	Q_7
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	L	L	H
7	H	L	L	H
8	L	H	L	H
9	H	H	L	H
10	L	L	H	H
11	H	L	H	H

Notes:

1. Q_1 connected to T_2
2. To reset all outputs in the LOW state, S_2 and S_4 inputs must be HIGH.
3. Either S_2 or S_4 (or both) must be LOW to count.

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	7.0	V
Input voltage	V_T; V_S	max.	5.5	V [1]
Peak negative input voltage (T, S)	$-V_M$	max.	2	V [2]
Storage temperature	T_{stg}	-65 to	+150	°C
Operating ambient temperature	T_{amb}	0 to	+70	°C

[1] In addition the input voltage between any two T inputs or between any two S inputs: max. 5.5 V.

[2] Pulse duration $t_p = 20$ ns; repetition frequency $f = 5$ MHz; source resistance $R_S \geq 75\Omega$.

CHARACTERISTICS

		T_{amb} (°C)			Conditions and References	
		0	25	75	V_P (V)	
STATIC DATA						
Voltages						
Input threshold LOW						
S_2; S_4; T_1	V_{S2Lmax} } V_{S4Lmax} } V_{T1Lmax}	0.8	0.8	0.8 V	4.75	
T_2	V_{T2Lmax}	0.6	0.6	0.6 V	4.75	
Input threshold HIGH						
S_2; S_4; T_1	V_{S2Hmin} } V_{S4Hmin} } V_{T1Hmin}	2.0	2.0	2.0 V	4.75	
T_2	V_{T2Hmin}	2.2	2.2	2.2 V	4.75	
Output LOW						
Q_1; Q_3; Q_5; Q_7	V_{Q1Lmax} } V_{Q3Lmax} } V_{Q5Lmax} } V_{Q7Lmax}	0.4	0.4	0.4 V	4.75	Q_1 connected to T_2 $I_Q = I_{QLmax}$
Output HIGH						
Q_1; Q_3; Q_5; Q_7	V_{Q1Hmin} } V_{Q3Hmin} } V_{Q5Hmin} } V_{Q7Hmin}	2.4	2.4	2.4 V	4.75	Q_1 connected to T_2 $I_Q = -I_{QHmax}$
Currents						
Input LOW: S_2 S_4	$-I_{S2Lmax}$ } $-I_{S4Lmax}$ }	1.6	1.6	1.6 mA	5.25	$V_S = V_{QLmax}$
T_1	$-I_{T1Lmax}$	3.2	3.2	3.2 mA	5.25 }	$V_T = V_{QLmax}$
T_2	$-I_{T2Lmax}$	6.4	6.4	6.4 mA	5.25 }	
Input HIGH: S_2 S_4	I_{S2Hmax} } I_{S4Hmax} }	40	40	40 μA	5.25	$V_S = V_{QHmin}$ 1)
T_1	I_{T1Hmax}	80	80	80 μA	5.25 }	$V_T = V_{QHmin}$ 2)
T_2	I_{T2Hmax}	160	160	160 μA	5.25 }	
Output LOW						
Q_1; Q_3; Q_5; Q_7	I_{Q1Lmax} } I_{Q3Lmax} } I_{Q5Lmax} } I_{Q7Lmax}	16	16	16 mA	4.75	

1) Input current 1 mA at V_S = 5.5 V.
2) Input current 1 mA at V_T = 5.5 V.

CHARACTERISTICS (continued)

		T_{amb} (°C)			Conditions and References	
		0	25	75	V_P (V)	
STATIC DATA (continued)						
Output HIGH						
Q_1; Q_3; Q_5; Q_7	$-I_{Q1Hmax}$ } $-I_{Q3Hmax}$ } $-I_{Q5Hmax}$ } $-I_{Q7Hmax}$ }	0.4	0.4	0.4 mA	4.75	
Output short circuited						
Q_1; Q_3; Q_5; Q_7 (see note 2)	$-I_{Q1scmin}$ } $-I_{Q3scmin}$ } $-I_{Q5scmin}$ } $-I_{Q7scmin}$ }	18	18	18 mA	5.25	$V_Q = 0$; $V_S = V_T = 0$
	$-I_{Q1scmax}$ } $-I_{Q3scmax}$ } $-I_{Q5scmax}$ } $-I_{Q7scmax}$ }	57	57	57 mA	5.25	$V_Q = 0$; $V_S = V_T = 0$
SUPPLY DATA						
Supply current	I_P typ.	–	31	– mA	5.0	All inputs and outputs
	<	51	51	51 mA	5.25	open
DYNAMIC DATA						
Rise propagation delay time (note 1)	t_{pdr} typ.	–	60	– ns	5	$C_L = 15$pF; $R_L = 390\ \Omega$
	t_{pdr} <	–	100	– ns	5	
Fall propagation delay time (note 1)	t_{pdf} typ.	–	60	– ns	5	
	t_{pdf} <	–	100	– ns	5	
Rise time	t_r <	–	10	– ns	5	f = 1 MHz; duty cycle: 0.5
Fall time	t_f <	–	10	– ns	5	
Trigger time HIGH	t_{T1H}; t_{T2H} <	–	50	– ns	5	
Trigger time LOW	t_{T1L}; t_{T2L} <	–	50	– ns	5	
Width of pulse S_2 and S_4, LOW	t_{S2L}; t_{S4L} <	–	50	– ns	5	

Note 1:

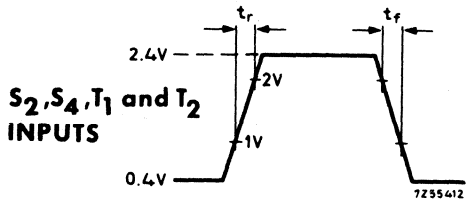
All four outputs loaded. Output Q_1 connected to input T_2.

Note 2:

Not more than one output should be short circuited at a time.

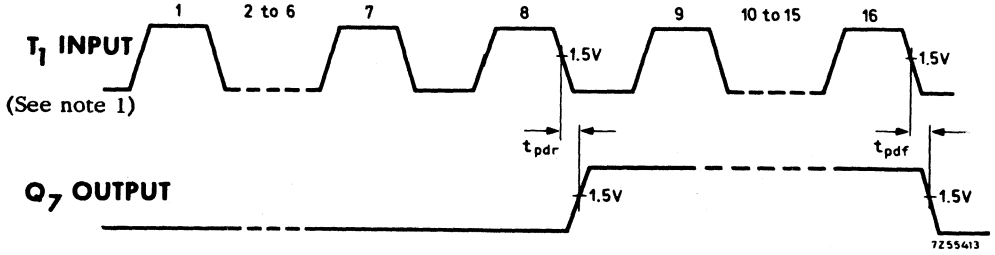
CHARACTERISTICS (continued)

DYNAMIC DATA



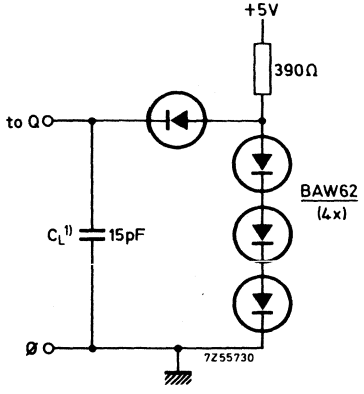
Pulse generator:

$t_r < 10$ ns
$t_f < 10$ ns
f = 1 MHz
duty cycle $\delta = 0.5$



Waveforms inllustrating measurement of t_{pdr} and t_{pdf}

Note 1:
T_1 input (Q_1 output connected to T_2 input)



To outputs Q_3, Q_5 and Q_7 the same loading circuit.

[1]) Including probe and jig capacitance.

DUAL JK MASTER-SLAVE FLIP-FLOP

For data of this type please refer to FJJ121/7473

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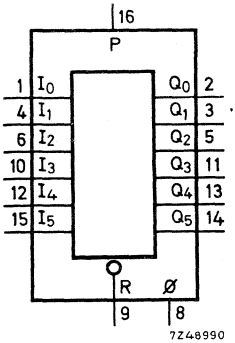
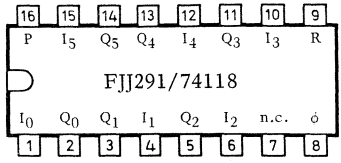
HEX SET-RESET LATCH

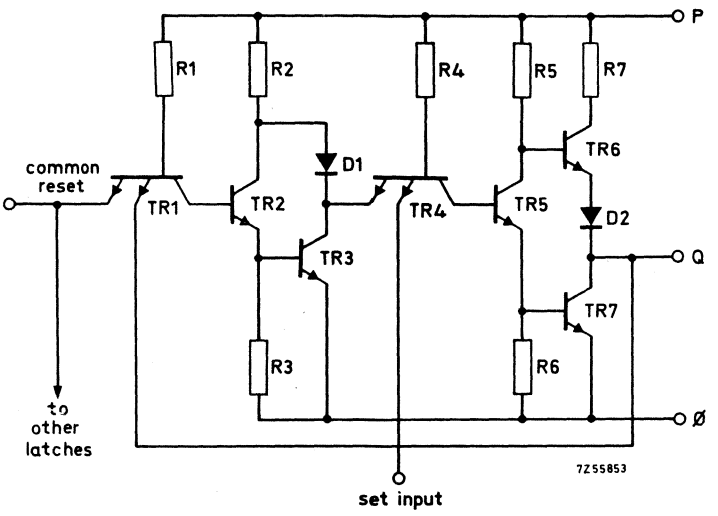




QUICK REFERENCE DATA				
Supply voltage	V_P		5.0 ±5%	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Available d.c. fan-out (full temperature range)	N_a	≥	10	
D.C. noise margin (full temperature range)	M_L	>	0.4	V
		typ.	1.0	V
Average power consumption (total) T_{amb} = 25 °C	P_{av}	typ.	180	mW

PACKAGE OUTLINE 16 lead plastic dual in-line (type A) (See General Section).

CIRCUIT DIAGRAM of one latch (six in one package)



LOGIC FUNCTIONS

The circuit employs standard TTL-NAND gates cross-coupled to form six set-reset flip-flops as latches, each latch having a set input and a TTL output. There is also an unbuffered common reset line to facilitate external reset of the complete latch array.

Function table (each gate)

SET	RESET	OUTPUT Q
L	L or H	H
H	L	L
H	H	store

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134).

Supply voltage	V_P	max.	7.0	V
Input voltage (all inputs)	V_I	max.	5.5	V
Peak negative input voltage	$-V_{IM}$	max.	2	V[1]
Storage temperature	T_{stg}		−65 to +150	°C
Operating ambient temperature	T_{amb}		0 to +70	°C

[1]) Pulse duration t_p = 20 ns; repetition frequency f = 5 MHz; source resistance R_S ≥75 Ω.

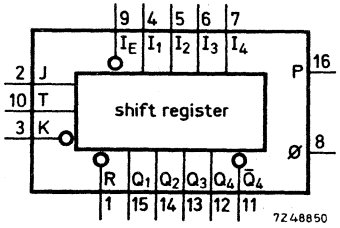
CHARACTERISTICS

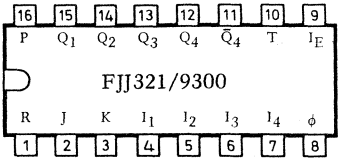
		T_{amb} (0°C)				Conditions and references	
		0	25	70		V_P (V)	
STATIC DATA							
Voltages							
Input threshold LOW (any input)	V_{ILmax}	0.8	0.8	0.8	V		
Input threshold HIGH (any input)	V_{IHmin}	2.0	2.0	2.0	V		
Output LOW	V_{QLmax}	0.4	0.4	0.4	V	4.75	$I_Q = I_{QLmax}$
Output HIGH	V_{QHmin}	2.4	2.4	2.4	V	4.75	$-I_Q = -I_{QHmax}$
Currents							
Input LOW							
I_0 to I_5	$-I_{ILmax}$	1.6	1.6	1.6	mA	5.25	$V_I = V_{QLmax}$; $I_Q = 0$
R	$-I_{RLmax}$	8.0	8.0	8.0	mA	5.25	$V_R = V_{QLmax}$; $I_Q = 0$
Input HIGH							
I_0 to I_5	I_{IHmax}	40	40	40	µA	5.25	$V_G = V_{QHmin}$; $I_Q = 0$
R	I_{RHmax}	200	200	200	µA	5.25	$V_G = V_{QHmin}$; $I_Q = 0$
Output LOW	I_{QLmax}	16	16	16	mA	4.75	
Output HIGH	$-I_{QHmax}$	0.4	0.4	0.4	mA	4.75	
Output short circuited	$-I_{QSCmin}$	18	18	18	mA	5.25	$V_Q = 0$
	$-I_{QSCmax}$	57	57	57	mA	5.25	$V_Q = 0$
SUPPLY DATA							
Supply current	I_P typ.	30	30	30	mA	5.0	
	I_P <	60	60	60	mA	5.25	
DYNAMIC DATA							
Performance							
Rise propagation delay time	t_{pdr} typ.	-	18	-	ns	5.0	N = 10; C_L = 15 pF; R_L = 400 Ω
I_0 to $I_5 \rightarrow Q$	t_{pdr} <	-	29	-	ns	5.0	
Fall propagation delay time	t_{pdf} typ.	-	18	-	ns	5.0	
$R \rightarrow Q$	t_{pdf} <	-	29	-	ns	5.0	
	t_{pdf} typ.	-	10	-	ns	5.0	
I_0 to $I_5 \rightarrow Q$	t_{pdf} <	-	17	-	ns	5.0	

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

SINGLE 4-BIT SHIFT REGISTER





QUICK REFERENCE DATA				
Supply voltage	V_P		5.0 ± 5 %	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Typical operating frequency	f	typ.	25	MHz
D.C. noise margin (full temperature range)	M_L	≥	0.4	V
Total power dissipation	P_{tot}	typ.	300	mW

GENERAL DESCRIPTION

The FJJ321/9300 four bit shift register may be used in shift-left or shift-right mode. Date transfers can be any combination from the serial and parallel inputs and outputs. Its features include: 25 MHz typical shift frequency; a J and K input to the first stage; asynchronous common clear input; synchronous parallel entry of input data is possible by using the input enable (I_E) facility.

PACKAGE OUTLINE 16 lead plastic dual in-line (type A) (See General Section).

FUNCTIONAL DESCRIPTION

The logic symbol provides an indication of the functional characteristics of the FJJ321/9300 four bit shift register. Several special logic features providing a high degree of general usefulness are described below:

1. A J and inverted K input are provided to the first flip-flop in the register. This type of input is the same as the more common JK input except that the low voltage level activates the inverted K input. Both inputs can be used for more general applications. The simple D type input that is most appropriate for a shift register can be easily obtained by simply tying the two inputs together.
2. Parallel inputs (I) for all four stages are provided. These will determine the next condition of the shift register synchronous with the trigger input (T), whenever the input enable (I_E) input is LOW. With the input enable LOW the device appears as four common triggered D flip-flops. When the input enable is HIGH, or not connected, the shift register performs a one bit shift for each trigger pulse. In both cases the next state of the flip-flops occurs after the LOW to HIGH transition of the trigger input.
4. An internal trigger buffer provides both reduced trigger input loading, and the ability to gate the trigger with only a single NAND gate.
5. The output in HIGH state is provided for all four stages. Output LOW state is also provided for the last stage.
6. A master asynchronous clear (R) input sets all stages LOW, independent of the condition of any other input.

FUNCTION TABLE (for serial entry)

t_n		$t_{(n+1)}$
J	$\overline{K}$	$Q_{1(n+1)}$
L	L	L
L	H	Q_1 *)
H	L	$\overline{Q_1}$ *)**)
H	H	H

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
t_n = bit time before trigger pulse
t_{n+1} = bit time after 1 trigger pulse

input enable (I_E) is HIGH
clear input (R) is HIGH

*) n: no change
**) n: toggle

RATINGS limiting values in accordance with the Absolute Maximum System (IEC134).

Supply voltage	V_P	−0.5 to +7	V
Input voltage	All inputs	−0.5 to +5.5	V
Output voltage (HIGH state)	V_Q	−0.5 to V_P	V
Storage temperature	T_{stg}	−65 to +150	°C
Operating ambient temperature	T_{amb}	0 to +70	°C

CHARACTERISTICS

		T_{amb} (°C)			Conditions and references	
		0	25	70	V_P (V)	
STATIC DATA						
Voltages						
Input threshold LOW (any input)	V_{ILmax}	0.8	0.8	0.8 V		
Input threshold HIGH (any input)	V_{IHmax}	2.0	2.0	2.0 V	4.75	I_{QL} = 8.5 mA
Output LOW	V_{QLmax}	0.4	0.4	0.4 V	5.25	I_{QL} = 9.6 mA
Output HIGH	V_{QHmin}	2.4	2.4	2.4 V	4.75	$-I_{QH}$ = 0.36 mA
Currents						
Input LOW						
J; K; R; I_1; I_2; I_3; I_4	$-I_{ILmax}$	1.6 1.41	1.6 1.41	1.6 mA 1.41 mA	5.25 4.75	$V_I = V_{QLmax}$
Input HIGH						
J; K; R; I_1; I_2; I_3; I_4	I_{IHmax}	-	60	60 µA	5.25	V_I = 4.5 V
Output LOW	I_{QLmax}	9.6 8.46	9.6 8.46	9.6 mA 8.46 mA	5.25 4.75	$V_Q = V_{QLmax}$
Output HIGH	$-I_{QHmax}$	-	360	360 µA	5.25	$V_Q = V_{QHmin}$

CHARACTERISTICS (continued)

		Tamb (°C)			Conditions and references	
		0	25	70	V_P (V)	
DYNAMIC DATA					5.0	C_L = 15 pF
Performance						
Rise propagation dealy time						
T→Q	t_{pdr} ≤	–	35	– ns		
	t_{pdr} typ.	–	20	– ns		
Fall propagation delay time						
T→Q	t_{pdf} ≤	–	45	– ns		
R→Q	t_{pdf} typ.	–	25	– ns		
	t_{pdf} typ.	–	35	– ns		
Signal requirements						
Set-up time for J, K, I_1 to I_4	t_{SU} ≥	–	35	– ns		
	t_{SU} typ.	–	17	– ns		
I_E	t_{SU} ≥	–	45	– ns		
	t_{SU} typ.	–	26	– ns		
recovery time for R→T	t_{rec} typ.	–	20	– ns		
release time for						
I_E	t_{rel} ≤	–	10	– ns		
	t_{rel} typ.	–	25	– ns		
J, K, I_1 to I_4	t_{rel} ≤	–	0	– ns		
	t_{rel} typ.	–	16	– ns		
Minimum pulse width:						
T	t_{TH} ≥	–	35	– ns		
	t_{TH} typ.	–	15	– ns		
	t_{TL} ≥	–	35	– ns		
	t_{TL} typ.	–	15	– ns		
R	t_{RL} typ.	–	15	– ns		
Shift right frequency	f_{SR} ≥	–	15	– MHz		
	f_{SR} typ.	–	25	– MHz		

CHARACTERISTICS (continued)

Set-up time: t_{su}

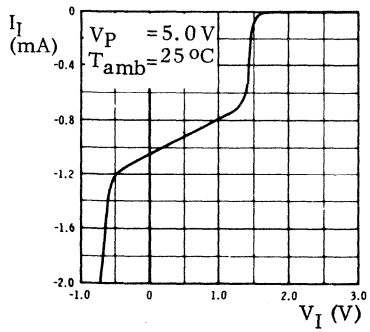
Defined as the **minimum** time required for the logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order for the flip-flops to respond.

Release time : t_{rel}

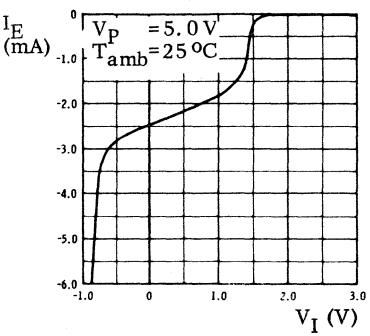
Defined as the maximum time allowed for the logic level to be present at the logic input prior to the trigger input (T) transition from LOW to HIGH in order for the flip-flop(s) not to respond.

Recovery time : t_{rec}

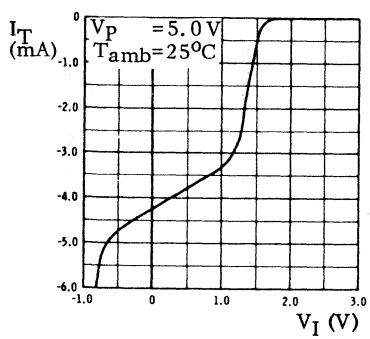
Defined as the minimum time required between the LOW to HIGH transition of the clear pulse (R) and the trigger input (T) transition from LOW to HIGH in order for the flip-flop(s) to respond to the trigger input (T).



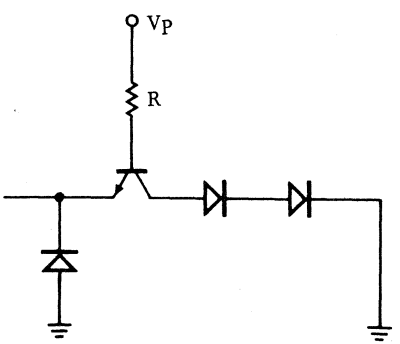
Input curve for: I_1; I_2; I_3; I_4; J; K; R



Input curve for: I_E

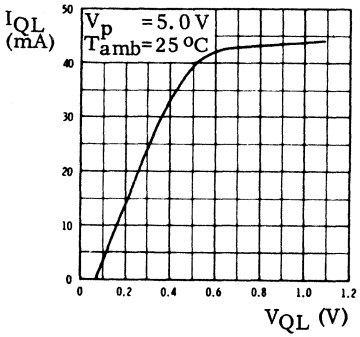


Input curve for: T

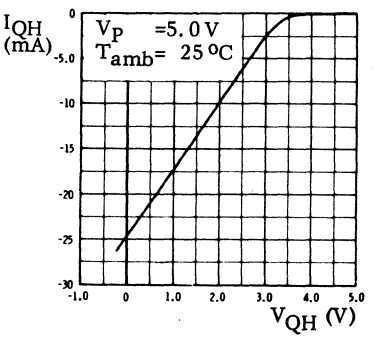


Equivalent input circuit

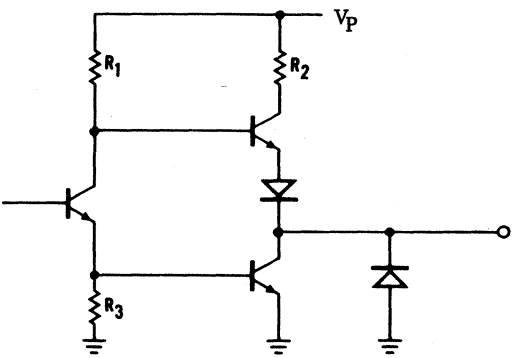
CHARACTERISTICS (continued)



Output curve (LOW state)

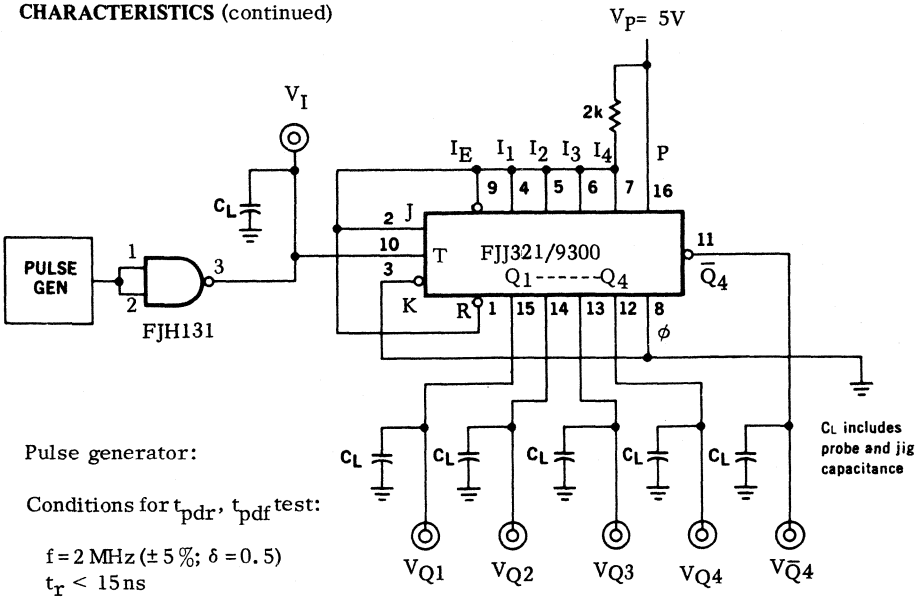


Output curve (HIGH state)



Equivalent output circuit

CHARACTERISTICS (continued)



Pulse generator:

Conditions for t_{pdr}, t_{pdf} test:

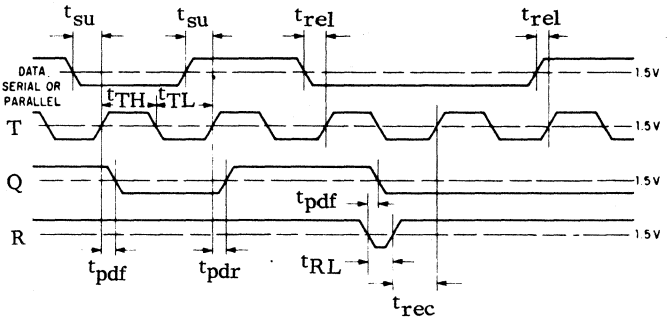
f = 2 MHz (± 5 %; δ = 0.5)
t_r < 15 ns
t_f < 15 ns
Amplitude = 4 V

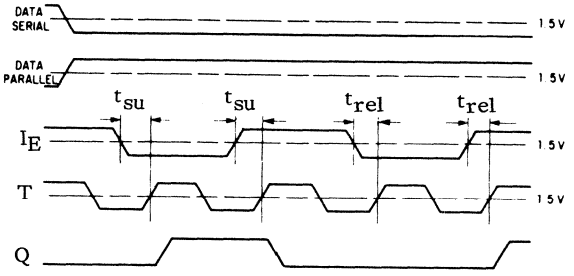
Conditions for shift right frequency test:

f = 15 MHz (with pulse width adjustment so that V_I has δ = 0.5
t_r < 15 ns
t_f < 15 ns
Amplitude = 4 V

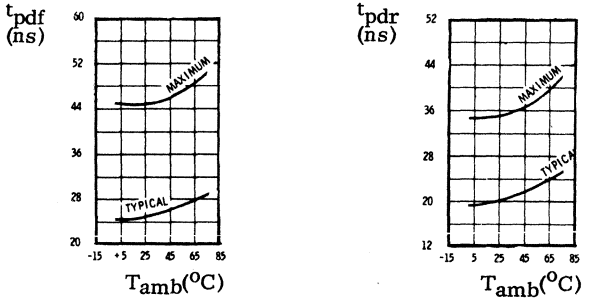
Switching times and shift right frequency test circuit

CHARACTERISTICS (continued)





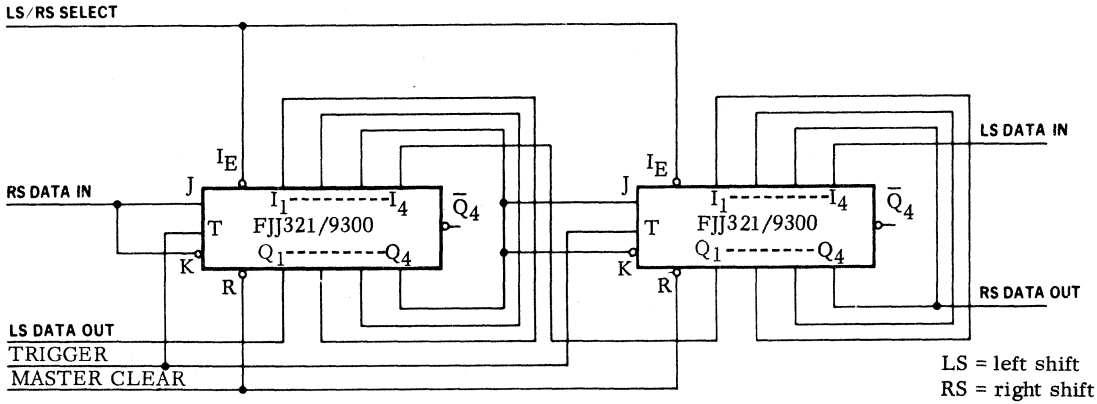
Waveforms illustrating dynamic data



Propagation delay times (T→Q) as a function of temperature

APPLICATION INFORMATION

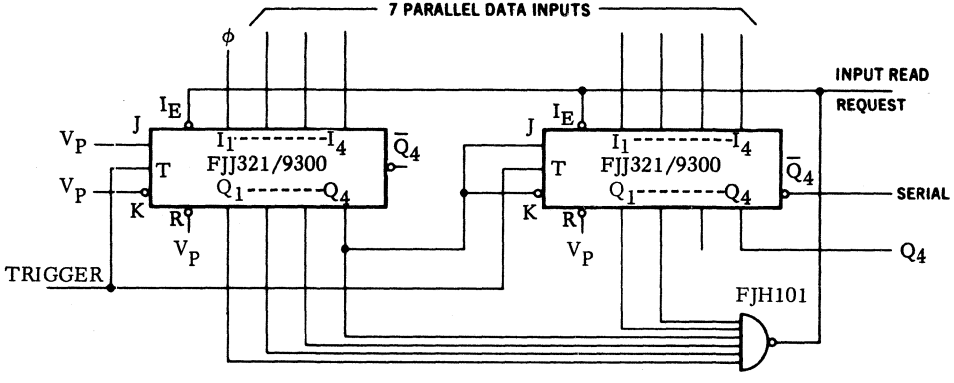
The FJJ321/9300 has been designed to be useful in a wide variety of applications.
The multifunctional capability is illustrated by the applications shown.



Eight bit left/right shift register

This register shifts left or right on each shift trigger, depending upon the condition of the LS/RS select input. If this input is HIGH, right shift occurs and if LOW, left shift occurs.

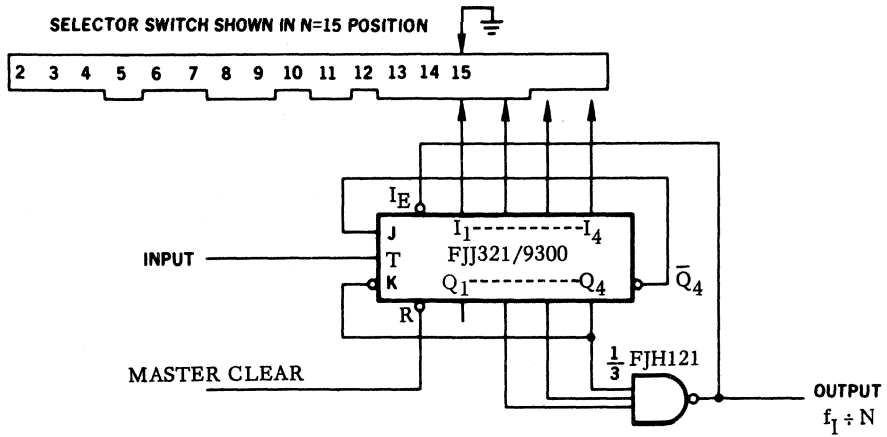
APPLICATION INFORMATION (continued)



Seven bit parallel to serial converter

This parallel to serial converter uses a marker bit, to count the data bits shifted out, so that a parallel load enable (input READ REQUEST) is generated to load the next parallel word for conversion at the correct time.

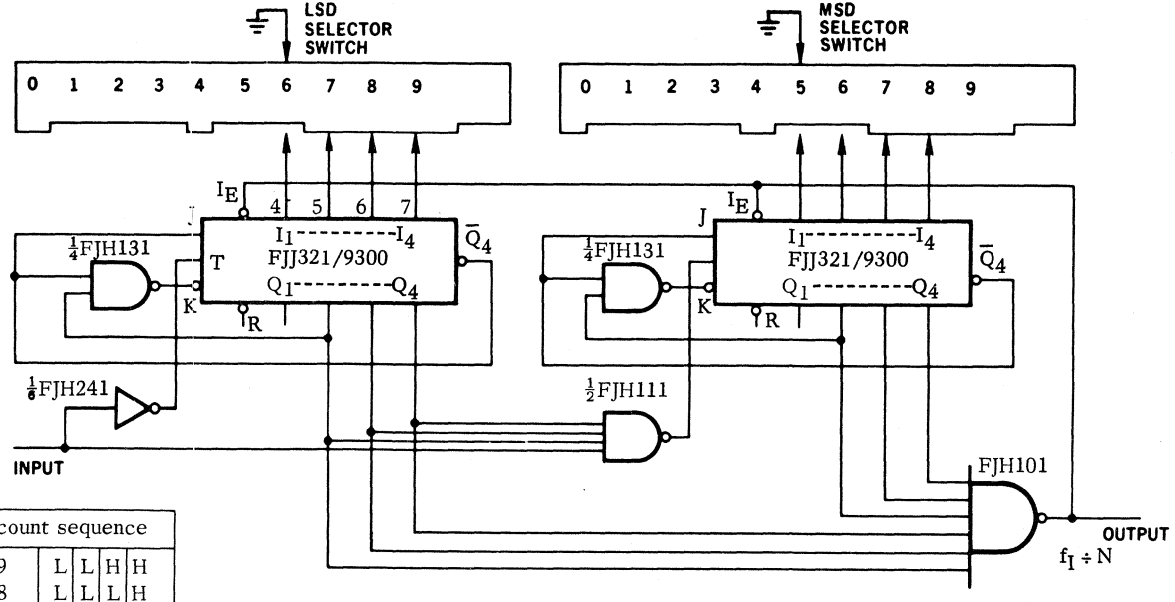
APPLICATION INFORMATION (continued)



Divide by N counter for N = 2 to 15

This counter produces an output pulse for every N input pulses, where the number N is determined by the setting of the slide selector switch as shown or by logic inputs to the parallel data lines from an external source.

APPLICATION INFORMATION (continued)



count sequence				
9	L	L	H	H
8	L	L	L	H
7	L	L	L	L
6	H	L	L	L
5	H	H	L	L
4	L	H	H	L
3	H	L	H	H
2	H	H	L	H
1	H	H	H	L
0	L	H	H	H

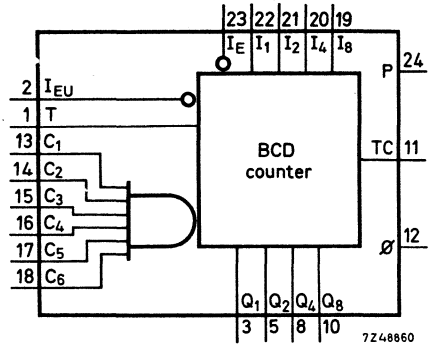
This circuit divides by any number N from 1 to 100. The selected N is one greater than is shown on the slide switches.

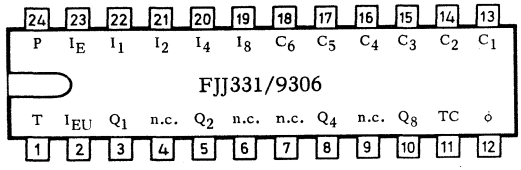
As an example the switches are showing 56, therefore the circuit will divide by 57 with this setting.

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

UP/DOWN COUNTER





QUICK REFERENCE DATA				
Supply voltage	V_P		5.0 ± 5 %	V
Operating ambient temperature	T_{amb}		0 to +70	°C
D.C. noise margin (full temperature range)	M_L	≥	0.4	V
Average power consumption (total)	P_{av}	typ.	350	mW

PACKAGE OUTLINE 24 lead ceramic dual in-line (See General Section)

LOGIC FUNCTION

$C = C_1 \cdot C_2 \cdot C_3 \cdot C_4 \cdot C_5 \cdot C_6$

Function table

I_E	I_{EU}	C	Mode
L	L	L	presetting
L	L	H	presetting
L	H	L	presetting
L	H	H	presetting
H	H	H	count-up
H	L	H	count-down
H	H	L	no change
H	L	L	no change

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with Absolute Maximum System (IEC 134).

Supply voltage	V_P	−0.5 to +7.0	V
Input voltage (all inputs)	V_I	−0.5 to +5.5	V
Output voltage (HIGH state)	V_Q	−0.5 to V_P	V
Storage temperature	T_{stg}	−65 to +150	°C
Operating ambient temperature	T_{amb}	0 to +70	°C

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references	
		0	25	70		V_P (V)	
STATIC DATA							
Voltages							
Input threshold LOW (any input)	V_{ILmax}	0.8	0.8	0.8	V		
Input threshold HIGH (any input)	V_{IHmin}	2.0	2.0	2.0	V		
Output LOW	V_{QLmax}	0.4	0.4	0.4	V	5.25	I_{QL} = 9.6 mA
Output HIGH	V_{QHmin}	2.4	2.4	2.4	V	4.75	$-I_{QH}$ = 0.36 mA
Currents							
Input LOW							
C_1; C_2; C_3; C_4; C_5; C_6; I_{EU}	$-I_{ILmax}$	1.6	1.6	1.6	mA	5.25	$V_I = V_{QLmax}$
T; I_E	$-I_{ILmax}$	3.2	3.2	3.2	mA	5.25	$V_I = V_{QLmax}$
I_1; I_2; I_4; I_8	$-I_{ILmax}$	1.07	1.07	1.07	mA	5.25	$V_I = V_{QLmax}$
Input HIGH							
C_1; C_2; C_3; C_4; C_5; C_6; I_{EU}	I_{IHmax}	60	60	60	µA	5.25	V_I = 4.5 V
T; I_E	I_{IHmax}	120	120	120	µA	5.25	V_I = 4.5 V
I_1; I_2; I_4; I_8	I_{IHmax}	40	40	40	µA	5.25	V_I = 4.5 V
SUPPLY DATA							
Supply current	I_P typ.	-	70	-		5.0	

CHARACTERISTICS (continued)

		T_{amb} (°C) 0 25 **70**	Conditions and references	
			V_P (V)	
DYNAMIC DATA				All tests at C_L = 15 pF
Performance				Fig's on page 5
Rise propagation delay time				
T → Q	t_{pdr} typ.	- 20 - ns	5.0	Fig. 1
T → TC	t_{pdr} typ.	- 40 - ns	5.0	
Fall propagation delay time				
T → Q	t_{pdf} typ.	- 20 - ns	5.0	
T → TC	t_{pdf} typ.	- 30 - ns	5.0	
Signal requirements				
Set-up time				
C → T	t_{su} typ.	- 25 - ns	5.0	Fig. 2
I → T	t_{su} typ.	- 15 - ns	5.0	Fig. 3
I_E → T	t_{su} typ.	- 20 - ns	5.0	Fig. 3
Release time				
C → T	t_r typ.	- 25 - ns	5.0	Fig. 2
I → T	t_r typ.	- 15 - ns	5.0	Fig. 3
I_E → T	t_r typ.	- 20 - ns	5.0	Fig. 3

Set-up time

t_{su} is defined as the minimum time required for the logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order for the flip-flop(s) to respond.

Release time

t_r is defined as the maximum time allowed for the logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order for the flip-flop(s) not to respond.

CHARACTERISTICS (continued)

DYNAMIC DATA

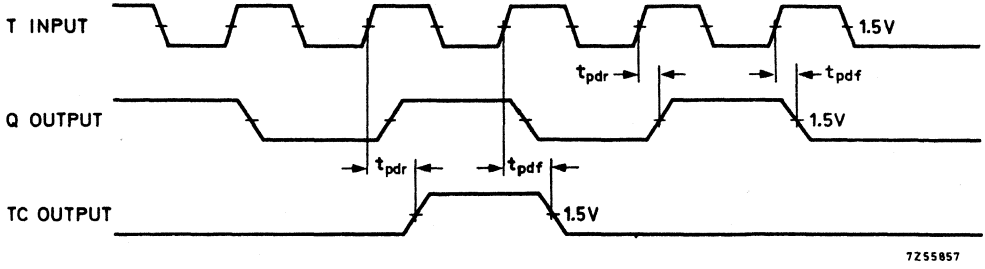


Fig. 1

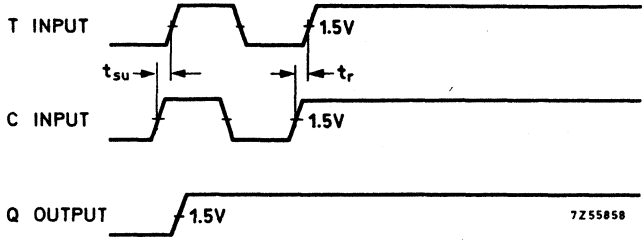


Fig. 2

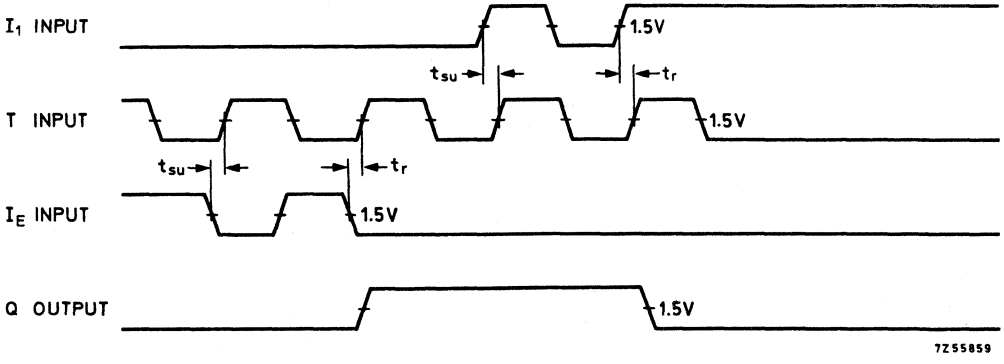
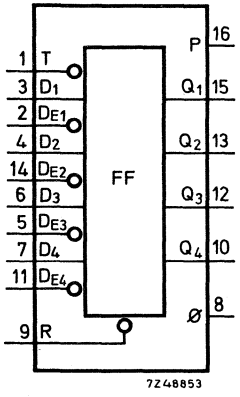


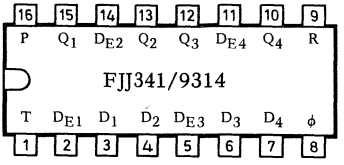
Fig. 3

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

QUADRUPLE 2-INPUT LATCH FLIP-FLOP





QUICK REFERENCE DATA				
Supply voltage	V_P		5.0 ± 5 %	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Propagation delay time	t_{pd}	typ.	25	ns
D.C. noise margin (full temperature range)	M_L	≥	0.4	V
Total power dissipation	P_{tot}	typ.	175	mW

GENERAL DESCRIPTION

The FJJ341/9314 is a multi-functional 4-bit latch flip-flop. The latch is designed for general purpose storage applications in high speed digital systems. Its features include: use either as a single input quadruple latch D flip-flop or as set/reset latches, active LOW gate-enable input (T) to inhibit destruction of stored data; an overriding master clear (R) which sets all flip-flops LOW; a typical propagation delay of 25 ns.

PACKAGE OUTLINE 16 lead plastic dual in-line (type A) (See General Section).

FUNCTIONAL DESCRIPTION

Latch operation

The **FJJ341/9314** consists of 4 latches with a common active LOW enable input (T) and active LOW master reset input (R). When T goes HIGH, data present in the latches is stored and the state of a latch is no longer affected by the D and D_E inputs. The master reset (R) when activated overrides all other input conditions forcing all latch outputs LOW.
Each of the four latches can be operated in one or two modes:

1. D-type latch; For D-type operation the D_E input of a latch is held LOW. While the common enable (T) is LOW the latch output follows the D input. Information present at the latch output is stored in the latch when the enable (T) goes HIGH.
2. Set/reset latch; During set/reset operation when the common enable (T) is LOW a latch is reset by LOW on the D input, and can be set by LOW on the D_E input if the D input is HIGH. If both D and D_E inputs are LOW, the D input will dominate and the latch will be reset. When the enable (T) goes HIGH, the latch remains in the last state prior to disablement.

The two modes of operation of the **FJH341/9314** latches are shown in the FUNCTION TABLE on page 3.

FUNCTION TABLE

type of operation	inputs				outputs (n + 1)
	R	T	D_1 (D_2; D_3; D_4)	D_{E1} (D_{E2}; D_{E3}; D_{E4})	Q_1 (Q_3; Q_5; Q_7)
D-mode	H	L	L	L	L
	H	L	H	L	H
	H	H	X	X	Q_n
R/S mode	H	L	L	L	L
	H	L	H	L	H
	H	L	L	H	L
	H	L	H	H	Q_n
	H	H	X	X	Q_n
Reset	L	X	X	X	L

Q_n = previous output state

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134).

Supply voltage	V_P		−0.5 to +7	V
Input voltage	All inputs		−0.5 to +5.5	V [1]
Input current	All inputs		−30 to +5	V [1]
Output voltage (HIGH state)	V_Q		−0.5 to V_P	V
Output current (LOW state)	I_Q	max.	30	mA
Storage temperature	T_{stg}		−65 to +150	°C
Operating ambient temperature	T_{amb}		0 to +70	°C

[1]) Either input voltage or input current limit is sufficient to protect the inputs.

CHARACTERISTICS

		T_{amb} (°C)			Conditions and references		
		0	25	70	V_P (V)		
STATIC DATA							
Voltages [1]							
Input threshold LOW (any input)	V_{ILmax}	0.8	0.8	0.8	V		
Input threshold HIGH (any input)	V_{IHmin}	2.0	2.0	2.0	V		
Output LOW	V_{QLmax}	0.4	0.4	0.4	V	5.25	$I_{QL} = I_{QLmax}$ [1]
						4.75	$I_{QL} = I_{QLmax}$ [1]
Output HIGH	V_{QHmin}	2.4	2.4	2.4	V	4.75	$-I_{QH} = -I_{QLmax}$ [1]
Currents							
Input LOW:							
D_{E1};D_{E2};D_{E3};D_{E4}	$-I_{DELmax}$	1.6	1.6	1.6	mA	5.25	$V_I = V_{QLmax}$
R; T	$-I_{ILmax}$	1.6	1.6	1.6	mA	5.25	$V_I = V_{QLmax}$
D_1;D_2;D_3;D_4	$-I_{DLmax}$	2.7	2.7	2.7	mA	5.25	V_I = 0 V [2]
Input HIGH:							
D_{E1};D_{E2};D_{E3};D_{E4}	I_{DEHmax}	–	60	60	µA	5.25	
R;T	I_{IHmax}	–	60	60	µA	5.25	V_I = 4.5 V
D_1;D_2;D_3;D_4	I_{DHmax}	–	90	90	µA	5.25	
Output LOW	I_{QLmax}	14.4	14.4	14.4	mA	5.25	
	I_{QLmax}	12.7	12.7	12.7	mA	4.75	
Output HIGH	$-I_{QLmax}$	–	600	600	µA	5.25	
Supply Data							
Supply current	$I_P \leq$	60	60	60	mA	5.0	
	I_P typ.	–	35	–	mA	5.0	

[1] Inputs at threshold voltage (V_{ILmax} or V_{IHmin}). Output voltages are guaranteed for either the input enabled or input disabled case.

[2] This current is measured at V_I = 0 V to ensure that no current is being absorbed by the device internally. The maximum value given guarantees that the maximum instantaneous current that can flow out of the input at $V_I = V_{QLmax}$ is 2.4 mA.

CHARACTERISTICS (continued)

		T_{amb} (°C)			Conditions and references	
		0	25	75	V_P (V)	
DYNAMIC DATA					5.0	C_L = 15 pF
Performance						
Rise propagation delay time						
T ⟶ Q	t_{pdr} ≤	–	28	– ns		
D ⟶ Q	t_{pdr} ≤	–	18	– ns		
D_E ⟶ Q	t_{pdr} ≤	–	28	– ns		
Fall propagation delay time						
T⟶Q	t_{pdf} ≤	–	28	– ns		
D ⟶ Q	t_{pdf} ≤	–	32	– ns		
R⟶Q	t_{pdf} ≤	–	22	– ns		
Signal requirements						
Set-up time for:						
D ⟶ T	t_{suL} ≥	–	22	– ns		
	t_{suH} ≥	–	7	– ns		
Release time for:						
D ⟶ T	t_{relL} ≥	–	7	– ns		
	t_{relH} ≥	–	0	– ns		
Recovery time for:						
R⟶T	t_{rec} ≥	–	0	– ns		
Hold time for:						
D_E ⟶ D_1	t_{hold} ≥	–	10	– ns		
Pulse width for:						
T	t_{TL} ≥	–	22	– ns		
R	t_{RL} ≥	–	20	– ns		

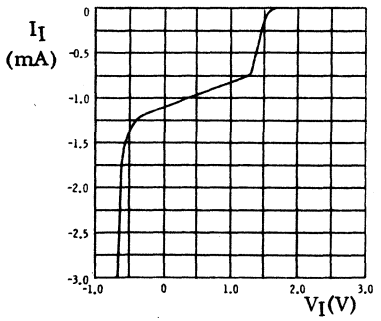
Release time : t_{rel} is defined as the minimum time that the logic level on the D input must remain constant after the Enable (T) transition from LOW to HIGH in order for the latch to retain the correct input information.

Recovery time: t_{rec} is defined as the minimum time that the Enable (T) must remain LOW after the Master Reset (R) transition from LOW to HIGH in order for the latch to recognize and store HIGH input information.

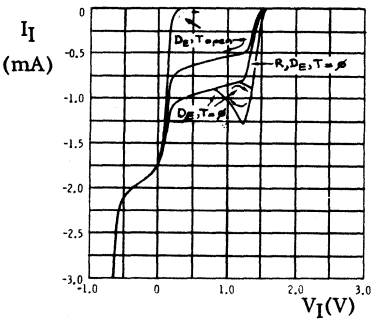
Hold time : t_{hold} is defined as the minimum time required for the D_E input to be HIGH prior to the D input transition from LOW to HIGH to retain a LOW output.

Set-up time : t_{su} is defined as the minimum time required for the logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order for the flip-flop(s) to respond.

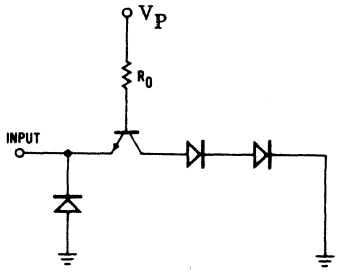
CHARACTERISTICSS (continued) $V_P = 5.0$ V; $T_{amb} = 25^oC$



Input characteristic for: R, T, D_E input

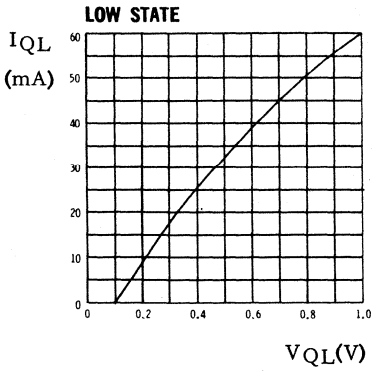


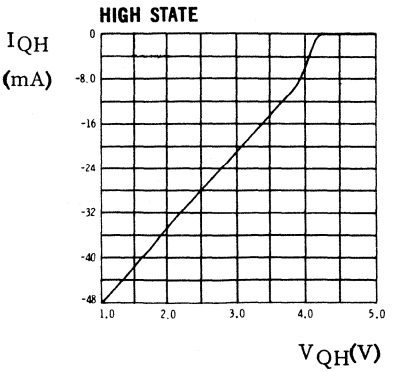
Input characteristic for: D input

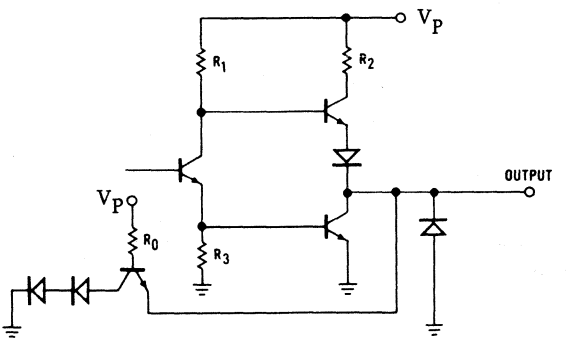


Equivalent input circuit

CHARACTERISTICS (continued) $V_P = 5.0$ V; $T_{amb} = 25\ ^oC$

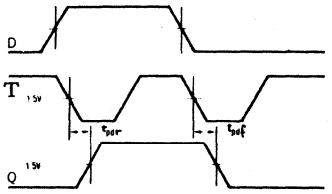






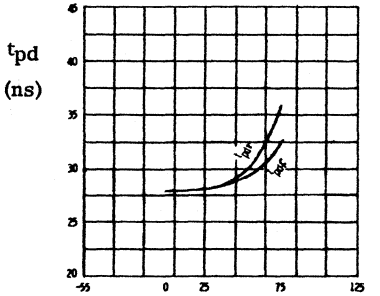
Equivalent output circuit

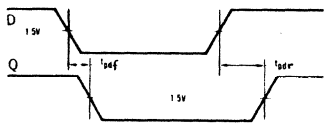
CHARACTERISTICS (continued)



t_{pd} (T→Q)
condition: $D_E = \phi$

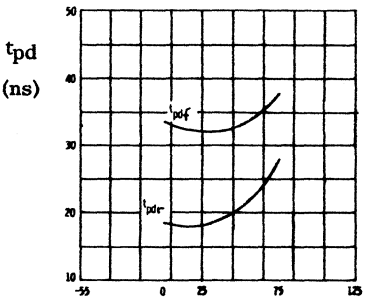
maximum values

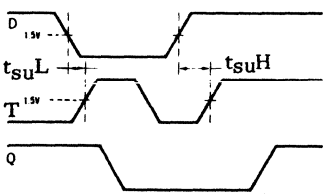




t_{pd} (D→Q)
condition: T = $D_E = \phi$

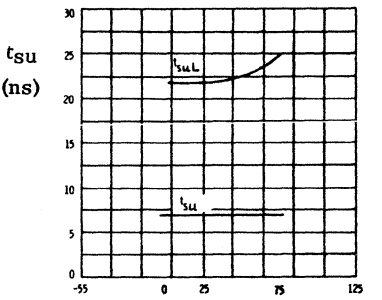
maximum values



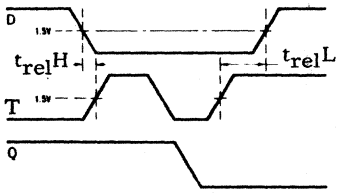


t_{su} (D→T)
condition: $D_E = \phi$

minimum values

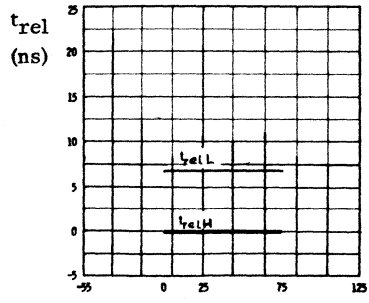


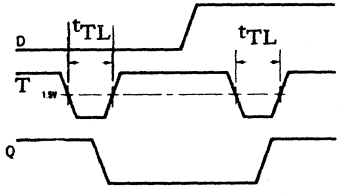
CHARACTERISTICS (continued)



t_{rel} (D⟶T)
condition: $D_E = \phi$

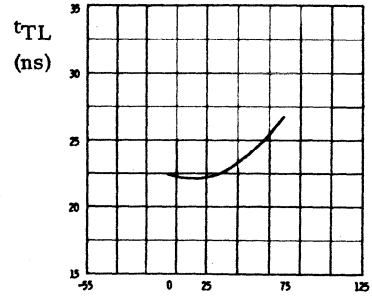
minimum values

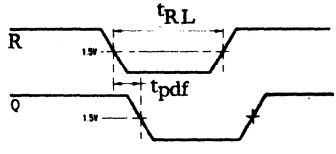




t_{TL}
condition: $D_E = \phi$

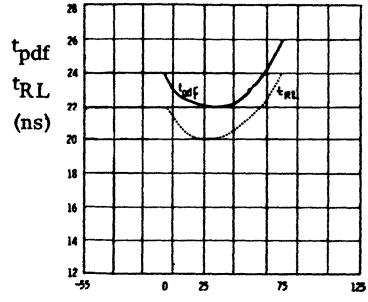
minimum values



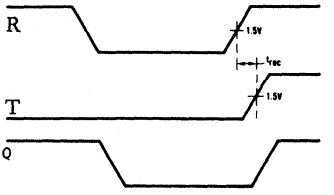


t_{pdf} and t_{RL} (R⟶Q)
condition: $T = D_E = \phi$

—— t_{pdf} (maximum values)
···· t_{RL} (minimum values)

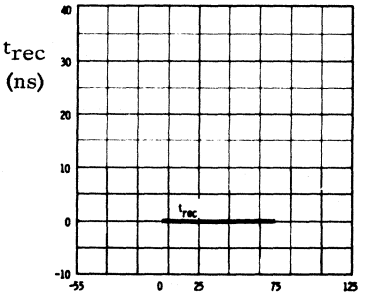


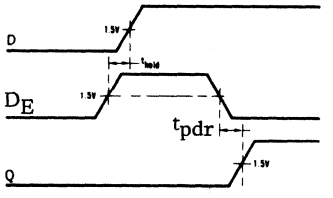
CHARACTERISTICS (continued)



t_{rec} (R → T)
condition: $D_E = \phi$; D = open

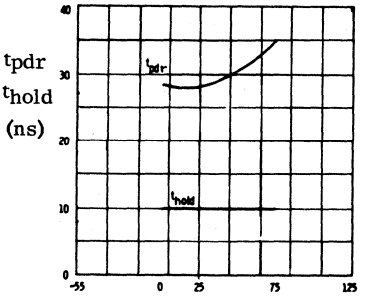
maximum values



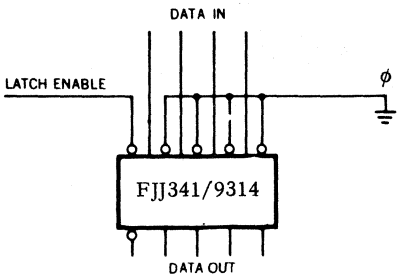


t_{pdr} (D_E → Q)
t_{hold} (D_E → D)
condition: T = ϕ

maximum values

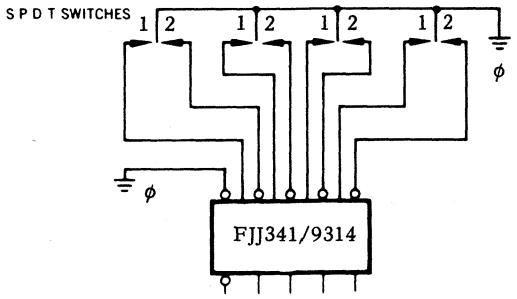


APPLICATION INFORMATION



4-bit storage latch

The figure illustrates the use of the FJJ341/9314 as a D-type storage latch. Data is stored in the latch when the enable line is HIGH.



Contact bounce eliminator

The FJJ341/9314 can be used to eliminate mechanical switch bounce for a single pole double throw switch. The latch operation is that of an active LOW input set/reset latch. The pole of the switch is LOW so that when in the 1 position, the output is LOW and in the 2 position the output is HIGH.

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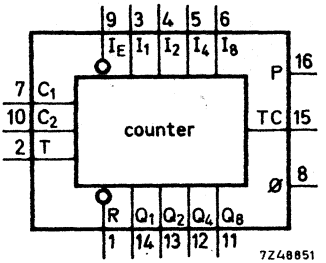
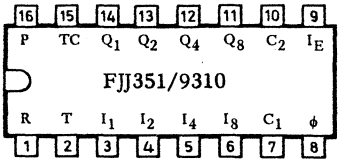
Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

BCD DECADE COUNTER





QUICK REFERENCE DATA			
Supply voltage	V_P	5.0 ±5%	V
Operating ambient temperature	T_{amb}	0 to +70	°C
Typical operating frequency	f	18	MHz
D.C. noise margin (full temperature range)	M_L	≥ 0.4	V
Total power dissipation	P_{tot}	typ. 300	mW

GENERAL DESCRIPTION

The FJJ351/9310 is a high speed synchronous BCD (1-2-4-8 code) decade counter. It has a parallel load facility and an overriding asynchronous master reset. By using the internal carry look-ahead counting technique, several decades of synchronous operation are obtainable with no external gating packages and with operating speeds equivalent to those of a single stage.

PACKAGE OUTLINE 16 lead plastic dual-in (type A) (See General Section).

FUNCTIONAL DESCRIPTION

A clock buffer and inverter drives the four clocked RS master-slave flip-flops in parallel, so that synchronous operation is obtained. When the trigger input (T) is LOW, the slave is steady, but data can enter the master via the R and S inputs. During the LOW to HIGH transition of T, first the data inputs (R and S) are inhibited, so that a later change in the input data will not affect the master; secondly, the now trapped information in the master is transferred to the slave and is reflected at the outputs. When the transfer is completed both the master and the slave are steady, as long as T remains HIGH, regardless of the logic state at any other input to the device. During the HIGH to LOW transition of the trigger input (T), first the transfer path from master to slave is inhibited, leaving the slave steady in its present state. Secondly, the data inputs (R and S) are enabled so that new data can enter the master. As a result of this synchronous operation higher clock frequency is possible and much less external logic is required in most applications. Some restrictions are placed on the manner of selection. First, the transition of C_1 or C_2 from HIGH to LOW or of I_E from LOW to HIGH may occur only when T is HIGH. The remaining transition requirements are specified under "Signal requirements" on page 5.
When a BCD count of 9 has been reached, the counter will recycle to a count of 0 ($Q_1 = Q_2 = Q_4 = Q_8$ = LOW) at the next T transition from LOW to HIGH. If a count greater than 9 is preset into the counter, it will follow the counting sequence shown below. The asynchronous reset (R) clears the counter independent of all other inputs.

FUNCTION TABLE

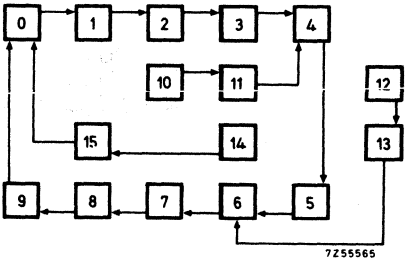
Count Enable	$\overline{I}_E$	mode
H	H	Count up
L	H	No change
X	L	Presetting

Count Enable = $C_1 \cdot C_2$

Terminal count TC = $C_2 \cdot Q_1 \cdot Q_2 \cdot Q_4 \cdot Q_8$

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

COUNT SEQUENCY



RATINGS Limiting values in accordance with Absolute Maximum System (IEC 134).

Supply voltage	V_P	−0.5 to +7.0	V
Input voltage	All inputs	−0.5 to +5.5	V
Output voltage (HIGH state)	V_Q	−0.5 to V_P	V
Storage temperature	T_{stg}	−65 to +150	°C
Operating ambient temperature	T_{amb}	0 to +70	°C

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references	
		0	25	70		V_P (V)	
STATIC DATA							
Voltages							
Input threshold LOW							
(any input)	V_{ILmax}	0.8	0.8	0.8	V		
Input threshold HIGH							
(any input)	V_{IHmin}	2.0	2.0	2.0	V		
Output LOW	V_{QLmax}	0.4	0.4	0.4	V	5.25 4.75	$I_{QL} = I_{QLmax}$
Output HIGH	V_{QHmin}	2.4	2.4	2.4	V	4.75	$-I_{QH} = -I_{QHmax}$
Currents							
Input LOW							
R; C_1	$-I_{ILmax}$	1.6	1.6	1.6	mA	5.25	$V_I = V_{QLmax}$
T; I_E; C_2	$-I_{ILmax}$	3.2	3.2	3.2	mA	5.25	
I_1; I_2; I_4; I_8	$-I_{ILmax}$	1.07	1.07	1.07	mA	5.25	
Input HIGH:							
R; C_1	I_{IHmax}	60	60	60	µA	5.25	V_I = 4.5 V
T; I_E; C_2	I_{IHmax}	120	120	120	µA	5.25	
I_1; I_2; I_4; I_8	I_{IHmax}	40	40	40	µA	5.25	
Output LOW	I_{QLmax}	9.6	9.6	9.6	mA	5.25	
	I_{QLmax}	8.5	8.5	8.5	mA	4.75	
Output HIGH	$-I_{QHmax}$	360	360	360	µA	4.75	

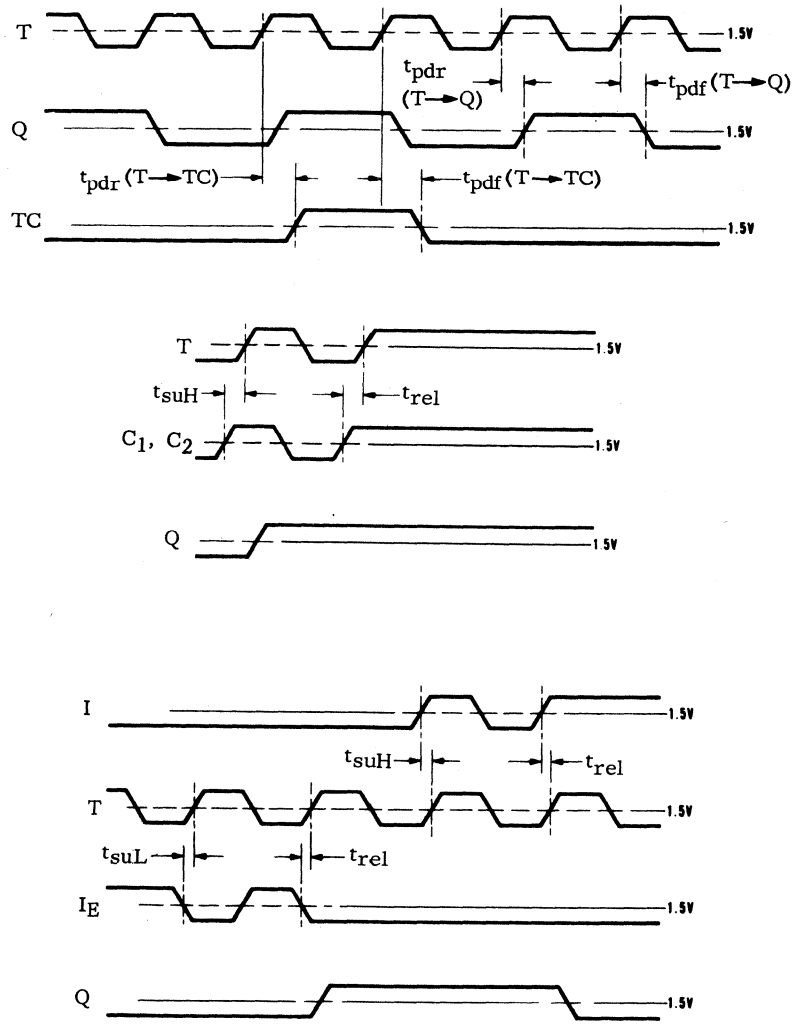
CHARACTERISTICS (continued)

		T_{amb} (°C)				Conditions and references	
		0	25	70		V_P (V)	
DYNAMIC DATA						5.0	C_L = 15 pF
Performance						↓	↓
Rise propagation delay time							
T → Q	t_{pdr} typ.	–	20	–	ns		
T → TC	t_{pdr} typ.	–	35	–	ns		
C_2 → TC	t_{pdr} typ.	–	14	–	ns		
Fall propagation delay time							
T → Q	t_{pdf} typ.	–	15	–	ns		
T → TC	t_{pdf} typ.	–	20	–	ns		
R → Q	t_{pdf} typ	–	33	–	ns		
C_2 → TC	t_{pdf} typ.	–	14	–	ns		
Signal requirements							
Set-up time for:							
I → T	t_{suH} typ.	–	18	–	ns		
C_1, C_2 → T	t_{suH} typ.	–	14	–	ns		
I_E → T	t_{suL} typ.	–	30	–	ns		
Release time for:							
I → T	t_{rel} typ.	–	17	–	ns		
C_1, C_2 → T	t_{rel} typ.	–	12	–	ns		
I_E → T	t_{rel} typ.	–	28	–	ns		

Set-up time : t_{su} is defined as the minimum time required for the logic level to be present at the logic input prior to the trigger (T) transition from LOW to HIGH in order for the flip-flop(s) to respond.

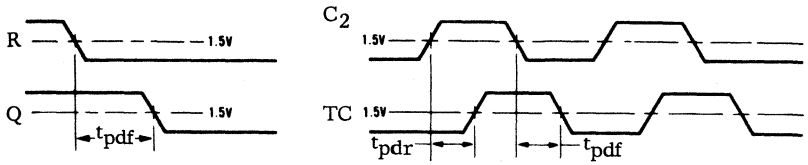
Release time: t_{rel} is defined as the maximum time allowed for the logic level to be present at the logic input prior to the trigger (T) transition from LOW to HIGH in order for the flip-flop(s) not to respond.

CHARACTERISTICS (continued)



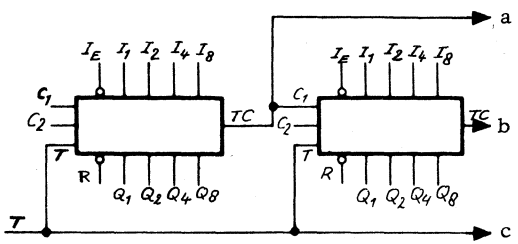
Waveforms illustrating switching times

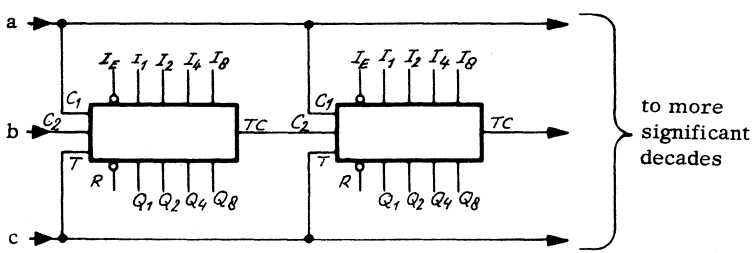
CHARACTERISTICS (continued)



Waveforms illustrating switching times

APPLICATION INFORMATION



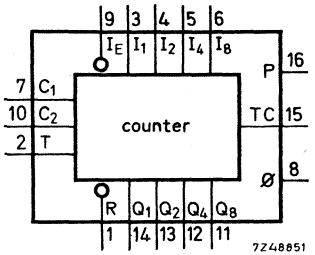


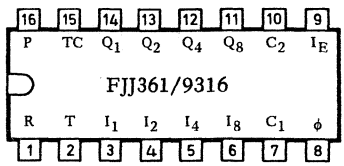
Synchronous counting scheme

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

SINGLE SYNCHRONOUS 4-BIT BINARY COUNTER





QUICK REFERENCE DATA			
Supply voltage	V_P	5.0 ±5%	V
Operating ambient temperature	T_{amb}	0 to +70	°C
Typical operating frequency	f	18	MHz
D.C. noise margin (full temperature range)	M_L	≥ 0.4	V
Total power dissipation	P_{tot}	typ. 300	mW

GENERAL DESCRIPTION

The FJJ361/9316 is a high speed synchronous 4-bit binary up counter. It has a parallel load facility and an overriding asynchronous master reset. By using the internal carry look-ahead counting technique, several stages of synchronous operation are obtainable with no external gating packages and with operating speeds equivalent to those of a single stage.

PACKAGE OUTLINE 16 lead plastic dual in-line (type A) (See General Section).

FUNCTIONAL DESCRIPTION

A clock buffer and inverter drives the four clocked RS master slave flip-flops in parallel, so that synchronous operation is obtained. When the trigger input (T) is LOW, the slave is steady, but data can enter the master via the R and S inputs. During the LOW to HIGH transition of T, first the data inputs (R and S) are inhibited, so that a later change in the input data will not affect the master; secondly, the now trapped information in the master is transferred to the slave and is reflected at the outputs. When the transfer is completed both the master and the slave are steady, as long as T remains HIGH, regardless of the logic state at any other input to the device. During the HIGH to LOW transition of the trigger input (T), first the transfer path from master to slave is inhibited, leaving the slave steady in its present state. Secondly,the data inputs (R and S) are enabled so that new data can enter the master. As a result of this synchronous operation higher clock frequency is possible and much less external logic is required in most applications. Some restrictions are placed on the manner of selection. First, the transition of C_1 or C_2 from HIGH to LOW or of I_E from LOW to HIGH may occur only when T is HIGH. The remaining transition requirements are specified under "Signal requirements" on pages 4, 5 and 6. The asynchronous reset (R) clears the counter independent of all other inputs.

FUNCTION TABLE

Count Enable	$\overline{I_E}$	mode
H	H	Count up
L	H	No change
X	L	Presetting

Count Enable = $C_1 . C_2$

Terminal count TC = $C_2 . Q_1 . Q_2 . Q_4 . Q_8$

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	−0.5 to +7.0	V
Input voltage	All inputs	−0.5 to +5.5	V
Output voltage	V_Q	−0.5 to V_P	V
Storage temperature	T_{stg}	−65 to +150	°C
Operating ambient temperature	T_{amb}	0 to +70	°C

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references	
		0	25	70		V_P (V)	
STATIC DATA							
Voltages							
Input threshold LOW (any input)	V_{IL} max.	0.8	0.8	0.8	V		
Input threshold HIGH (any input)	V_{IH} min.	2.0	2.0	2.0	V		
Output LOW	V_{QL} max.	0.4	0.4	0.4	V	5.25	$I_{QL} = I_{QLmax}$
	V_{QL} max.	0.4	0.4	0.4	V	4.75	$I_{QL} = I_{QLmax}$
Output HIGH	V_{QH} min.	2.4	2.4	2.4	V	4.75	$-I_{QH} = -I_{QHmax}$
Currents							
Input LOW:							
R; C_1	$-I_{IL}$ max.	1.6	1.6	1.6	mA	5.25	$V_I = V_{QL}$ max.
T; I_E; C_2	$-I_{IL}$ max.	3.2	3.2	3.2	mA	5.25	
I_1; I_2; I_4; I_8	$-I_{IL}$ max.	1.07	1.07	1.07	mA	5.25	
Input HIGH:							
R; C_1	I_{IH} max.	60	60	60	µA	5.25	V_I = 4.5 V
T; I_E; C_2	I_{IH} max.	120	120	120	µA	5.25	
I_1; I_2; I_4; I_8	I_{IH} max.	40	40	40	µA	5.25	
Output LOW	I_{QL} max.	9.6	9.6	9.6	µA	5.25	
	I_{QL} max.	8.5	8.5	8.5	µA	4.75	
Output HIGH	I_{QH} max.	360	360	360	µA	4.75	

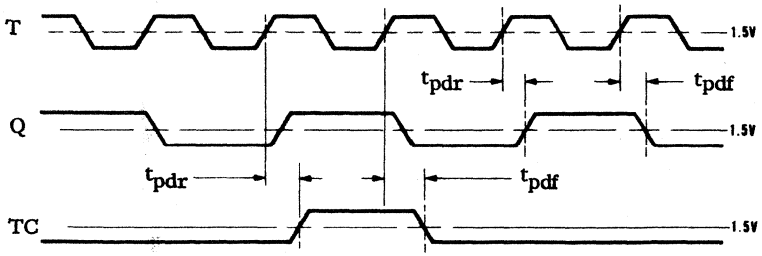
CHARACTERISTICS (continued)

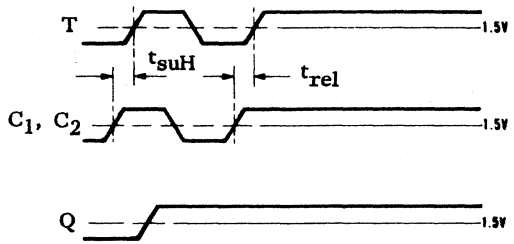
		T_{amb} (°C)				Conditions and References	
		0	25	70		V_P (V)	
DYNAMIC DATA						5.0	C_L = 15 pF
Performance						↓	↓
Rise propagation delay time							
T→Q	t_{pdr} typ.	–	20	–	ns		
T→TC	t_{pdr} typ.	–	35	–	ns		
C_2→TC	t_{pdr} typ.	–	14	–	ns		
Fall propagation delay time							
T→Q	t_{pdf} typ.	–	15	–	ns		
T→TC	t_{pdf} typ.	–	20	–	ns		
R→Q	t_{pdf} typ.	–	33	–	ns		
C_2→TC	t_{pdf} typ.	–	14	–	ns		
Signal requirements							
Set-up time for:							
I→T	t_{suH} typ.	–	18	–	ns		
C_1, C_2→T	t_{suH} typ.	–	14	–	ns		
I_E→T	t_{suL} typ.	–	30	–	ns		
Release time for:							
I→T	t_{rel} typ.	–	17	–	ns		
C_1, C_2→T	t_{rel} typ.	–	12	–	ns		
I_E→T	t_{rel} typ.	–	28	–	ns		

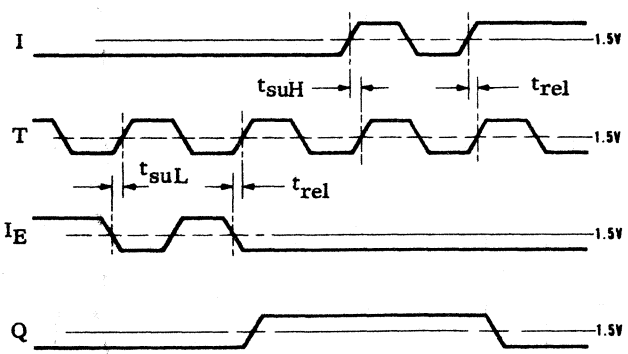
Set-up time : t_{su} is defined as the minimum time required for the logic level to be present at the logic input prior to the trigger (T) transition from LOW to HIGH in order for the flip-flop(s) to respond.

Release time: t_{rel} is defined as the maximum time allowed for the logic level to be present at the logic input prior to the trigger (T) transition from LOW to HIGH in order for the flip-flop(s) not to respond.

CHARACTERISTICS (continued)

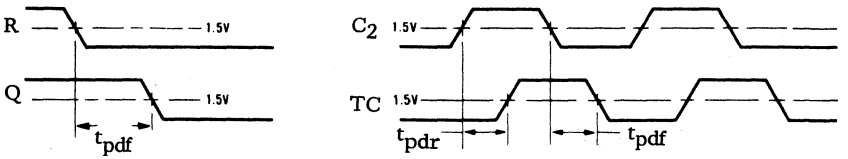






Waveforms illustrating switching times

CHARACTERISTICS (continued)

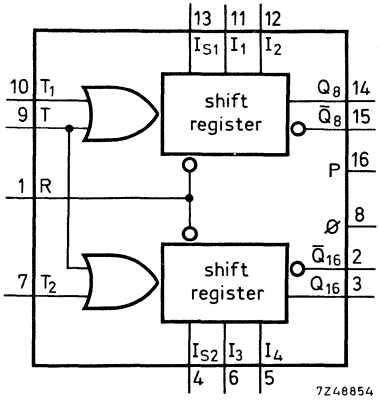


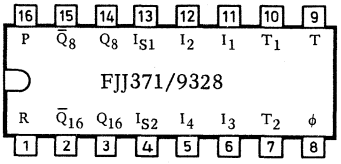
Waveforms illustrating switching times

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

DUAL 8-BIT SHIFT REGISTER





QUICK REFERENCE DATA			
Supply voltage	V_P	5.0 ± 5%	V
Operating ambient temperature	T_{amb}	0 to +70	°C
Typical operating frequency	f	20	MHz
D.C. noise margin (full temperature range)	M_L	≥ 0.4	V
Total power dissipation	P_{tot}	typ. 300	mW

PACKAGE OUTLINE 16 lead plastic dual in-line (type A) (See Genearl Section).

GENERAL DESCRIPTION

The FJJ371/9328 is a high speed serial storage element providing sixteen bits of storage in the form of two eight-bit registers that will shift at rates greater than 20 MHz. The multi-functional capability of this device is provided by several features.

1. Additional gating is provided at the input to both shift registers so that the input is easily multiplexed between two sources.
2. The trigger of each register may be provided separately or together.
3. Complementary outputs are provided from each eight bit register, and both registers may be master cleared from a common input.

FUNCTIONAL DESCRIPTION

The FJJ311/9328 contains two 8-bit shift registers, having both a common trigger input (T) and separate trigger inputs (T_1 and T_2). The triggering (or clocking) of each register is controlled by the OR-function of the separate and common clock input. Each register is composed of eight clocked RS master-slave flip-flops and a number of gates. The clock OR-gate drives the eight trigger inputs of the flip-flops in parallel. When the two clock inputs (the separate and the common) to the OR-gate are LOW, the slave latches are steady, but data can enter the master latches via the R and I_S inputs. During the first LOW to HIGH transition of either, or both simultaneously, of the two trigger inputs, the data inputs (R and I_S) are inhibited so that a later change in input data will not affect the master. The trapped information in the master is now transferred to the slave. When the transfer is complete, both the master and the slave are steady as long as either or both trigger inputs remain HIGH. During the HIGH to LOW transition of the last remaining HIGH trigger input, the transfer path from master to slave is inhibited first, leaving the slave steady in its present state; secondly the data inputs (R and I_S) are enabled so that new data can enter the master. Either of the trigger inputs can be used as "trigger inhibit" inputs by applying a HIGH signal. Each 8-bit shift register has a two-input multiplexer in front of the serial data input. The two data inputs (I_1 and I_2) are controlled by the data select input (I_S) following the Boolean expression:

$$\text{Serial data in} = \overline{I_{S1}} \cdot I_1 + I_{S1} \cdot I_2 \ ^{1)}$$

An asynchronous master reset (R) is provided which, when activated by a LOW logic level, will clear all sixteen stages independently of any other input signal.

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1) For I_3 and I_4: $\overline{I_{S2}} \cdot I_3 + I_{S2} \cdot I_4$

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134).

Supply voltage	V_P	−0.5 to +7.0	V
Input voltage	All inputs	−0.5 to +5.5	V
Ouput voltage (HIGH state)	V_Q	−0.5 to V_P	V
Storage temperature	T_{stg}	−65 to +150	°C
Operating ambient temperature	T_{amb}	0 to +70	°C

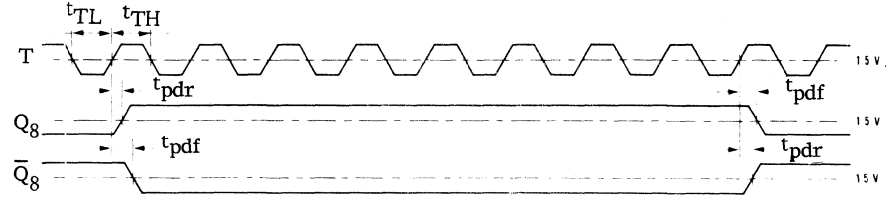
CHARACTERISTICS

		T_{amb} (°C)				Conditions and references	
		0	25	70		V_P (V)	
STATIC DATA							
Voltages							
Input threshold LOW (any input)	V_{IL} max.	0.8	0.8	0.8	V		
Input threshold HIGH (any input)	V_{IH} min.	2.0	2.0	2.0	V		
Output LOW	V_{QL} max.	0.4	0.4	0.4	V	5.25 4.75	$I_{QL} = I_{QLmax}$
Output HIGH	V_{QH} min.	2.4	2.4	2.4	V	4.75	$-I_{QH} = -I_{QHmax}$
Currents							
Input LOW:							
I_1; I_2; I_3; I_4; R	$-I_{IL}$ max.	1.6	1.6	1.6	mA	5.25	$V_I = V_{QL}$ max.
I_{S1} ; I_{S2}	$-I_{ISL}$ max.	3.2	3.2	3.2	mA	5.25	$V_{IS} = V_{QL}$ max.
T_1; T_2	$-I_{TL}$ max.	2.4	2.4	2.4	mA	5.25	$V_{IT} = V_{QL}$ max.
T	$-I_{TL}$ max.	4.8	4.8	4.8	mA	5.25	$V_{IT} = V_{QL}$ max.
Input HIGH:							
I_1; I_2; I_3; I_4; R	I_{IH} max.	60	60	60	µA	5.25	$V_I = 4.5$ V
I_{S1} ; I_{S2}	I_{ISH} max.	120	120	120	µA	5.25	$V_{IS} = 4.5$ V
T_1; T_2	I_{TH} max.	90	90	90	µA	5.25	$V_{IT} = 4.5$ V
T	I_{TH} max.	180	180	180	µA	5.25	$V_{IT} = 4.5$ V
Output LOW	I_{QL} max.	9.6	9.6	9.6	mA	5.25	$V_Q = V_{QLmax}$
	I_{QL} max.	8.5	8.5	8.5	mA	4.75	$V_Q = V_{QLmax}$
Output HIGH	$-I_{QH}$ max.	360	360	360	µA	5.25	$V_{QH} = V_{QHmin}$
SUPPLY DATA							
Supply current	$I_P \leq$	73	73	73	mA	5.0	
	I_P typ.	-	60	-	mA	5.0	

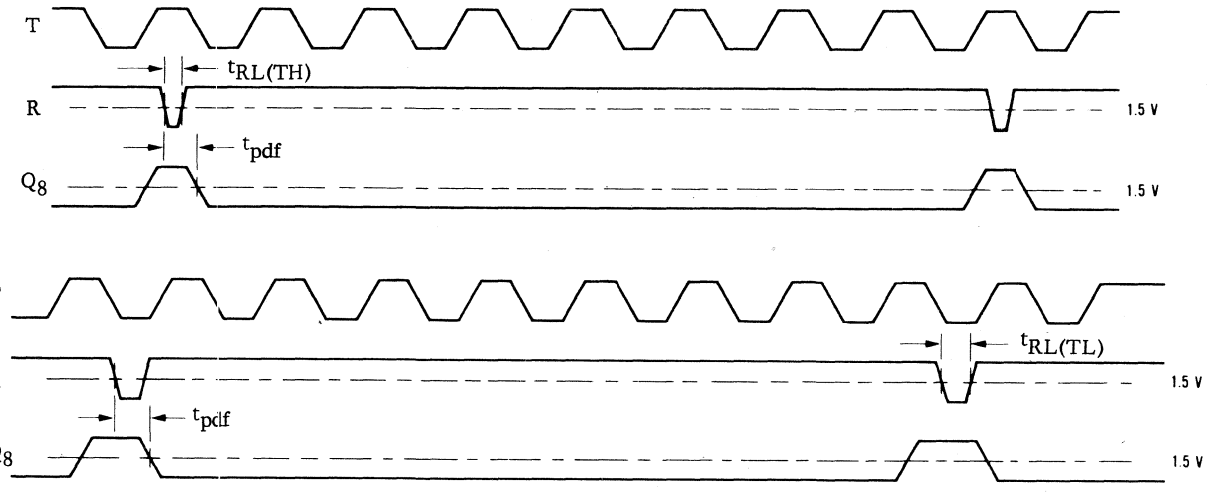
CHARACTERISTICS (continued)

		T_{amb} (°C)				Conditions and references	
		0	25	70		V_P (V)	
DYNAMIC DATA							
Performance							
Rise propagation delay time							
T → Q_8 (Q_{16}) or Q_8 (Q_{16}) inverted	t_{pdr} typ.	–	13	–	ns	5.0	C_L = 15 pF
Fall propagation delay time							
T → Q_8 (Q_{16}) or Q_8 (Q_{16}) inverted	t_{pdf} typ.	–	22	–	ns	5.0	C_L = 15 pF
R → Q_8 (Q_{16})	t_{pdf} typ.	–	35	–	ns	5.0	C_L = 15 pF
Signal requirements							
Pulse width for:							
T	t_{TH}; $t_{TL} \geq$	–	14	–	ns	5.0	C_L = 15 pF
R (trigger HIGH)	$t_{RL(TH)} \geq$	–	15	–	ns	5.0	C_L = 15 pF
R (trigger LOW)	$t_{RL(TL)} \geq$	–	28	–	ns	5.0	C_L = 15 pF

CHARACTERISTICS (continued)



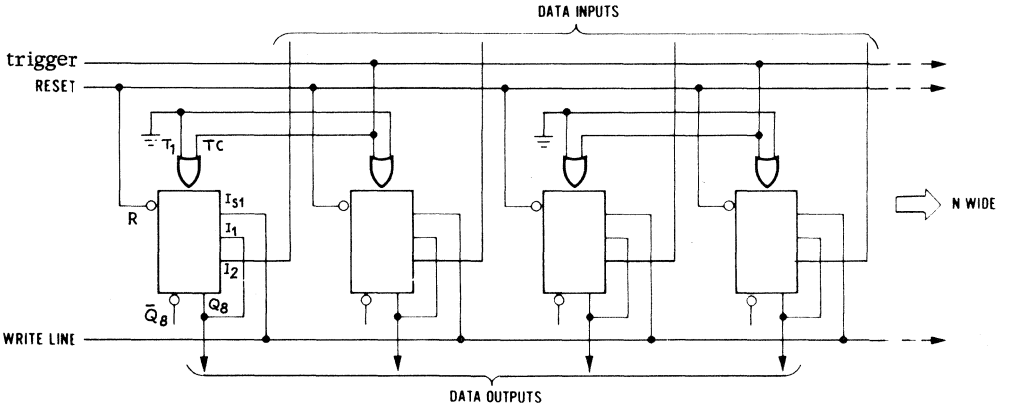
Test conditions: $\bar{Q}_8$ connected to I_2; $T_1 = \phi$



Test conditions: $I_{S1} = I_{\cdot\cdot} = I_2$ = HIGH; $T_1 = \phi$

Waveforms illustrating switching times

APPLICATION INFORMATION

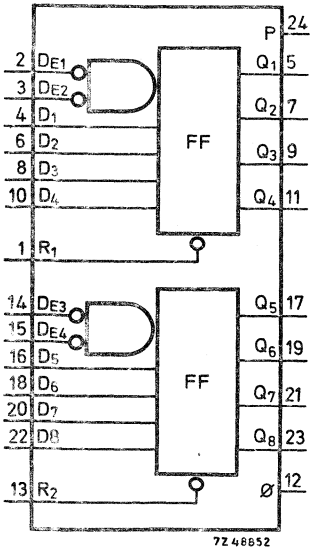


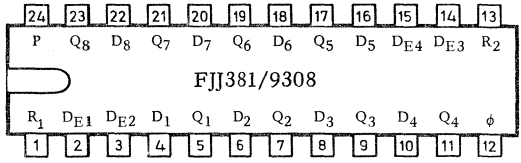
N-bit by 8-word high speed serial memory

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

DUAL QUADRUPLE LATCH D FLIP-FLOP





QUICK REFERENCE DATA			
Supply voltage	V_P	5.0 ± 5%	V
Operating ambient temperature	T_{amb}	0 to +70	°C
Propagation delay D_E to Q	t_{pd}	typ. 18	ns
D to Q	t_{pd}	typ. 15	ns
D.C. noise margin (full temperature range)	M_L	≥ 0.4	V

PACKAGE OUTLINE 24 lead ceramic dual in-line (See General Section).

GENERAL DESCRIPTION

The FJJ381/9308 is a dual quadruple D flip-flop designed for general purpose storage applications in high speed digital systems. All outputs have active pull-up circuitry to provide high capacitive drive and low impedance outputs in both logic states to provide good a.c. noise immunity.
Its features include: active level LOW enable gate inputs; overriding reset (R); propagation delay of 19 ns.

FUNCTIONAL DESCRIPTION

Data can be entered into the latch when both of the enable inputs are LOW. As long as this logic condition exists the output of the latch will follow the input. If either of the enable inputs goes HIGH, the data present in the latch at that time is held in the latch and is no longer affected by the data input.
The reset (R) overrides all other input conditions and forces the outputs of all the latch flip-flops LOW when a LOW signal is applied to the reset (R) input.

FUNCTION TABLE

inputs			outputs
D_{E1}; D_{E3}	D_{E2}; D_{E4}	D	
H	X	X	*
X	H	X	*
L	L	L	L
L	L	H	H

*) State is the same as prior to DE_1; DE_2

H=HIGH state (the more positive voltage)
L=LOW state (the less positive voltage)
X=state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	-0.5 to +7.0	V
Input voltage [1])	All inputs	-0.5 to +5.5	V
Input current [1])	All inputs	-30 to +5	mA
Output voltage (HIGH state)	V_Q	-0.5 to V_P	V
Output current (LOW state)	I_Q	+30	mA
Storage temperature	T_{stg}	-65 to +150	°C
Operating ambient temperature	T_{amb}	0 to +70	°C

[1]) Either input voltage or input current limit is sufficient to protect the inputs.

CHARACTERISTICS

		T_{amb} (°C)				Conditions and References	
		0	25	70		V_P (V)	
STATIC DATA							
Voltages							
Input threshold LOW (any input)	V_{ILmax}	0.8	0.8	0.8	V		
Input threshold HIGH (any input)	V_{IHmax}	2.0	2.0	2.0	V		
Output LOW	V_{QLmax}	0.4	0.4	0.4	V	5.25	$I_Q = I_{QLmax}$ [1]
	V_{QLmax}	0.4	0.4	0.4	V	4.75	$I_Q = I_{QLmax}$ [1]
Output HIGH	V_{QHmin}	2.4	2.4	2.4	V	4.75	$-I_{QH} = -I_{QHmax}$ [1]
Currents							
Input LOW:							
D_{E1};D_{E2}(D_{E3};D_{E4})	$-I_{DELmax}$	1.6	1.6	1.6	mA	5.25	$V_I = V_{QLmax}$
R_1;R_2	$-I_{RLmax}$	1.6	1.6	1.6	mA	5.25	$V_I = V_{QLmax}$
D (any input)	$-I_{DLmax}$	2.7	2.6	2.7	mA	5.25	V_D=0 V [2]
Input HIGH							
D_{E1};D_{E2}(D_{E3};D_{E4})	I_{DEHmax}	–	60	60	µA	5.25	V_{DE}=4.5 V
R_1;R_2	I_{RHmax}	–	60	60	µA	5.25	V_R =4.5 V
D (any input)	I_{DHmax}	–	90	90	µA	5.25	V_D =4.5 V
Output LOW	I_{QLmax}	14.4	14.4	14.4	mA	5.25	
		12.7	12.7	12.7	mA	4.75	
Output HIGH	$-I_{QHmax}$	600	600	600	µA	5.25	
SUPPLY DATA							
Supply current (total value)	I_{Pmax}	117	117	117	mA	5.0	All outputs LOW; inputs disabled
	I_{Ptyp}	–	65	–	mA	5.0	All outputs LOW; inputs disabled

[1] **Inputs at threshold** voltages (LOW or HIGH). Output voltages are guaranteed for either the input **enabled** or input disabled case.

[2] This current is measured at V_D= 0 V to ensure that no current is being absorbed by the device internally. The maximum value given guarantees that the maximum instantaneous current that can flow out of the input **at** V_D = 0.4 V is 2.4 mA.

CHARACTERISTICS (continued)

		T_{amb} (°C)				Conditions and References	
		0	25	70		V_P (V)	
DYNAMIC DATA							
Performance							
Rise propagation delay times							
$D_{E1} \rightarrow Q$ [1]	t_{pdr}	typ.	– 22	–	ns	5.0	C_L = 15 pF
$D_{E3} \rightarrow Q$ [2]	t_{pdr}	typ.	– 22	–	ns	5.0	C_L = 15 pF
Fall propagation delay times							
$D_{E1} \rightarrow Q$ [1]	t_{pdf}	typ.	– 15	–	ns	5.0	C_L = 15 pF
$D_{E3} \rightarrow Q$ [2]	t_{pdf}	typ.	– 15	–	ns	5.0	C_L = 15 pF
Signal requirements							
Set-up time for:							
$D \rightarrow D_{E1}$ (D_{E3}) [3]	t_{suH}	typ.	– 4	–	ns	5.0	C_L = 15 pF
	t_{suL}	typ.	– 0	–	ns	5.0	C_L = 15 pF
Release time	t_{relL}	typ.	– 5	–	ns	5.0	C_L = 15 pF
$D \rightarrow D_{E1}$(D_{E3}) [3]	t_{relH}	typ.	– 2	–	ns	5.0	C_L = 15 pF
Minimum pulse width for all D_E inputs	t_{DEL}	typ.	– 15	–	ns	5.0	C_L = 15 pF

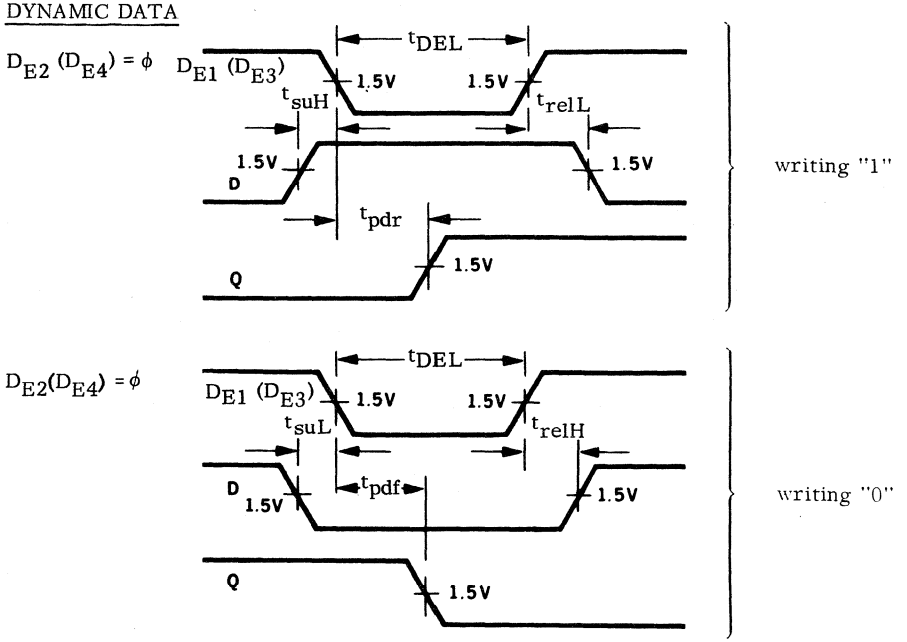
[1] Also when $D_{E2} \rightarrow Q$; $D_{E1} = \phi$

[2] Also when $D_{E4} \rightarrow Q$; $D_{E3} = \phi$

[3] Also when $D \rightarrow D_{E2}(D_{E4})$; $D_{E1} = D_{E3} = \phi$

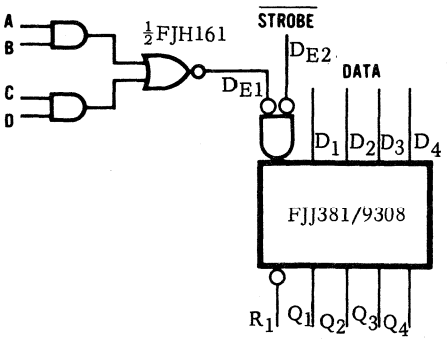
CHARACTERISTICS (continued)

DYNAMIC DATA



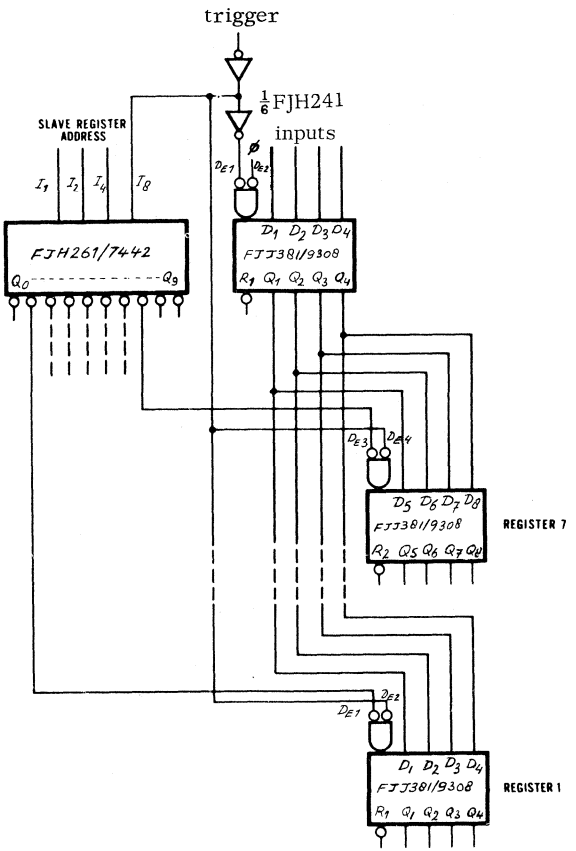
Waveforms illustrating switching times

APPLICATION INFORMATION



AND-OR enable showing active level LOW enable gate utility.

APPLICATION INFORMATION (continued)



Single master/multiple slave flip-flop

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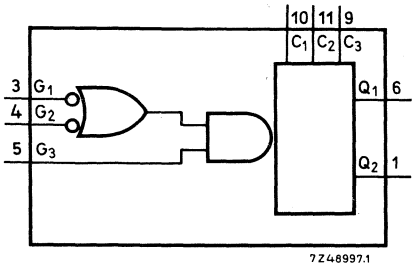
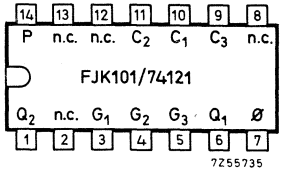
MONOSTABLE MULTIVIBRATOR





QUICK REFERENCE DATA			
Supply voltage	V_P	5.0 ± 5%	V
Operating ambient temperature	T_{amb}	0 to +70	°C
Available fan-out (each output)	N_a	≥ 10	
Average power consumption (50% duty cycle)	P_{av}	typ. 90	mW

PACKAGE OUTLINE 14 lead plastic dual in-line (type A) (See General Section)

The FJK101/74121 monostable multivibrator features D.C. voltage level triggering which is not directly related to the input pulse transition time. The input gating allows the choice of triggering either on the positive or negative-going edge of the input pulse, as well as providing an inhibit facility. Both positive and negative output pulses are available with a full fan-out of 10 and TTL line driving capabilities.
G_1 and G_2 are negative-edge trigger inputs and will trigger the one-shot when either or both go LOW as long as G_3 is HIGH. G_3 is a positive-edge Schmitt-trigger input for slow edges or level detection, and will trigger the one-shot when G_3 goes HIGH as long as G_1 or G_2 are LOW.
Output pulse duration may be varied between 40 ns and 40 s and is determined by the value of external components used (see TIMING NOTES on page 6).

FUNCTION TABLE

inputs						outputs
t_n			t_{n+1}			
G_1	G_2	G_3	G_1	G_2	G_3	
H	H	L	H	H	H	inhibit
L	X	H	L	X	L	"
X	L	H	X	L	L	"
L	X	L	L	X	H	one-shot
X	L	L	X	L	H	"
H	H	H	X	L	H	"
H	H	H	L	X	H	"
X	L	L	X	H	L	inhibit
L	X	L	H	X	L	"
X	L	H	H	H	H	"
L	X	H	H	H	H	"
H	H	L	X	L	L	"
H	H	L	L	X	L	"

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state immaterial

t_n = time before input transition
t_{n+1} = time after input transition

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	7.0	V
D.C. input voltage	V_G	max.	5.5	V [1]
Negative transient input voltage	$-V_{GM}$	max.	2.0	V [2]
Storage temperature	T_{stg}	−65 to	+150	°C
Operating ambient temperature	T_{amb}	0 to	+70	°C

[1] In addition, the voltage between any two inputs must not exceed 5.5 V.
[2] Pulse duration t_p = 20 ns; repetition frequency f = 5 MHz; source resistance $R_S \geq 75\Omega$.

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references	
		0	25	70		V_P (V)	
STATIC DATA							
Voltages							
Input threshold LOW (negative-going)							
any input	V_{GLmin}	0.8	0.8	0.8	V	4.75	
G_1; G_2	V_{GLtyp}	–	1.4	–	V	5.0	
G_3	V_{GLtyp}	–	1.35	–	V	5.0	
Input threshold HIGH (positive-going)							
any input	V_{GHmax}	2.0	2.0	2.0	V	4.75	
G_1; G_2	V_{GHtyp}	–	1.4	–	V	5.0	
G_3	V_{GHtyp}	–	1.55	–	V	5.0	
Output LOW	V_{QLmax}	0.4	0.4	0.4	V	4.75	$I_Q = I_{QLmax}$
	V_{QLtyp}	–	0.22	–	V	5.0	
Output HIGH	V_{QHmin}	2.4	2.4	2.4	V	4.75	$-I_Q = -I_{QHmax}$
	V_{QHtyp}	–	3.3	–	V	5.0	
Currents							
Input LOW							
G_1; G_2	$-I_{GLmax}$	1.6	1.6	1.6	mA	5.25	$V_I = V_{QLmax}$
G_3	$-I_{GLmax}$	3.2	3.2	3.2	mA	5.25	
Input HIGH							
G_1; G_2	I_{GHmax}	40	40	40	µA	5.25	$V_I = V_{QHmin}$
G_3	I_{GHmax}	80	80	80	µA	5.25	
any input	I_{GHmax}	1	1	1	mA	5.25	V_I = 5.5 V
Output LOW	I_{QLmax}	16	16	16	mA		
Output HIGH	$-I_{QHmax}$	0.4	0.4	0.4	mA		
Output short-circuit [1])	$-I_{Qsc\ min}$	18	18	18	mA	5.25	
	$-I_{Qsc\ max}$	55	55	55	mA	5.25	
SUPPLY DATA							
Supply current							
quiescent (unfired)	I_P typ.	–	13	–	mA	5.0	
	I_P <	25	25	25	mA	5.25	
fired	I_P typ.	–	23	–	mA	5.0	
	I_P <	40	40	40	mA	5.25	

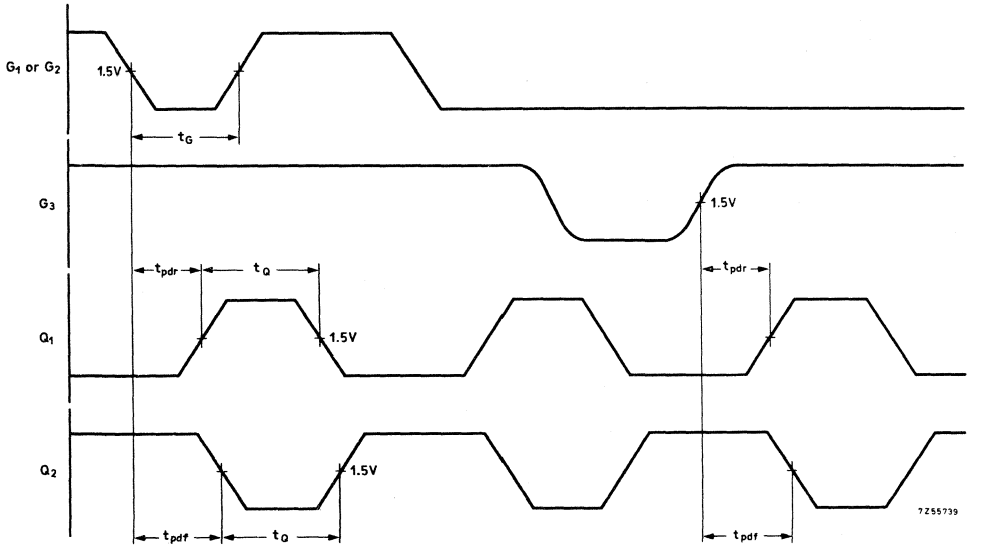
[1]) Only one output to be shorted at a time.

CHARACTERISTICS (continued)

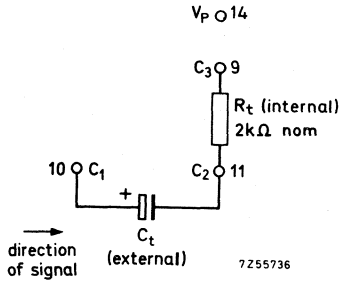
		T_{amb} (°C)			Conditions and references	
		0	25	70	V_P (V)	C_L = 15 pF; N_a = 10
DYNAMIC DATA						
Signal requirements						
Input pulse width	t_G >	–	50	– ns		
Input pulse rise/fall time						
G_1; G_2	$\frac{dV_G}{dt}$ <	–	1	– V/µs		
G_3	$\frac{dV_G}{dt}$ <	–	1	– V/s		
Performance						
Rise propagation delay time						
G_1, G_2 → Q_1	t_{pdr} >	–	25	– ns	5.0	C_t = 80 pF
	t_{pdr} typ.	–	45	– ns	5.0	
	t_{pdr} <	–	70	– ns	5.0	
G_3 → Q_1	t_{pdr} >	–	15	– ns	5.0	
	t_{pdr} typ.	–	35	– ns	5.0	
	t_{pdr} <	–	55	– ns	5.0	
Fall propagation delay time						
G_1, G_2 → Q_2	t_{pdf} >	–	30	– ns	5.0	
	t_{pdf} typ.	–	50	– ns	5.0	
	t_{pdf} <	–	80	– ns	5.0	
G_3 → Q_2	t_{pdf} >	–	20	– ns	5.0	
	t_{pdf} typ.	–	40	– ns	5.0	
	t_{pdf} <	–	65	– ns	5.0	
Output pulse width:						
with internal timing resistance	t_Q >	–	70	– ns	5.0	C_t = 80pF; R_t=open; pin C_3 connected to 5.0 V
	t_Q typ.	–	110	– ns	5.0	
	t_Q <	–	150	– ns	5.0	
with zero timing capacitance	t_Q >	–	20	– ns	5.0	C_t = 0; R_t = open; pin C_3 connected to 5.0 V
	t_Q typ.	–	30	– ns	5.0	
	t_Q <	–	50	– ns	5.0	
with external timing resistance	t_Q >	–	600	– ns	5.0	C_t = 100 pF; R_t = 10 KΩ; pin C_3 open
	t_Q typ.	–	700	– ns	5.0	
	t_Q <	–	800	– ns	5.0	
	t_Q >	–	6	– ms	5.0	C_t = 1 µF; R_t = 10 KΩ; pin C_3 open
	t_Q typ.	–	7	– ms	5.0	
	t_Q <	–	8	– ms	5.0	

CHARACTERISTICS (continued)

DYNAMIC DATA

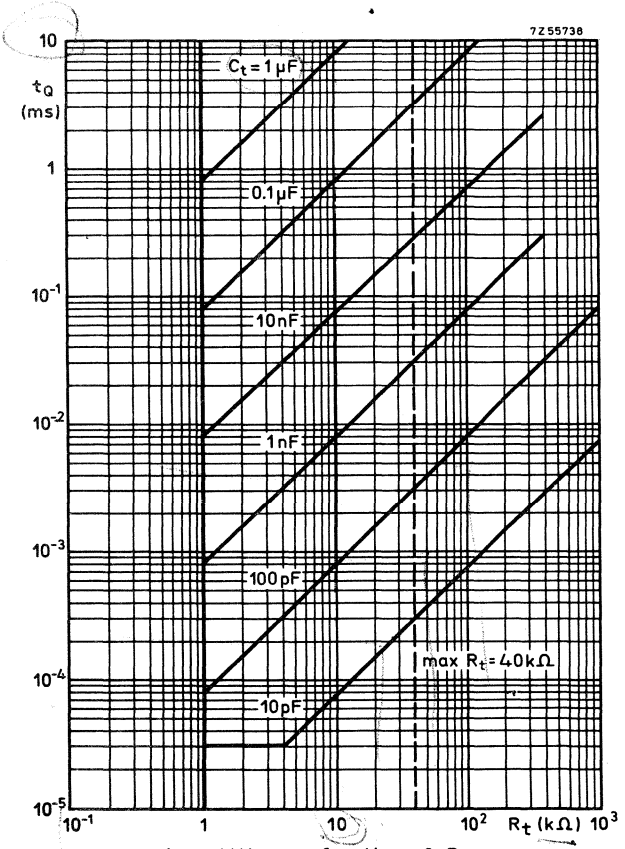


CHARACTERISTICS (continued)
TIMING NOTES



1. An external timing capacitor may be connected between C_1 (pin 10 - positive) and C_2 (pin 11 - negative). Without an external capacitor the output pulse width is typically 30 ns.
2. An internal timing resistor is incorporated between C_3 (pin 9) and C_2 (pin 11) and has a nominal value of 2 kΩ. It may be brought into the circuit by connecting C_3 to V_P (pin 14).
3. For variable pulse widths an external variable resistor should be connected between C_3 and V_P; no external limiting is then required.
4. For accurate repeatable pulse widths connect an external resistor between point C_2 and V_P, leaving point C_3 open.
5. Jitter-free operation is maintained over the full temperature and supply voltage range for timing capacitances from 10 pF to 10 µF and timing resistances from 2 kΩ to 40 kΩ.
   Within these limits the output pulse width follows the relationship $t_Q = C_t.R_t \ell nZ$.
6. A duty cycle of up to 67 % is achieved by using only the internal timing resistance. Duty cycles as high as 90 % are obtained by using R_t = 40 kΩ. Higher duty cycles are achievable if a certain amount of pulse-width jitter is allowed.

CHARACTERISTICS (continued)

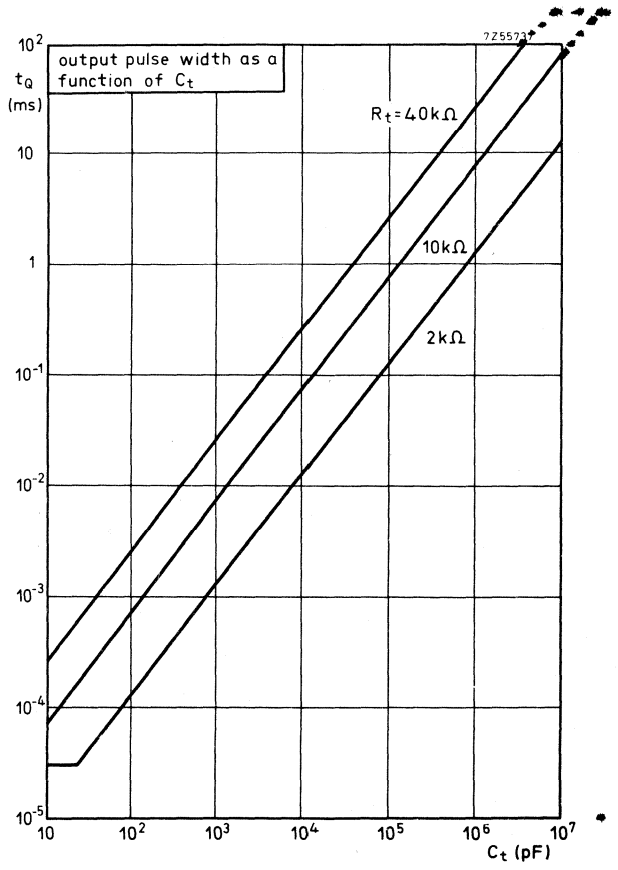


output pulse width as a function of R_t

$$f = \frac{1}{T}$$

$$50\,Hz = 20\,ms$$

CHARACTERISTICS (continued)



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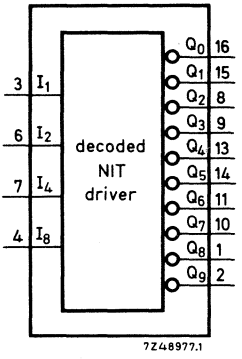
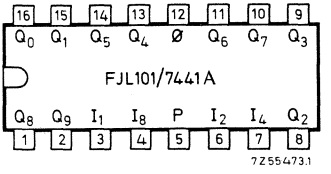
Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

SINGLE DECODER N.I.T. DRIVER [1])





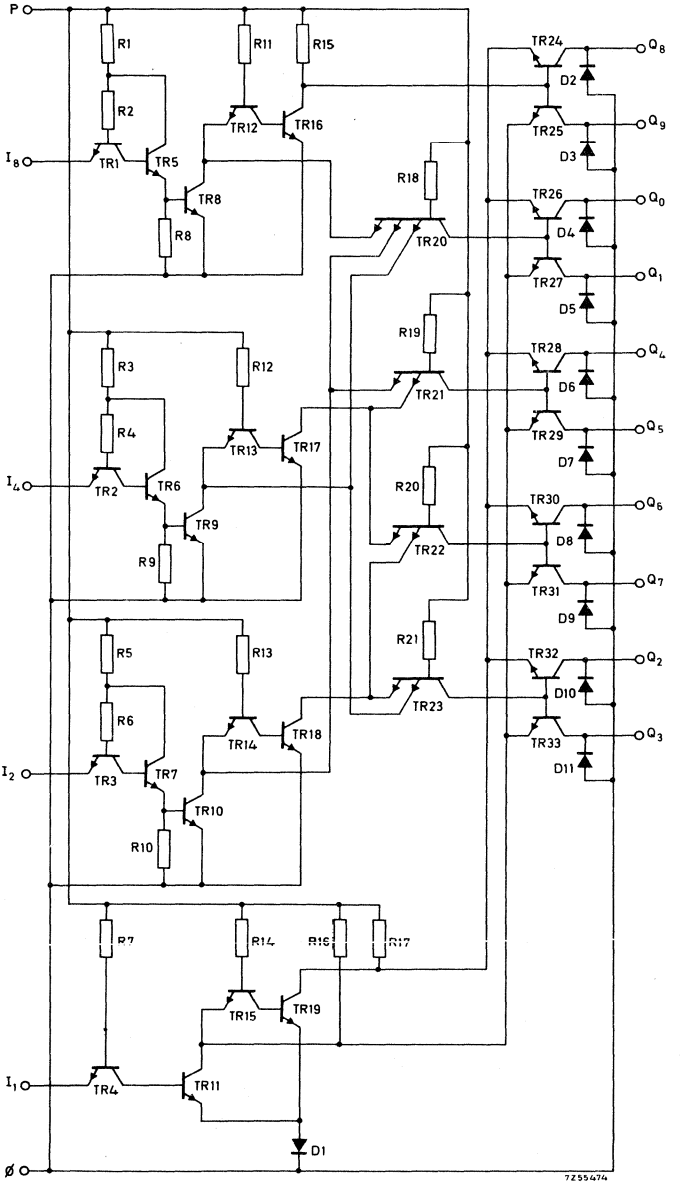
QUICK REFERENCE DATA			
Supply voltage	V_P	5.0 ± 5%	V
Operating ambient temperature	T_{amb}	0 to +70	°C
Supply current	I_P	typ. 19	mA
Drive lines		10	
Output voltage at any output	V_Q	> 55	V

The FJL101/7441A is a BCD (1-2-4-8 code) to decimal decoder incorporating high voltage output transistors for driving numerical indicator tubes. It contains a decoding array followed by ten output driver stages which can be used for parallel or serial drive. For parallel drive no external clamping diodes are needed. For serial drive the cathode voltages must be clamped to prevent excessive dissipation that may be caused by the leakage currents of non-ignited cathodes are cut-off.

PACKAGE OUTLINE: 16 lead plastic dual in-line (type A) (See General Section)

[1]) N.I.T.; Numerical Indicator Tube.

CIRCUIT DIAGRAM



FUNCTION TABLE

inputs				output
I_1	I_2	I_4	I_8	ON-state *)
L	L	L	L	0
H	L	L	L	1
L	H	L	L	2
H	H	L	L	3
L	L	H	L	4
H	L	H	L	5
L	H	H	L	6
H	H	H	L	7
L	L	L	H	8
H	L	L	H	9

*) All other outputs are off.

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	7.0	V
Input voltage	V_I	max.	5.5	V
Current into any output (OFF state)	I_Q	max.	0.5	mA
Operating ambient temperature	T_{amb}	0 to	+70	°C
Storage temperature	T_{stg}	−65 to	+150	°C

CHARACTERISTICS

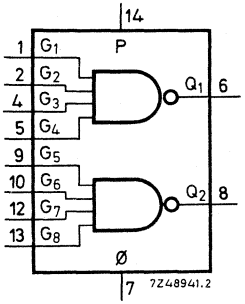
		T_{amb} (°C) 0	25	70	Conditions and References V_P (V)	
STATIC DATA						
Voltages						
Input threshold LOW [1])	V_{ILmax}	0.8	0.8	0.8 V	4.75	
Input threshold HIGH [1])	V_{IHmin}	2.0	2.0	2.0 V	4.75	
Output LOW (ON-state) [1])	V_{QLmax}	2.5	2.5	2.5 V	4.75	I_{QL} = 7 mA; V_{IL} = 0.8 V; V_{IH} = 2.0 V
Currents						
Input LOW I_1	$-I_{I1Lmax}$	3.2	3.2	3.2 mA	5.25	V_{IL} = 0.4 V
I_2, I_4, I_8	$-I_{I2Lmax}$, $-I_{I4Lmax}$, $-I_{I8Lmax}$	1.6	1.6	1.6 mA	5.25	V_{IL} = 0.4 V
Input HIGH I_1	I_{I1Hmax}	80	80	80 µA	5.25	V_{IH} = 2.4 V
	I_{I1Hmax}	1	1	1 mA	5.25	V_{IH} = 5.5 V
I_2, I_4, I_8	I_{I2Hmax}, I_{I4Hmax}, I_{I8Hmax}	40	40	40 µA	5.25	V_{IH} = 2.4 V
I_2, I_4, I_8	I_{I2Hmax}, I_{I4Hmax}, I_{I8Hmax}	1	1	1 mA	5.25	V_{IH} = 5.5 V
Output leakage current HIGH (OFF-state) [1])	$-I_{QHmax}$	200	200	200 µA	5.25	V_Q = 55 V, V_{IL} = V_{ILmax}; V_{IH} = V_{IHmax}
SUPPLY DATA						
Supply current	I_P typ	-	21	- mA	5.0	All inputs and outputs open
	I_P <	42	42	42 mA	5.25	

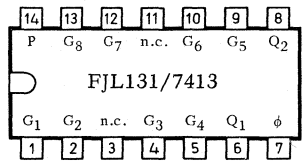
[1]) See function table on page 3. V_{IL} and V_{IH} to be maintained as in function table.

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

DUAL 4-INPUT SCHMITT TRIGGER
positive NAND gate



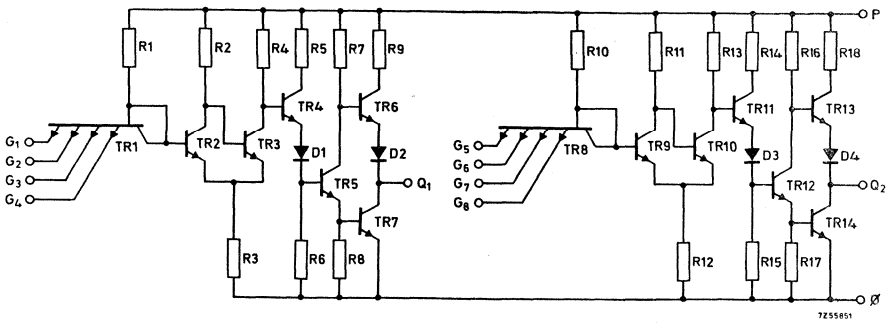


QUICK REFERENCE DATA				
Supply voltage	V_P		5.0 ±5%	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Available d.c. fan-out (full temperature range)	N_a	≥	10	
Hysteresis	ΔV_G	typ.	800	mV
Propagation delay time	t_{pd}	typ.	17	ns
Average power consumption (50 % duty cycle: T_{amb} = 25 °C)	P_{av}	typ.	85	mW

An important design feature is the built-in temperature compensation which ensures very high stability of the threshold levels and the hysteresis over a very wide temperature range. Typically the hysteresis is virtually unchanged over the range 0 to 70 °C. The Schmitt will trigger from very low input ramps producing a very stable output signal. It can also be triggered from d.c. levels.

PACKAGE OUTLINE 14 lead plastic dual in-line (type A) (See General Section).

CIRCUIT DIAGRAM



LOGIC FUNCTION

Each circuit functions as a four-input NAND gate but, because of the SCHMITT action, the gate has different input threshold levels for positive and negative-going signals. The Hysteresis or backlash which is the difference between the two threshold levels is typically 800 mV.

Individual gate operation

Function table (For two input terminals)

A	B	C
L	L	H
H	L	H
L	H	H
H	H	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
$C = \overline{A.B.}$ (positive logic)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134).

Supply voltage	V_P	max.	7.0	V
Output voltage	V_Q	max.	5.5	V
G-input voltage	V_G	max.	5.5	V [1]
Peak negative G-input voltage	$-V_{GM}$	max.	2.0	V [2]
D.C. voltage applied to the outputs ($R_L \geq 270\ \Omega$)		max.	7.0	V
Storage temperature	T_{stg}		−55 to +150	°C
Operating ambient temperature	T_{amb}		0 to +70	°C

[1]) In addition, the voltage between any two inputs must not exceed 5.5 V.
[2]) Pulse duration t_p = 20 ns; repetition frequency f = 5 MHz; source resistance $R_S \geq 75\ \Omega$.

CHARACTERISTICS

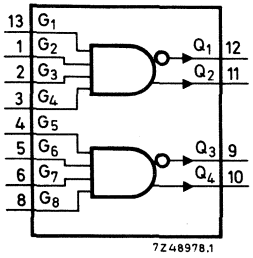
		T_{amb} (°C)			Conditions and references	
		0	25	70 V	V_P (V)	
STATIC DATA						
Voltages						
Input threshold positive going	V_{Gmin}	1.5	1.5	1.5 V	5.0	
Input threshold negative going	V_{Gmax}	1.1	1.1	1.1 V	5.0	
Input threshold hysteresis	ΔV_{Gmin}	0.4	0.4	0.4 V	5.0	
Output LOW	V_{QLmax}	0.4	0.4	0.4 V	4.75	$I_Q = I_{QLmax}$; $V_G = V_{GHmin}$
Output HIGH	V_{QHmin}	2.4	2.4	2.4 V	4.75	$-I_Q = -I_{QHmax}$; $V_G = V_{GLmax}$
Currents						
Input current at upper threshold	$-I_{GL1}$ typ.	0.65	0.65	0.65 mA	5.0	
Input current at lower threshold	$-I_{GL2}$ typ.	0.85	0.85	0.85 mA	5.0	
Input LOW (note 1)	$-I_{GLmax}$	1.6	1.6	1.6 mA	5.25	$V_G = V_{QLmax}$; $I_Q = 0$
Input HIGH (note 2)	I_{GHmax}	40	40	40 µA	5.25	$V_G = V_{QHmin}$; $I_Q = 0$; other inputs = 0 V
Output LOW	I_{QLmax}	16	16	16 mA		
Output HIGH	$-I_{QHmax}$	0.8	0.8	0.8 mA		
Output short-circuited (note 3)	$-I_{Qsc\ min}$	18	18	18 mA	5.25	$V_Q = 0$; $V_G = 0$
	$-I_{Qsc\ max}$	55	55	55 mA	5.25	$V_Q = 0$; $V_G = 0$
SUPPLY DATA						
Supply current						
Output LOW	I_{PL} typ.	-	20	- mA	5.0	$V_G = 5.0$ V; $I_Q = 0$
	I_{PL} <	36	36	36 mA	5.25	$V_G = 5.0$ V; $I_Q = 0$
Output HIGH	I_{PH} typ.	-	14	- mA	5.0	$V_G = 0$; $I_Q = 0$
	I_{PH} <	28	28	28 mA	5.25	$V_G = 0$; $I_Q = 0$
DYNAMIC DATA						
Rise propagation delay time	t_{pdr} typ.	-	18	- ns	5.0	N = 10; C_L = 15 pF; R_L = 400 Ω
	t_{pdr} <	-	30	- ns	5.0	
Fall propagation delay time	t_{pdf} typ.	-	15	- ns	5.0	
	t_{pdf} <	-	30	- ns	5.0	

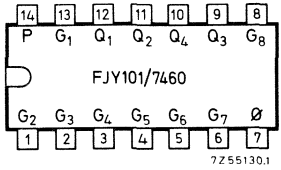
Note 1 The LOW state normally corresponds to a voltage level between 0 and 0.4 V.
2 The HIGH state normally corresponds to a voltage level between 2.4 V and 5.25 V.
3 Not more than one output must be short-circuited at any time.

The FJ family of TTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and control.

Features of the FJ family: * high-fan-out * low power consumption (typ. 10 mW for standard gates) * high logic swing * low output impedance * short circuit protection * high capacitance drive capability * high noise margin (typ. 1.0 V for standard gates) * comprehensive range of circuits, including NAND gates, AND-OR-NOT gates, gate expanders, flip-flops and complex-function devices.

DUAL 4-INPUT AND-OR-NOT EXPANDER





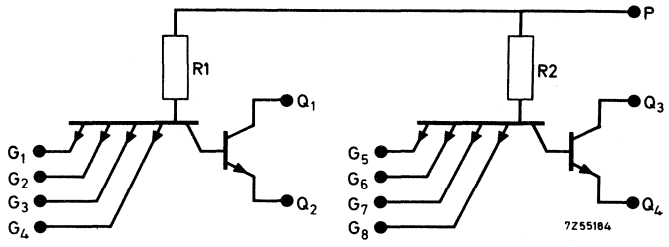
QUICK REFERENCE DATA			
Supply voltage	V_P	5.0 ± 5%	V
Operating ambient temperature range	T_{amb}	0 to + 70	°C
Average propagation delay time when used with FJH151 or FJH171 N = fan-out = 10; T_{amb} = 25 °C	t_{pd}	typ. 15	ns
D.C. noise margin [1]) (full temperature range)	M_L	> 0.4 typ. 1.0	V V
Average power consumption; (each expander) T_{amb} = 25 °C	P_{av}	typ. 4.0	mW

The FJY101/7460 is a dual 4-input AND-OR-NOT expander for use with the FJH151/7450 and FJH171/7453. Up to 4 expanders may be connected to the expandable gates of FJH151/7450 and FJH171/7453.

PACKAGE OUTLINE 14 lead plastic dual in-line (type A) (*See General Section*)

[1]) When used with FJH151/7450 or FJH171/7453 as applicable.

CIRCUIT DIAGRAM



RATINGS Limiting values in accrodance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	7.0	V
Input voltage	V_G	max.	5.5	V[1]
Peak negative G input voltage	$-V_{GM}$	max.	2	V[2]
Storage temperature	T_{stg}	-65 to +150		°C
Operating ambient temperature	T_{amb}	0 to +70		°C

[1] In addition the voltage between any two inputs: max. 5.5 V.
[2] Pulse duration $t_p = 20$ ns; repetition frequency f = 5 MHz; source resistance $R_S \geq 75\ \Omega$.

CHARACTERISTICS [1])

			T_{amb} (°C)				Conditions and references	
			0	25	70		V_P (V)	
STATIC DATA								
Voltages								
Input threshold LOW	V_{GLmax}		0.8	0.8	0.8	V		
Input threshold HIGH	V_{GHmin}		2.0	2.0	2.0	V		
Currents								
Input LOW	$-I_{GLmax}$		1.6	1.6	1.6	mA	5.25	V_G = 0.40 V
Input HIGH	I_{GHmax}		40	40	40	µA	5.25	V_G = 2.4 V
SUPPLY DATA								
Supply current								
Input LOW	I_{PL}	typ.	-	2.0	-	mA	5.0	V_G = 0
	I_{PL}	<	4.0	4.0	4.0	mA	5.25	
Input HIGH	I_{PH}	typ.	-	1.2	-	mA	5.0	V_G = 5.0 V
	I_{PH}	<	2.5	2.5	2.5	mA	5.25	
DYNAMIC DATA								
Rise propagation delay time	t_{pdr}	typ.	-	15	-	ns	5.0	C_L = 15 pF, N = 10
		<	-	30	-	ns		
Fall propagation delay time	t_{pdf}	typ.	-	10	-	ns	5.0	
		<	-	20	-	ns		

[1]) When used in conjunction with the FJH151/7450

TTL GJ family

GJH101/74H30	single 8-input NAND gate
GJH111/74H20	dual 4-input NAND gate
GJH121/74H10	triple 3-input NAND gate
GJH131/74H00	quadruple 2-input NAND gate
GJH141/74H40	dual NAND power gate
GJH231/74H01	quadruple 2-input NAND gate
GJJ111/74H72	JK master-slave FLIP-FLOP
GJJ131/74H74	dual D-type edge-triggered FLIP-FLOP

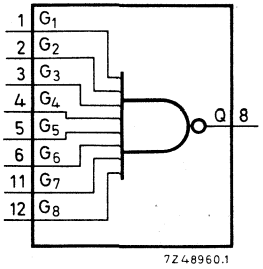
The GJ family of TTL silicon monolithic integrated circuits is designed for use in high speed digital equipment.

Using the same supply voltage (5 V) and maintaining the same noise margin (typ. 1 V), this range is compatible with the medium speed FJ/74N series.

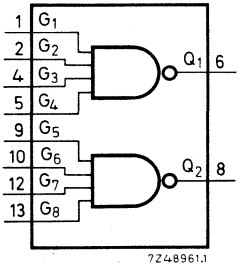
This allows the selective use of GJ types in system locations where its high speed is required. The FJ/74N series types can then be used in other locations, thereby minimizing the total system dissipation.

NAND GATES

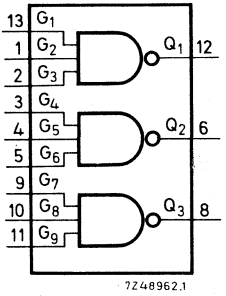
Single 8-input NAND gate	GJH101/74H30
Dual 4-input NAND gate	GJH111/74H20
Triple 3-input NAND gate	GJH121/74H10
Quadruple 2-input NAND gate	GJH131/74H00



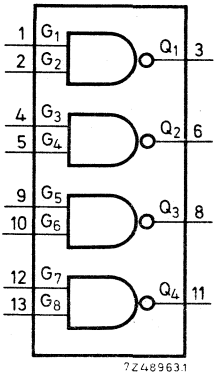
GJH101/74H30



GJH111/74H20



GJH121/74H10



GJH131/74H00

QUICK REFERENCE DATA

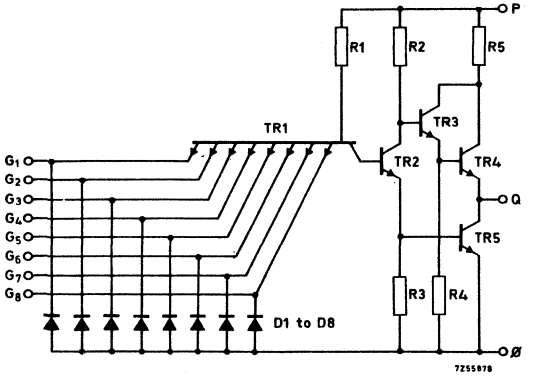
Supply voltage	V_P		5.0 ± 5%	V
Operating ambient temperature range	T_{amb}		0 to +70	°C
Average propagation delay time N = fan-out = 10; T_{amb} = 25 °C	t_{pd}	typ.	6	ns
Available d.c. fan-out (full temperature range)	N_a	≥	10	
D.C. noise margin (full temperature range)	M_L	> typ.	0.4 1.0	V V
Average power consumption (per gate) T_{amb} = 25 °C	P_{av}	typ.	23	mW

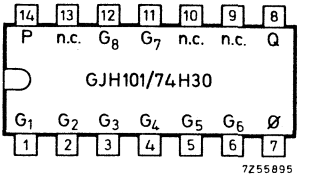
PACKAGE OUTLINE : 14 lead plastic dual in-line (type A) (See General Section).

CIRCUIT DIAGRAMS AND TERMINAL CONNECTIONS

GJH101/74H30

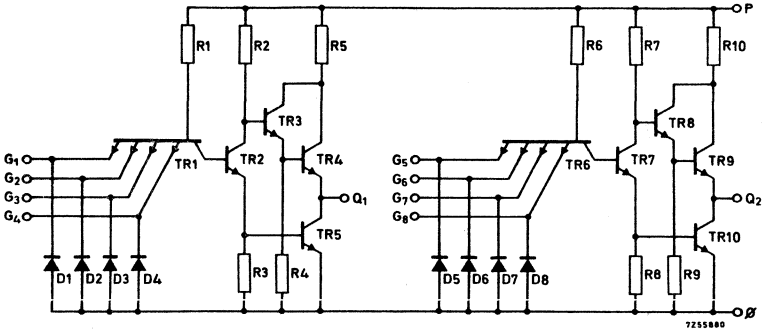
Single 8-input NAND gate

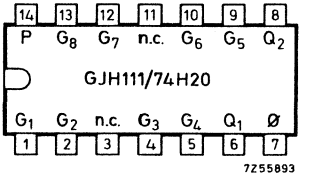




GJH111/74H20

Dual 4-input NAND gate

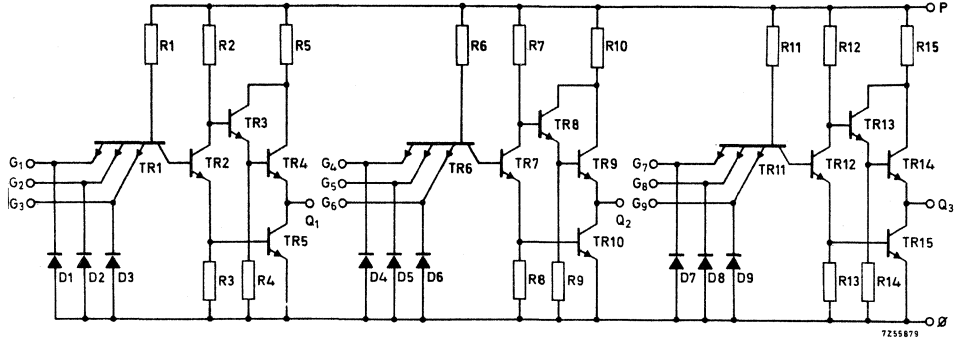


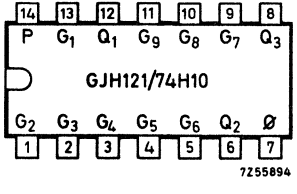


CIRCUIT DIAGRAMS AND TERMINAL CONNECTIONS (continued)

GJH121/74H10

Triple 3-input NAND gate

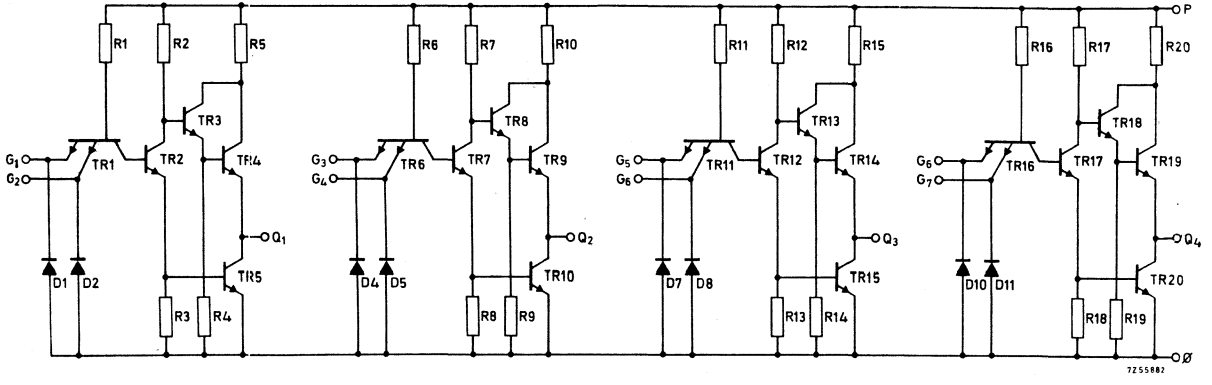


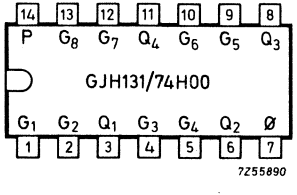


CIRCUIT DIAGRAMS AND TERMINAL CONNECTIONS (continued)

GJH131/74H00

Quadruple 2-input NAND gate





LOGIC FUNCTION

Individual gate operation

$C = \overline{A.B}$ positive logic

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

Function table

A	B	C
L	L	H
L	H	H
H	L	H
H	H	L

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.	7.0	V
Output voltage	V_Q	max.	5.5	V
G input voltage	V_G	0 to	5.5	V [1]
Storage temperature	T_{stg}	-65 to	+150	°C
Operating ambient temperature	T_{amb}	0 to	+ 70	°C

[1]) In addition the voltage difference between any two inputs:max. 5.5 V.

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references	
		0	25	70		V_P (V)	
STATIC DATA							
Voltages							
Input threshold LOW	V_{GLmax}	0.8	0.8	0.8	V		
Input threshold HIGH	V_{GHmin}	2.0	2.0	2.0	V		
Output LOW	V_{QLmax}	0.4	0.4	0.4	V	4.75	$I_Q = I_{QLmax}$; $V_G = V_{GHmin}$
Output HIGH	V_{QHmin}	2.4	2.4	2.4	V	4.75	$-I_Q = -I_{QHmax}$; $V_G = V_{GLmax}$
Currents							
Input LOW	$-I_{GLmax}$	2	2	2	mA	5.25	$V_G = V_{QLmax}$
Input HIGH	I_{GHmax}	50	50	50	µA	5.25	$V_G = V_{QHmin}$
	I_{GHmax}	1	1	1	mA	5.25	V_G = 5.5 V
Output LOW	I_{QLmax}	20	20	20	mA		
Output HIGH	$-I_{QHmax}$	0.5	0.5	0.5	mA		
Output short-circuited	$-I_{Qsc\,min}$ $-I_{Qsc\,max}$	40 100	40 100	40 100	mA mA	5.25	$V_Q = 0$; $V_G = 0$
DYNAMIC DATA							
Rise propagation delay time	t_{pdr} <	-	10	-	ns	5.0	N = 10 C_L = 25 pF R_L = 280 Ω
Fall propagation delay time[1])	t_{pdf} <	-	10	-	ns	5.0	

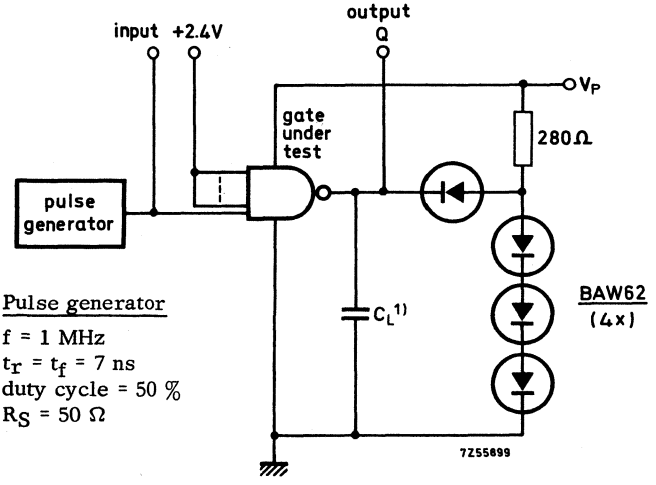
[1]) For GJH101/74H30 t_{pdf} < 12 ns.

CHARACTERISTICS (continued)

		T_{amb} (°C)				Conditions and references	
		0	25	70		V_P (V)	
SUPPLY DATA							
Supply current							
Output LOW							
GJH101/74H30	I_{PL} <	10	10	10	mA	5.25	V_G = 4.5 V, I_Q = 0
GJH111/74H20	I_{PL} <	20	20	20	mA	5.25	
GJH121/74H10	I_{PL} <	30	30	30	mA	5.25	
GJH131/74H00	I_{PL} <	40	40	40	mA	5.25	
Output HIGH							
GJH101/74H30	I_{PH} <	4.2	4.2	4.2	mA	5.25	V_G = 0, I_Q = 0
GJH111/74H20	I_{PH} <	8.4	8.4	8.4	mA	5.25	
GJH121/74H10	I_{PH} <	12.6	12.6	12.4	mA	5.25	
GJH131/74H00	I_{PH} <	16.8	16.8	16.8	mA	5.25	

CHARACTERISTICS (continued)

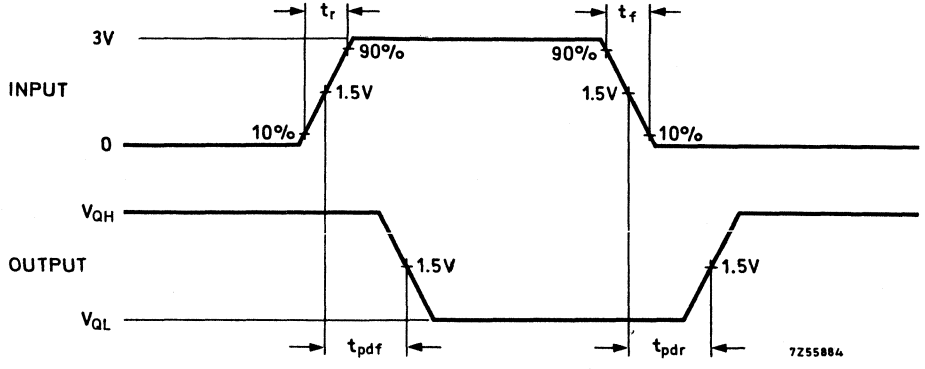
Test circuit:



Pulse generator

f = 1 MHz
$t_r = t_f$ = 7 ns
duty cycle = 50 %
R_S = 50 Ω

1) C_L includes probe and jig capacitance



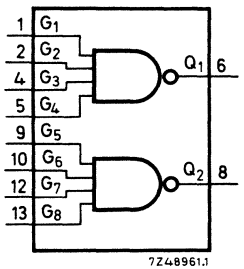
Waveforms illustrating measurement of t_{pdr} and t_{pdf}.

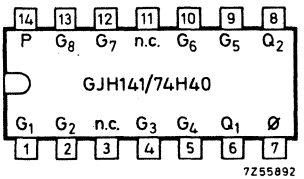
The GJ family of TTL silicon monolithic integrated circuits is designed for use in high speed digital equipment.

Using the same supply voltage (5 V) and maintaining the same noise margin (typ. 1 V), this range is compatible with the medium speed FJ/74N series.

This allows the selective use of GJ types in system locations where its high speed is required. The FJ/74N series types can then be used in other locations, thereby minimizing the total system dissipation.

DUAL NAND POWER GATE

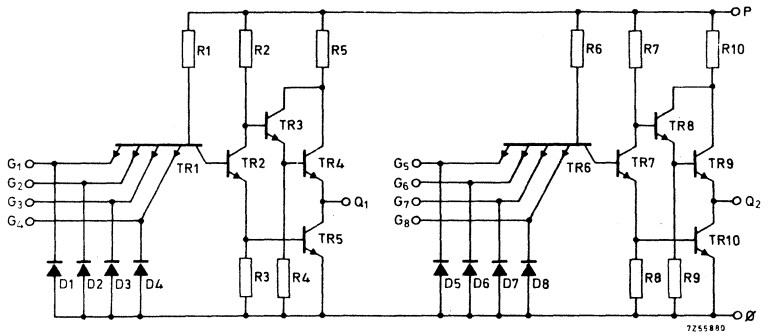




QUICK REFERENCE DATA				
Supply voltage	V_P		5.0 ± 5%	V
Operating ambient temperature	T_{amb}		0 to + 70	°C
Average propagation delay time N = fan-out = 30; T_{amb} = 25 °C	t_{pd}	typ.	7.5	ns
Available d.c. fan-out (full temperature range)	N_a	≥	30	
D.C. noise margin (full temperature range)	M_L	> typ.	0.4 1.0	V V
Average power consumption (per gate) T_{amb} = 25 °C	P_{av}	typ.	44	mW

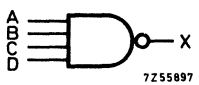
PACKAGE OUTLINE 14 lead plastic dual in-line (type A) (See General Section).

CIRCUIT DIAGRAM



LOGIC FUNCTION

Individual gate operation



$X = \overline{A.B.C.D}$
(for positive logic)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.	7.0	V
Output voltage	V_Q	max.	5.5	V
G input voltage	V_G	max.	5.5	V [1]
Storage temperature	T_{stg}	−65 to	+150	°C
Operating ambient temperature	T_{amb}	0 to	+70	°C

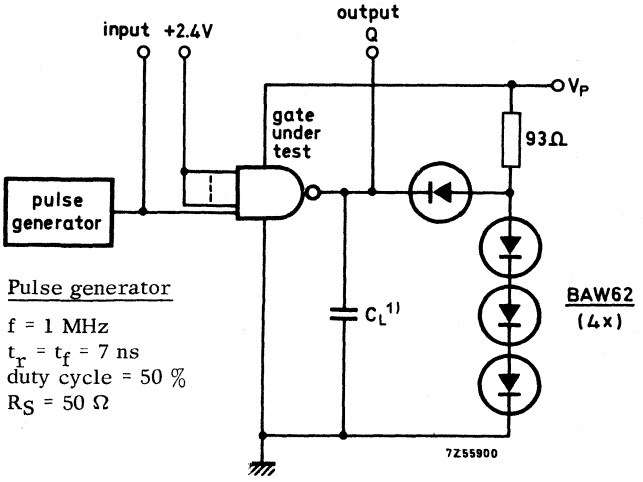
[1]) In addition, peak voltage difference between any two inputs: max. 5.5 V.

CHARACTERISTICS

		T_{amb} (°C)			Conditions and references	
		0	25	70	V_P (V)	
STATIC DATA						
Voltages						
Input threshold LOW	V_{GLmax}	0.8	0.8	0.8 V		
Input threshold HIGH	V_{GHmin}	2.0	2.0	2.0 V		
Output LOW	V_{QLmax}	0.4	0.4	0.4 V	4.75	$I_Q = I_{QLmax}$; $V_G = V_{GHmin}$
Output HIGH	V_{QHmin}	2.4	2.4	2.4 V	4.75	$-I_Q = -I_{QHmax}$; $V_G = V_{GLmax}$
Currents						
Input LOW	$-I_{GLmax}$	4	4	4 mA	5.25	$V_G = V_{QLmax}$
Input HIGH	I_{GHmax}	100	100	100 µA	5.25	$V_G = V_{QHmin}$
	I_{GHmax}	1	1	1 mA	5.25	$V_G = 5.5$ V
Output LOW	I_{QLmax}	60	60	60 mA		
Output HIGH	$-I_{QHmax}$	1.5	1.5	1.5 mA		
Output short-circuited	$-I_{Qsc}$ min $-I_{Qsc}$ max	40 125	40 125	40 mA 125 mA	5.25	$V_Q = 0$; $V_G = 0$
SUPPLY DATA						
Supply current						
Output LOW	I_{PL} typ. I_{PL} <	- 40	25 40	- mA 40 mA	5.0 5.25	$V_G = 4.5$ V; $I_Q = 0$
Output HIGH	I_{PH} typ. I_{PH} <	- 16	10.4 16	- mA 16 mA	5.0 5.25	$V_G = 0$; $I_Q = 0$
DYNAMIC DATA						
Rise propagation delay time	t_{pdr} typ. t_{pdr} <	- -	8.5 12	- ns - ns	5.0	N = 30 C_L = 25 pF R_L = 93 Ω
Fall propagation delay time	t_{pdf} typ. t_{pdf} <	- -	6.5 12	- ns - ns	5.0	

CHARACTERISTICS (continued)

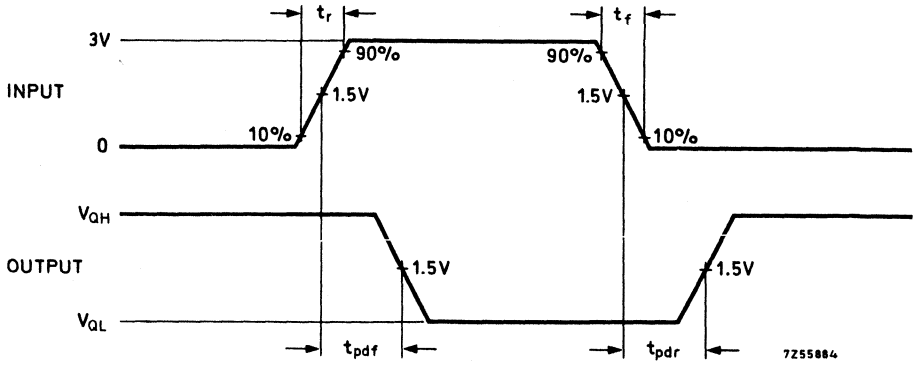
Test circuit:



Pulse generator

f = 1 MHz
$t_r = t_f$ = 7 ns
duty cycle = 50 %
R_S = 50 Ω

1) C_L includes probe and jig capacitance



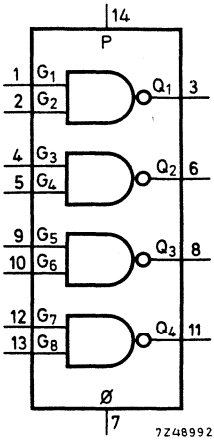
Waveforms illustrating measurement of t_{pdr} and t_{pdf}.

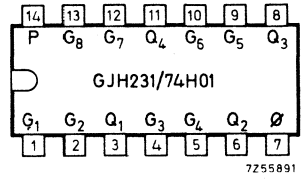
The GJ family of TTL silicon monolithic integrated circuits is designed for use in high speed digital equipment.

Using the same supply voltage (5 V) and maintaining the same noise margin (typ. 1 V), this range is compatible with the medium speed FJ/74N series.

This allows the selective use of GJ types in system locations where its high speed is required. The FJ/74N series types can then be used in other locations, thereby minimizing the total system dissipation.

QUADRUPLE 2-INPUT NAND GATE



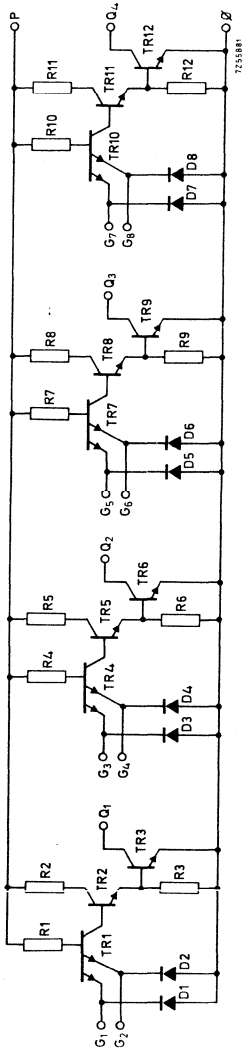


QUICK REFERENCE DATA				
Supply voltage	V_P		5.0 ± 5%	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Average propagation delay time N = fan-out = 10; T_{amb} = 25 °C	t_{pd}	typ.	9	ns
Available d.c. fan-out (full temperature range)	N_a	≥	10	
D.C. noise margin (full temperature range)	M_L	>	0.4	V
		typ.	1.0	V
Average power consumption (each gate) T_{amb} = 25 °C	P_{av}	typ.	21	mW

The GJH231/74H01 is a quadruple 2-input NAND gate with open-collector output transistors for use in "wired-OR" connection with other gates of the GJ and FJ family.

PACKAGE OUTLINE 14 lead plastic dual in-line (type A) (See General Section).

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.	7.0	V
G input voltage	V_G	max.	5.5	V [1])
Storage temperature	T_{stg}	−65 to	+150	°C
Operating ambient temperature	T_{amb}	0 to	+70	°C

[1]) In addition, the voltage between any two inputs must not exceed 5.5 V.

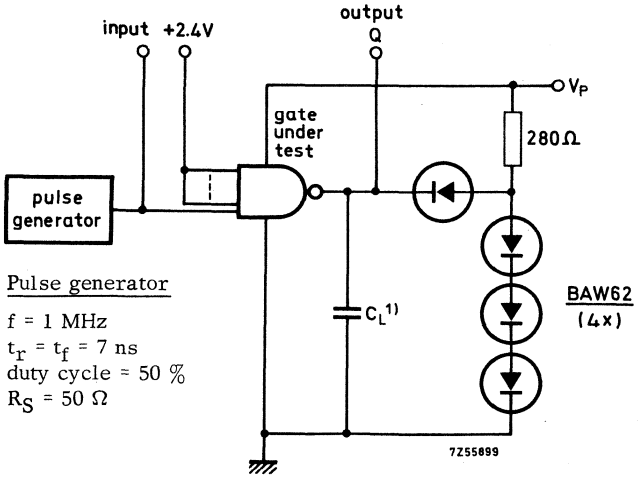
CHARACTERISTICS

		T_{amb} (°C)				Conditions and references
		0	25	70	V_P (V)	
STATIC DATA						
Voltages						
Input threshold LOW	V_{GLmax}	0.8	0.8	0.8 V		
Input threshold HIGH	V_{GHmin}	2.0	2.0	2.0 V		
Output LOW	V_{QLmax}	0.4	0.4	0.4 V	4.75	$I_Q = I_{QLmax}$; $V_G = V_{GHmin}$
Currents						
Input LOW	$-I_{GLmax}$	2	2	2 mA	5.25	$V_G = V_{QLmax}$
Input HIGH	I_{GHmax}	50	50	50 µA	5.25	V_G = 2.4 V
	I_{GHmax}	1	1	1 mA	5.25	V_G = 5.5 V
Output LOW	I_{QLmax}	20	20	20 mA		
Output HIGH(reverse)	I_{QHmax}	250	250	250 µA	4.75	$V_G = V_{GLmax}$; V_Q = 5.5 V
SUPPLY DATA						
Supply current						
Output LOW	I_{PL} typ.	-	26	- mA	5.0	V_G = 4.5 V
	I_{PL} <	40	40	40 mA	5.25	
Output HIGH	I_{PH} typ.	-	6.8	- mA	5.0	V_G = 0
	I_{PH} <	10	10	10 mA	5.25	
DYNAMIC DATA						
Rise propagation delay time	t_{pdr} typ.	-	10	- ns	5.0	R_L = 280 Ω
	t_{pdr} <	-	15	- ns	5.0	
Fall propagation delay time	t_{pdf} typ.	-	7.5	- ns	5.0	C_L = 25 pF
	t_{pdf} <	-	12	- ns	5.0	

CHARACTERISTICS (continued)

DYNAMIC DATA

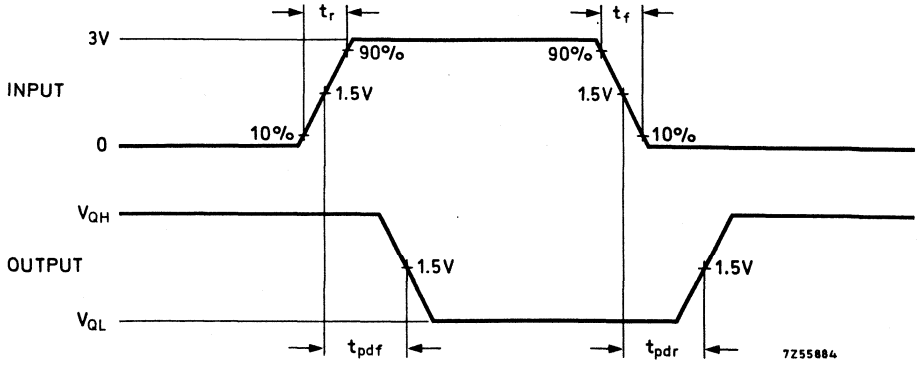
Test circuit



Pulse generator

f = 1 MHz
$t_r = t_f$ = 7 ns
duty cycle = 50 %
R_S = 50 Ω

[1]) C_L includes probe and jig capacitance

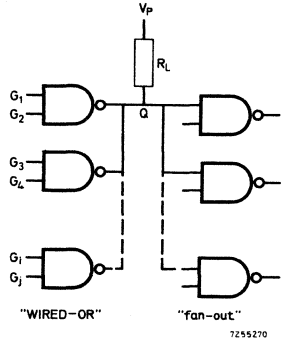


Waveforms illustrating measurement of t_{pdr} and t_{pdf}.

APPLICATION INFORMATION

Fan-out and the "wired-OR" function

TTL gates with open collector can be connected to a common load resistor (R_L) to give a wired-OR function.
A GJ gate alone will drive 10 loads in the GJ family; when it is paralleled with other gates it can drive from 1 to 9 loads.



Wired-OR logic function (positive logic)

$$Q = \overline{G_1.G_2 + G_3.G_4 + \ldots\ldots + G_i.G_j}$$

APPLICATION INFORMATION (continued)

Determining the value of R_L

Proper operation of the functions mentioned depends on the value of the common load resistor. The maximum value is set by the need to ensure sufficient load current to TTL loads and off current I_{QHmax} through paralleled outputs when the output is HIGH. A minimum value is set by the need to limit the total current through the resistor, including the "sink" current of the TTL (GJ family) loads, so that the output voltage does not rise above the LOW level, even when one of the paralleled outputs is absorbing all the current. The table shows minimum and maximum resistor values for up to 10 TTL (GJ family) loads and up to 7 gates connected in wired-OR.

Table I

fan-out to TTL loads	wired-OR outputs							
	1	2	3	4	5	6	7	1 to 7
1	8666	4727	3250	2476	2000	1677	1444	255
2	7428	4333	3058	2363	1925	1625	1405	288
3	6500	4000	2888	2260	1857	1575	1368	323
4	5777	3714	2736	2166	1793	1529	1333	384
5	5200	3466	2600	2080	1733	1485	1300	460
6	4727	3250	2476	2000	1677	1444	1268	578
7	4333	3058	2363	1925	1625	1405	1238	767
8	4000	2888	2260	1857	1575	1368	1209	1150
9	3714	2736	X	X	X	X	X	2300
10	3466	X	X	X	X	X	X	3466*
	maximum							min.
	load resistor value in ohms							

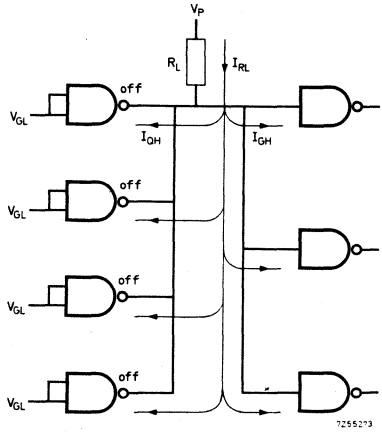
X = not recommended or not possible
* = the theoretical value is ∞
All values shown in the table are based on:
Logical HIGH conditions: V_P = 5 V; V_{QH} required = 2.4 V
Logical LOW conditions: V_P = 5 V; V_{QL} required = 0.4 V

APPLICATION INFORMATION (continued)

Circuit calculations

HIGH (off level) configurations (see figure below)

GJ family loads



M = 4 N = 3

$M.I_{QH} = 4 \times 250\ \mu A$ $N.I_{GH} = 3 \times 50\ \mu A$ $R_{Lmax} = \frac{(5 - 2.4)\ V}{(0.001 + 0.00015)A} = 2260\ \Omega$

The allowable voltage drop across the load resistor (V_{RL}) is the difference between V_P applied and the output voltage V_{QH} required at the TTL load.

$$V_{RL} = V_P - V_{QHmin}$$

The total current through the load resistor (I_{RL}) is the sum of the load currents I_{GH} and off-level reverse current I_{QH} through each of the "wired-OR" connected outputs. Putting N as the number of TTL (GJ family) loads, and M as the number of outputs, the current is given by

$$I_{RL} = M.I_{QH} + N.I_{GH}$$

Therefore, the maximum value of R_L is

$$R_{Lmax} = \frac{V_P - V_{QHmin}}{M.I_{QH} + N.I_{GH}}$$

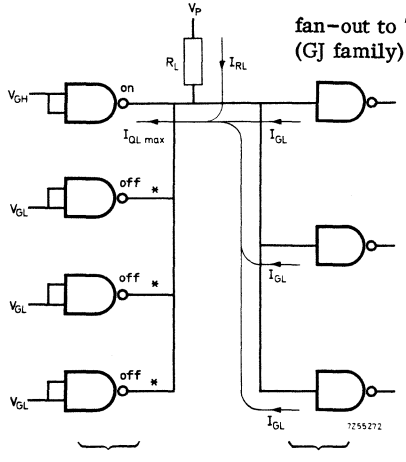
APPLICATION INFORMATION (continued)

LOW (on level) configurations (see figure below)

The current through the resistor must be limited to the maximum for one output transistor. If several outputs are "wired-OR" connected the current through R_L may be shared among the paralleled output transistors, but, unless it can be guaranteed that more than one transistor will be in the ON (conducting) state during the LOW output periods, the current must be limited to 20 mA, i.e. the maximum current that will still ensure a maximum LOW output voltage of 0.4 V.
The fan-out current must be considered as well. Part of the 20 mA will be supplied from the inputs being driven, which further reduces the current through R_L.
These considerations lead to the minimum value of R_L:

$$R_{Lmin} = \frac{V_P - V_{QLmax}}{I_{QLmax} - N. \left|I_{GLmax}\right|}$$

For up to 10 TTL (GJ family) loads and up to 7 "wired-OR" connected outputs table I gives the maximum and minimum values of R_L calculated in this way.
For a single output the values are determined by the fan-out plus the leakage current of one transistor.
More than 7 outputs can be connected in "wired-OR" provided valid maximum and minimum resistor values are possible.
The value of R_L for driving 10 loads should be infinite according to these calculations but 3466 Ω is sufficient to satisfy logic HIGH while keeping logic LOW to less than 0.42 V.



M = 4 N = 3

I_{QLmax} = 20 mA N. $\left|I_{GLmax}\right|$ = 3 x 2 mA $R_{Lmin} = \frac{(5 - 0.4)V}{(0.020 - 0.006)A}$ = 323 Ω

*) current through OFF outputs negligible at LOW output state

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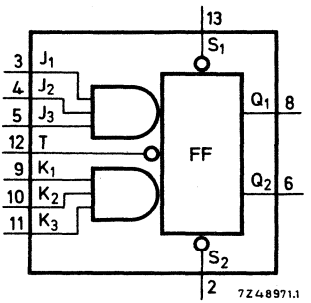
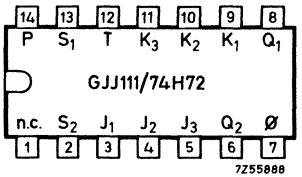
Using the same supply voltage (5 V) and maintaining the same noise margin (typ. 1 V), this range is compatible with the medium speed FJ/74N series.

This allows the selective use of GJ types in system locations where its high speed is required. The FJ/74N series types can then be used in other locations, thereby minimizing the total system dissipation.

JK MASTER-SLAVE FLIP-FLOP

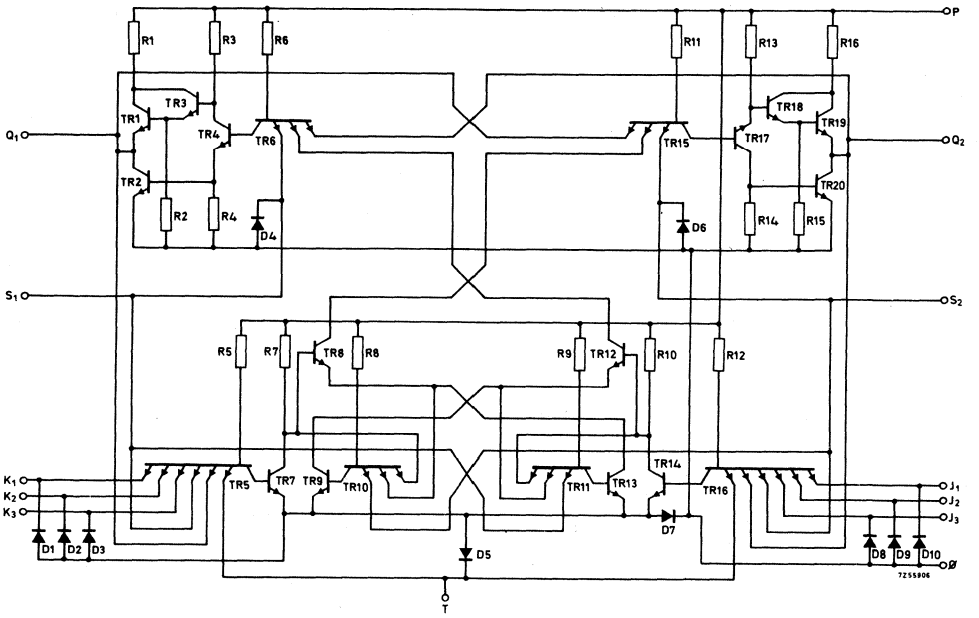




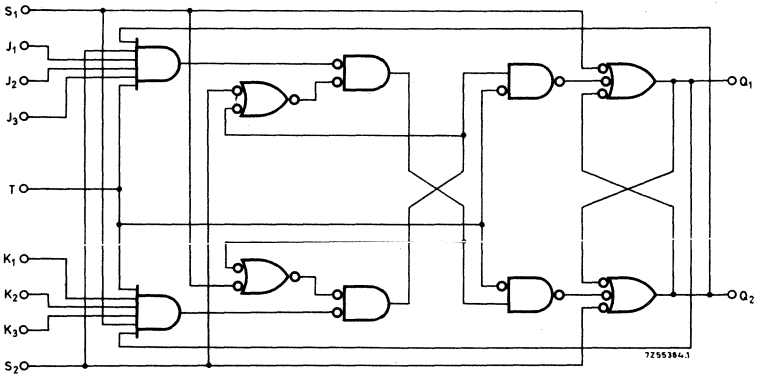
QUICK REFERENCE DATA				
Supply voltage	V_P		5.0 ± 5%	V
Operating ambient temperature range	T_{amb}		0 to +70	°C
Available d.c. fan-out (full temperature range)	N_a	≥	10	
Max. operating frequency; T_{amb} = 25 °C	f	>	25	MHz
Average power consumption; T_{amb} = 25 °C	P_{av}	typ.	80	mW

PACKAGE OUTLINE 14 lead plastic dual in-line (Type A)(See General Section).

CIRCUIT DIAGRAM



LOGIC DIAGRAM



FUNCTION TABLE

t_n		$t_n + 1$
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

$J = J_1 . J_2 . J_3$
$K = K_1 . K_2 . K_3$
t_n = bit time before clock pulse
t_{n+1} = bit time after clock pulse

positive logic:

LOW input to S_1 sets Q HIGH
LOW input to S_2 sets Q LOW
S_1 and S_2 functions are independent of T

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.	7.0	V
Output voltage	V_Q	max.	5.5	V
Input voltage	V_J, V_K, V_T, V_S	max.	5.5	V [1]
Storage temperature	T_{stg}	-65 to	+150	°C
Operating ambient temperature	T_{amb}	0 to	+70	°C

[1]) In addition, peak voltage difference between any two inputs: max. 5.5 V.

CHARACTERISTICS

		T_{amb}(°C)				Conditions and references	
		0	25	70		V_P (V)	
STATIC DATA							
Voltages							
Input threshold LOW (any input)	V_{ILmax}	0.8	0.8	0.8	V		
Input threshold HIGH (any input)	V_{IHmin}	2.0	2.0	2.0	V		
Output LOW	V_{QLmax}	0.4	0.4	0.4	V	4.75	I_Q = 20 mA
Output HIGH	V_{QHmin}	2.4	2.4	2.4	V	4.75	$-I_Q$ = 500 μA
Currents							
Input LOW (J, K, T)	$-I_{ILmax}$	2.0	2.0	2.0	mA	5.25	$V_I = V_{QLmax}$
Input HIGH (J, K)	I_{IHmax}	50	50	50	μA	5.25	$V_I = V_{QHmin}$
	I_{IHmax}	1.0	1.0	1.0	mA	5.25	V_I = 5.5 V
Input LOW (S)	$-I_{SLmax}$	4.0	4.0	4.0	mA	5.25	$V_S = V_{QLmax}$
Input HIGH (S)	I_{SHmax}	100	100	100	μA	5.25	$V_S = V_{QHmin}$
	I_{SHmax}	1.0	1.0	1.0	mA	5.25	V_S = 5.5 V
Input HIGH (T)	I_{THmax}	50	50	50	μA	5.25	$V_T = V_{QHmin}$
	I_{THmax}	1.0	1.0	1.0	mA	5.25	V_T = 5.5 V
Output short circuited	$-I_{Qscmin}$	40	40	40	mA	5.25	V_Q = 0
	$-I_{Qscmax}$	100	100	100	mA		
SUPPLY DATA							
Supply current	I_P typ.	-	16	-	mA	5.0	
	I_P <	25	25	25	mA	5.25	

CHARACTERISTICS (continued)

			T_{amb} (°C)				Conditions and references	
			0	25	70		V_P (V)	
DYNAMIC DATA							5.0 V	N = 10 C_L = 25 pF
Signal requirements								
Pulse duration (T input)	t_{TL}	>	-	12	-	ns	↓	↓
Pulse duration (S input)	t_{SL}	>	-	16	-	ns		
Performance								
Rise propagation delay time (S→Q)	t_{pdr}	typ.	-	6	-	ns		
	t_{pdr}	<	-	13	-	ns		
Fall propagation delay time (S→Q)	t_{pdf}	typ.	-	12	-	ns		
	t_{pdf}	<	-	24	-	ns		
Rise propagation delay time (T→Q)	t_{pdr}	typ.	-	16	-	ns		
	t_{pdr}	<	-	21	-	ns		
Fall propagation delay time (T→Q)	t_{pdf}	typ.	-	22	-	ns		
	t_{pdf}	<	-	27	-	ns		
Set-up time	t_{su}	>	-	12	-	ns		
Hold time	t_{hold}	>	-	0	-	ns		
Operating frequency (T input)	f_{max}	<	-	25	-	MHz		

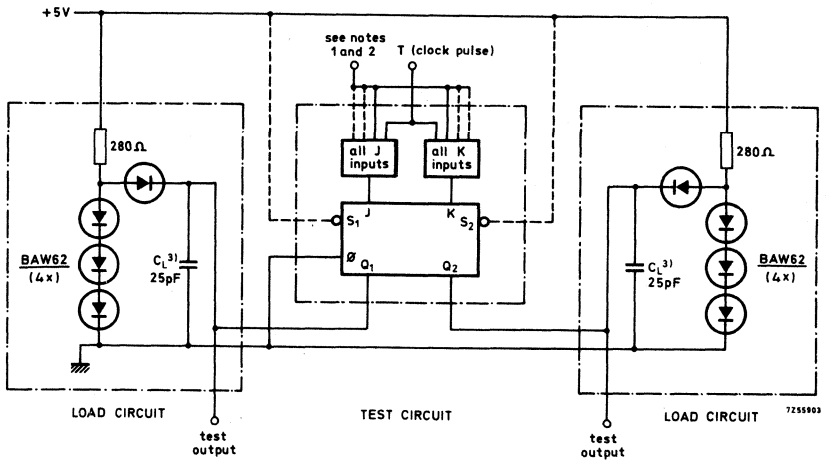
Notes:

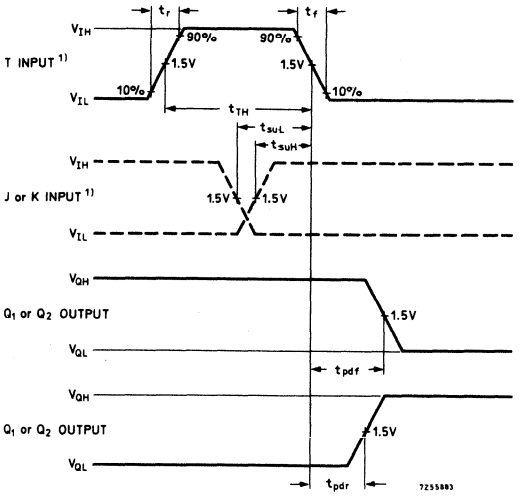
Set-up time: t_{su} is defined as the interval immediately preceding the positive going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.

Hold time: t_{hold} is defined as the interval immediately following the positive-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its continued recognition.

CHARACTERISTICS (continued)

DYNAMIC DATA





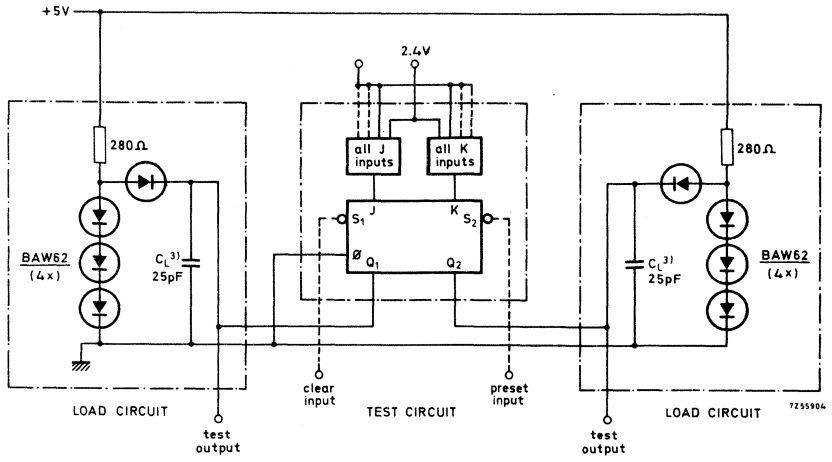
1) When testing t_{pdr} and t_{pdf} the clock (T input) characteristics are V_I = 0 to +3 V; $t_r = t_f$ = 7 ns; t_{TL} = 20 ns and f = 1 MHz. All J and K inputs are held at 2.4 V.

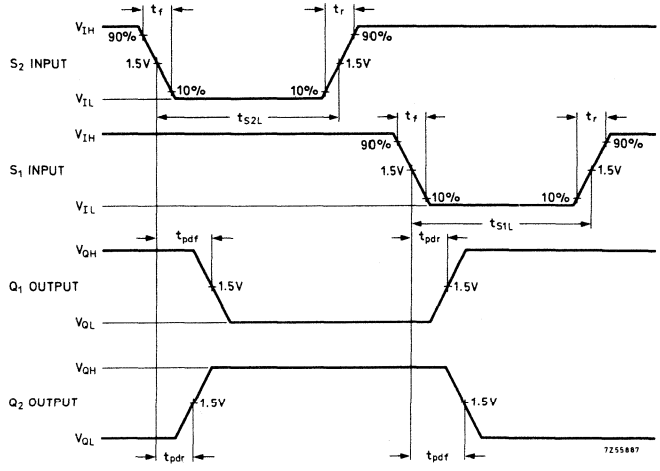
2) When testing the operation frequency, the clock (T input) characteristics are V_I = 0 to +3 V; $t_r = t_f$ = 3 ns; t_{TL} = 12 ns and f = 25 MHz. All J and K inputs are held at 2.4 V.

3) C_L includes probe and jig capacitance.

CHARACTERISTICS (continued)

DYNAMIC DATA





1) $\overline{S_2}$ and $\overline{S_1}$ inputs dominate regardless of the state of T or J-K inputs.

2) S_2 or S_1 input pulse characteristics: V_I = 0 to 3 V; $t_r = t_f$ = 7 ns; $t_{S1L} = t_{S2L}$ = 16 ns and f = 1MHz.

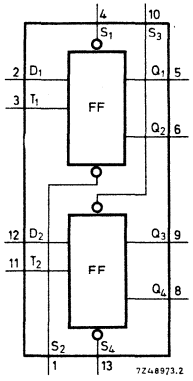
3) C_L includes probe and jig capacitance.

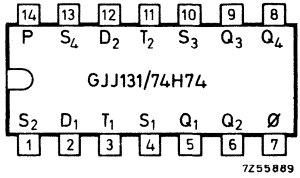
The GJ family of TTL silicon monolithic integrated circuits is designed for use in high speed digital equipment.

Using the same supply voltage (5 V) and maintaining the same noise margin (typ. 1 V), this range is compatible with the medium speed FJ/74N series.

This allows the selective use of GJ types in system locations where its high speed is required. The FJ/74N series types can then be used in other locations, thereby minimizing the total system dissipation.

DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOP



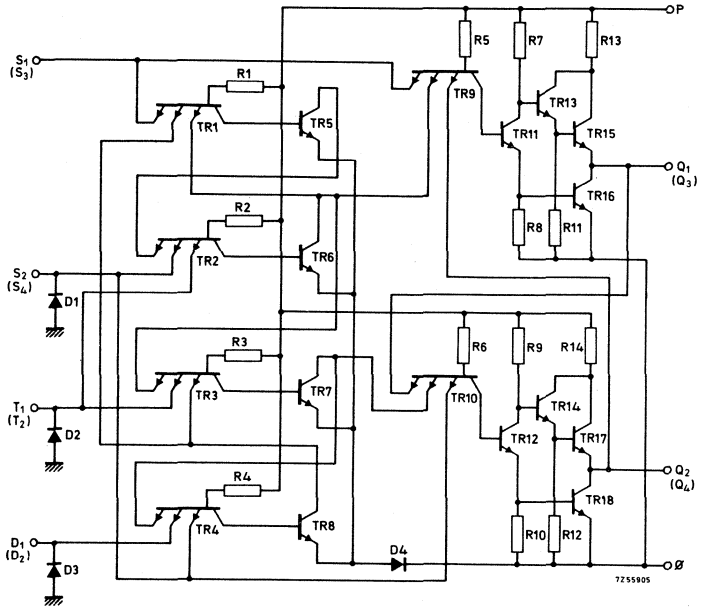


QUICK REFERENCE DATA				
Supply voltage	V_P		5.0 ± 5%	V
Operating ambient temperature range	T_{amb}		0 to + 70	°C
Available d.c. fan-out LOW level	N_a	≥	10	
full temperature range HIGH level	N_a	≥	20	
Max. operating frequency; T_{amb} = 25 °C	f		34	MHz
Total power consumption; T_{amb} = 25 °C	P_{tot}	typ.	150	mW

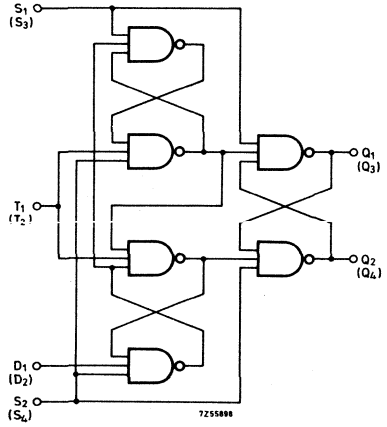
The GJJ131/74H74 is an edge-triggered dual D-type flip-flop with direct SET inputs and complementary outputs. On the positive going edge of the clock pulse the information on the D input is transferred to the Q output. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse.

PACKAGE OUTLINE : 14 lead plastic dual in-line (type A) (See General Section).

CIRCUIT DIAGRAM



LOGIC DIAGRAM



FUNCTION TABLE

t_n	t_{n+1}	
D	Q_1	Q_2
L	L	H
H	H	L

t_n = bit time before clock pulse
t_{n+1} = bit time after clock pulse.

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

RATINGS Limting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.	7.0	V
Output voltage	V_Q	max.	5.5	V
Input voltage	V_D, V_S, V_T	max.	5.5	V [1])
Storage temperature	T_{stg}	-65 to	+150	°C
Operating ambient temperature	T_{amb}	0 to	+70	°C

[1]) In addition, peak voltage difference between any two inputs: max. 5.5 V.

CHARACTERISTICS

		T_{amb} (°C)				Conditions and references	
		0	25	70		V_P (V)	
STATIC DATA							
Voltages							
Input threshold LOW (any input)	V_{ILmax}	0.8	0.8	0.8	V		
Input threshold HIGH (any input)	V_{IHmin}	2.0	2.0	2.0	V		
Output LOW	V_{QLmax}	0.4	0.4	0.4	V	4.75	$I_Q = I_{QLmax}$
Output HIGH	V_{QHmin}	2.4	2.4	2.4	V	4.75	$-I_Q = -I_{QHmax}$
Currents							
Input LOW (S_1, D_1)	$-I_{ILmax}$	2.0	2.0	2.0	mA	5.25	V_{S1}, V_{D1} = V_{QLmax}
Input LOW (S_2, T_1)	$-I_{ILmax}$	4.0	4.0	4.0	mA	5.25	V_{S2}, V_{T1} = V_{QLmax}
Input HIGH (D)	I_{DHmax}	50	50	50	µA	5.25	$V_D = V_{QHmin}$
	I_{DHmax}	1.0	1.0	1.0	mA	5.25	V_D = 5.5 V
Input HIGH (S_1,T_1)	I_{IHmax}	100	100	100	µA	5.25	V_{S1}, V_{T1} = V_{QHmin}
	I_{IHmax}	1.0	1.0	1.0	mA	5.25	V_{S1}, V_{T1} = 5.5 V
Input HIGH (S_2)	I_{S2Hmax}	150	150	150	µA	5.25	$V_{S2} = V_{QHmin}$
	I_{S2Hmax}	1.0	1.0	1.0	mA	5.25	V_{S2} = 5.5 V
Output LOW	I_{QLmax}	20	20	20	mA		
Output HIGH	$-I_{QHmax}$	1.0	1.0	1.0	mA		
Output short circuited see note 1	$-I_{Qscmin}$	40	40	40	mA	5.25	$V_Q = 0$
	$-I_{Qscmax}$	100	100	100	mA	5.25	
SUPPLY DATA							
Supply current	I_P typ.	-	30	-	mA	5.0	V_I = 5.0 V
	I_P <	50	50	50	mA	5.25	

1) Not more than one output should be short circuited at a time.

CHARACTERISTICS (continued)

		T_{amb} (°C)				Conditions and references	
		0	25	70		V_P (V)	
DYNAMIC DATA						5.0	N = 10 C_L = 25 pF
Signal requirement							
Pulse duration							
(T input)	t_{TH} >	15	15	15	ns	↓	↓
(S input)	t_{SL} >	25	25	25	ns		
Performance							
Rise propagation delay time (S→Q)	t_{pdr} <	-	20	-	ns		
Fall propagation delay time (S→Q)	t_{pdf} <	-	30	-	ns		
Rise propagation delay time (T→Q)	t_{pdr} >	-	4	-	ns		
	t_{pdr} typ.	-	8.5	-	ns		
	t_{pdr} <	-	15	-	ns		
Fall propagation delay time (T→Q)	t_{pdf} >	-	7	-	ns		
	t_{pdf} typ.	-	13	-	ns		
	t_{pdf} <	-	20	-	ns		
Set-up time HIGH	t_{suL} >	-	10	-	ns		
LOW	t_{suH} >	-	15	-	ns		
Hold time	t_{hold} >	-	0	-	ns		
Operating frequency (T input)	f >	-	0	-	MHz		
	f <	-	35	-	MHz		

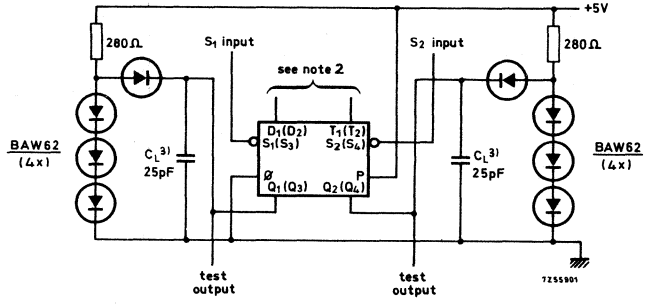
Notes:

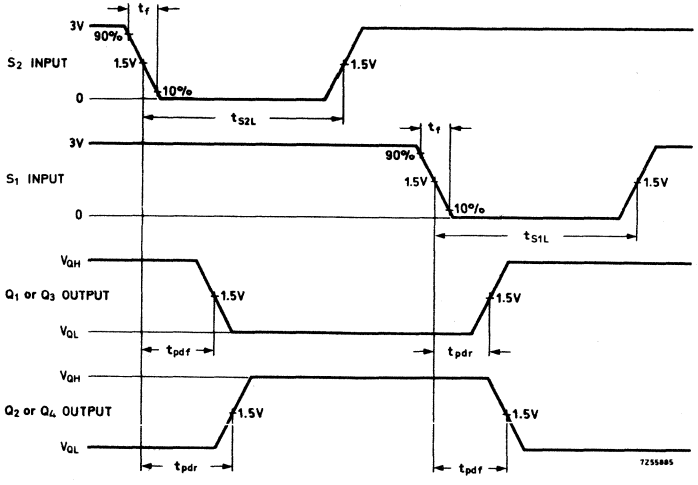
Set-up time: t_{su} is defined as the interval immediately preceding the positive-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.

Hold time : t_{hold} is defined as the interval immediately following the positive-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its continued recognition.

CHARACTERISTICS (continued)

DYNAMIC DATA





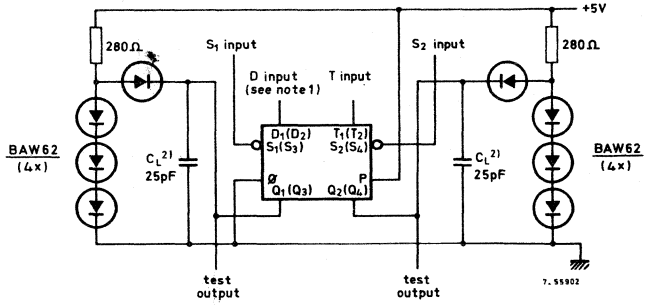
1) S_2 or S_1 input pulse characteristics $t_{S1L} = t_{S2L} = 25$ ns; $t_r = t_f = 7$ ns; f = 1 MHz.

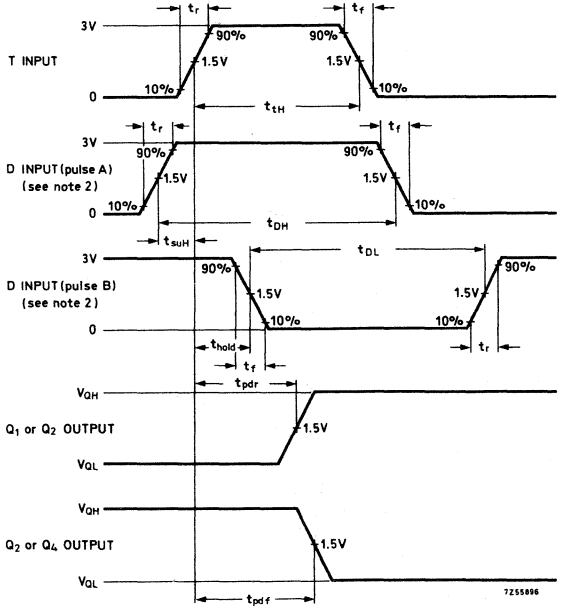
2) S_2 and S_1 inputs dominate regardless of the state of trigger or D inputs.

3) C_L including probe and jig capacitance.

CHARACTERISTICS (continued)

DYNAMIC DATA





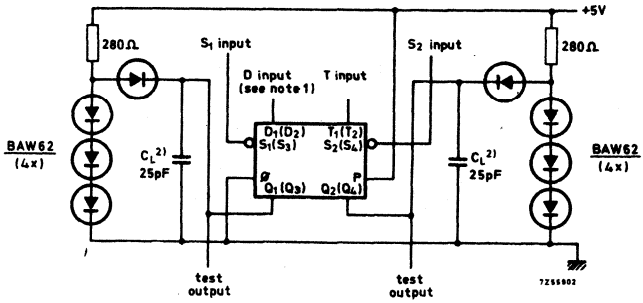
T input pulse has the following characteristics: t_{TH} = 20 ns; f = 1 MHz.

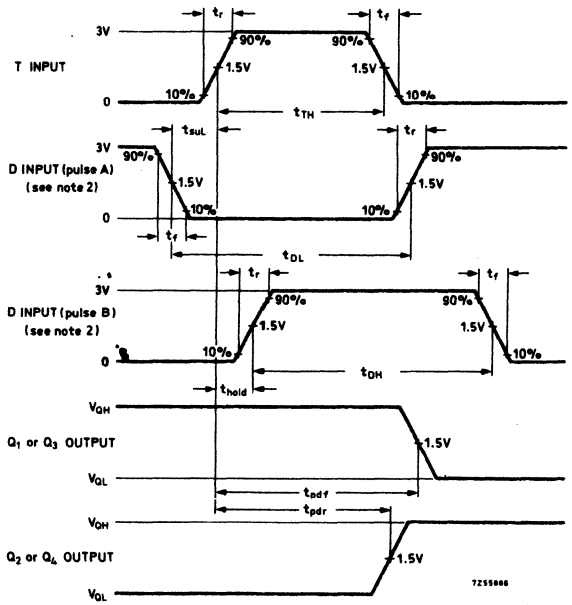
1) D input (pulse A) has the following characteristics: t_{su} = 10 ns; t_{DH} = 60 ns; f = 50 % of the clock frequency. D input (pulse B): t_{hold} = 0 ; t_{DL} = 60 ns; f = 50 % of the clock freq.

2) C_L including probe and jig capacitance.

CHARACTERISTICS (continued)

DYNAMIC DATA





T input pulse has the following characteristics: t_{TH} = 20 ns; f = 1 MHz.

1) D input (pulse A) has the following characteristics: t_{su} = 15 ns; t_{DL} = 60 ns; f = 50 % of the clock frequency. D input (pulse B): t_{hold} = 0; t_{DH} = 60 ns; f = 50 % of the clock frequency.

2) C_L including probe and jig capacitance.

CML

GH family

GHH121/9502	dual 4-input OR/NOR gate (with enable input)
GHH131/9503	triple 2-input OR/NOR gate (with enable input)
GHH141/9504	quadruple 2-input NOR gate (with enable input)
GHH151/9538	one of eight DECODER
GHH161/9581	eight input MULTIPLEXER
GHH171/9505	four wide OR-AND/OR-NAND gate
GHH181/95H02	dual 4-input high speed OR/NOR gate (with enable input)
GHH191/95H03	triple 2-input high speed OR/NOR gate (with enable input)
GHH201/95H04	quadruple 2-input high speed OR/NOR gate (with enable input)
GHH211/95L22	dual 4-input low power OR/NOR gate (with enable input)
GHH221/95L23	triple 2-input low power OR/NOR gate (with enable input)
GHH231/95L24	quadruple 2-input low power NOR gate (with enable input)
GHJ101/9528	high speed dual D-type FLIP-FLOP
GHJ111/9534	resettable quadruple "D" LATCH with I/O ENABLE
GHJ121/95H90	divide by 10/11 PRESCALER
GHL101/9595	dual high speed CML to TTL CONVERTER
GHY101/9582	line RECEIVER/AMPLIFIER

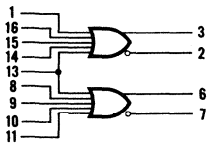
The GH family of CML silicon monolithic integrated circuits is designed for high speed instrumentation, digital communication systems, central processors and computer terminals. All GH family elements incorporate a unique temperature compensation network which insures that significant parameters such as logic levels, noise margin and speed remain relatively constant over a wide temperature range.

The GHH121/9502, GHH131/9503 and GHH141/9504 are OR/NOR gates employing a non-saturating current switch emitter follower configuration to achieve high speed.

Input and output pull-down resistors (2 kΩ) eliminate the necessity for external termination of lines up to 15 cm and unused logic inputs. Package pin locations are chosen to reduce internal noise generation and cross talk. The GH family corresponds to the ECL9500 series.

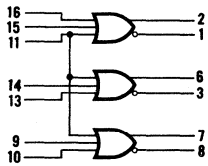
OR/NOR GATES

GHH121/9502



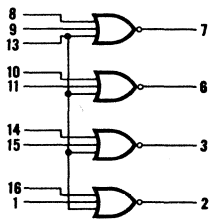
Dual 4-input OR/NOR gate with enable input

GHH131/9503



Triple 2-input OR/NOR gate with enable input

GHH141/9504



Quadruple 2-input NOR gate with enable input

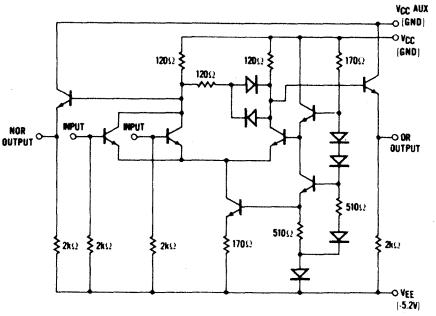
QUICK REFERENCE DATA				
Supply voltage	$-V_{EE}$		5.2	V
Operating ambient temperature range	T_{amb}		0 to +75	°C
Average propagation delay time	t_{pd}	typ.	2.3	ns
Output voltage HIGH state	$-V_{OH}$	nom.	895	mV
LOW state	$-V_{OL}$	nom.	1710	mV
Power consumption per gate				
GHH121/9502	P_{av}	typ.	91	mW
GHH131/9503	P_{av}	typ.	83	mW
GHH141/9504	P_{av}	typ.	70	mW

PACKAGE OUTLINE 16 lead ceramic dual in-line (See General Section).

Note

V_{CC} = ground (pins 4 and 5)
$-V_{EE}$ = 5.2 V (pin 12)

CIRCUIT DIAGRAM



FUNCTIONAL DESCRIPTION

The GH gates are based on the conventional emitter coupled configuration. Additional circuit complexity is incorporated to improve system operating characteristics. This includes temperature compensation networks to insure that logic levels and thresholds, set by the on chip bias driver, are essentially independent of temperature. On chip output emitter follower and input pulldown resistors of 2 kΩ reduce external components normally required for short line termination and unused logic inputs. A current source in the tail of the differential amplifier equalizes ONE (HIGH) and ZERO (LOW) level noise margins by removing the NOR side saturation knee, and also improves saturation temperature dependency.
Defining logic "ONE" as $-V_{OH}$ = 895 mV (typ.) and logic "ZERO" as $-V_{OL}$ = 1710 mV (typ.) the elements perform the logical NOR and OR functions (positive logic).
An input enable line common to all gates in each package is provided for additional logic flexibility.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134).

Supply voltage (d.c.)	$-V_{EE}$	max. 6.0 V
(peak value)	$-V_{EEM}$	max. 8.0 V
Input voltage		0 to −6.0 V
Output current		max. 40 mA
Storage temperature	T_{stg}	- 65 to + 150 °C
Operating ambient temperature	T_{amb}	0 to + 75 °C

CHARACTERISTICS (d.c.) at V_{CC} = ground; $-V_{EE}$ = 5.2 V

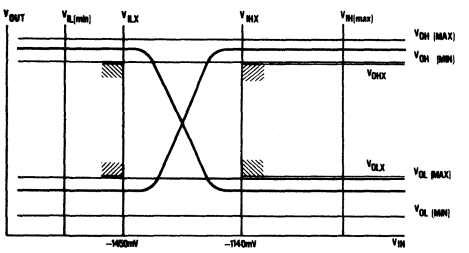
SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	0°C TYP.	0°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+75°C MIN.	+75°C TYP.	+75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage											$V_{IL} = -1700$ mV
	F.O. = 1 gate	−900	−850	−800	−900	−850	−800	−890	−840	−790	mV	for NOR gate
	F.O. = 5 gates	−940	−890	−840	−940	−890	−840	−940	−890	−840	mV	$V_{IH} = -900$ mV
	50 Ω to −2.0 V	−975	−925	−875	−975	−925	−875	−975	−925	−875	mV	for OR gate
V_{OL}	Output Low Voltage											$V_{IL} = -1700$ mV
	F.O. = 1 gate	−1745	−1670	−1595	−1745	−1670	−1595	−1745	−1670	−1595	mV	for OR gate
	F.O. = 5 gates	−1785	−1710	−1635	−1785	−1710	−1635	−1785	−1710	−1635	mV	$V_{IH} = -900$ mV
	50 Ω to −2.0 V	−1775	−1700	−1625	−1775	−1700	−1625	−1775	−1700	−1625	mV	for NOR gate
V_{OHX}	Output High Voltage at V_{IN} (threshold)											$V_{ILX} = -1450$ mV for NOR gate; $V_{IHX} = -1140$ mV for OR gate (To each input sequentially (other inputs open))
	F.O. = 1 gate	−910			−910			−900			mV	
	F.O. = 5 gates	−950			−950			−950			mV	
	50 Ω to −2.0 V	−985			−985			−985			mV	
V_{OLX}	Output Low Voltage at V_{IN} (threshold)											$V_{ILX} = -1450$ mV for OR gate; $V_{IHX} = -1140$ mV for NOR gate (To each input sequentially (other inputs open))
	F.O. = 1 gate			−1585			−1585			−1585	mV	
	F.O. = 5 gates			−1625			−1625			−1625	mV	
	50 Ω to −2.0 V			−1615			−1615			−1615	mV	

SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	0°C TYP.	0°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+75°C MIN.	+75°C TYP.	+75°C MAX.	UNITS	CONDITIONS
$I_{IN}(1)$	Input Current at V_{IH}											
	Standard Gate		2.30	3.15		2.25	3.10		2.15	3.00	mA	$V_{IH} = -900$ mV to each input sequentially
	Enable Lines											
	GHH121/9502		4.60	6.30		4.50	6.20		4.30	6.00	mA	
	GHH131/9503		6.90	9.45		6.75	9.30		6.45	9.00	mA	
	GHH141/9504		9.20	12.60		9.00	12.40		8.60	12.00	mA	
$I_{IN}(0)$	Input Current at V_{IL}											
	Standard Gate		1.80	2.40		1.75	2.35		1.65	2.25	mA	$V_{IL} = -1700$ mV to each input sequentially
	Enable Lines											
	GHH121/9502		3.60	4.80		3.50	4.70		3.30	4.50	mA	
	GHH131/9503		5.40	7.20		5.25	7.05		4.95	6.75	mA	
	GHH141/9504		7.20	9.60		7.00	9.40		6.60	9.00	mA	
I_{PD}	Power Supply Current											
	GHH121/9502	25	33	43	29	35	44	30	37	48	mA	All inputs open
	GHH131/9503	35	46	59	40	48	60	40	51	65	mA	
	GHH141/9504	40	52	67	45	54	68	41	57	74	mA	
ΔI_{IN}	Input Saturation Test									50	μA	$\Delta I_{IN} = I_B - I_A$; $I_A = I_{IN}$ @ $V_{IN} = 800$ mV; $I_B = I_{IN}$ @ $V_{IN} = 750$ mV

CHARACTERISTICS (continued) (a.c.) at V_{CC} = ground; $-V_{EE}$ = 5.2 V

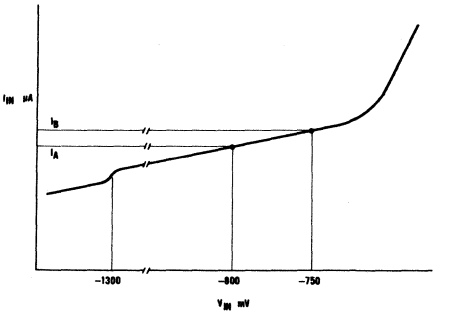
SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	0°C TYP.	0°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+75°C MIN.	+75°C TYP.	+75°C MAX.	UNITS	CONDITIONS
t_{pd}	Propagation Delay											
	t_{pd--}		2.3			2.3	3.5		2.5		ns	
	t_{pd++}		2.2			2.2	3.5		2.4		ns	$R_L = 50\,\Omega$ to -2.0 V
	t_{pd-+}		2.4			2.4	3.5		2.6		ns	$C_L < 5.0$ pF
	t_{pd+-}		2.5			2.5	3.2		2.7		ns	$t_r = t_f = 2.5$ ns
t_r	Rise Time	1.5		4.5	1.5	3.0	4.5	1.5		4.5	ns	$R_L = 50\,\Omega$ to -2.0 V $C_L < 5.0$ pF
t_f	Fall Time	1.5		4.5	1.5	3.0	4.5	1.5		4.5	ns	$R_L = 50\,\Omega$ to -2.0 V $C_L < 5.0$ pF
I_T	Transient Input Current											
	Standard Gate					2.5	3.5				mA	
	Enable Lines											
	GHH121/9502					3.4	4.5				mA	
	GHH131/9503					4.7	5.7				mA	
	GHH141/9504					5.0	6.0				mA	
t_{pd}	Propagation Delay											
	t_{pd--}		2.6			2.6	3.5		2.8		ns	
	t_{pd++}		2.5			2.5	3.5		2.7		ns	$R_L = 50\,\Omega$ to -2.0 V
	t_{pd-+}		2.7			2.7	3.5		2.9		ns	$C_L = 15$ pF ±5%
	t_{pd+-}		2.8			2.8	3.5		3.0		ns	$t_r = t_f = 2.5$ ns

Noise margin specification points



Corner points indicated on the transfer characteristics represent the worst case points (thresholds) at which the device will start to switch. The values V_{ILX} and V_{IHX} define the maximum width of the transition region.

Input saturation test

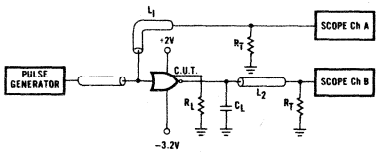


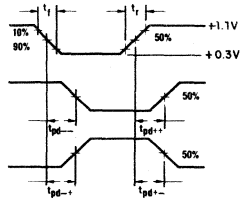
This test insures that the input transistor is not in saturation at $V_{IN} = 750$ mV. This represents a worst case condition with the driving gate at V_{OH} (min) = 750 mV (ie. for $T_A = 75$°C this is equivalent to driving gate into FO = 1 with its power supply at −5%).

Saturation is defined as no increase in collector current for 20% increase in base drive current I_R. The effect is to increase t_{pd}.

CHARACTERISTICS (continued)

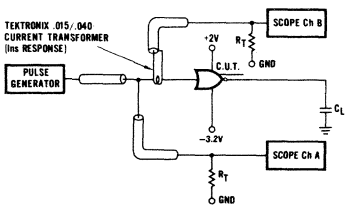
Switching times test circuit and waveforms

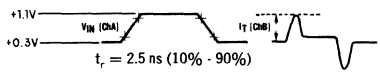




$t_r = t_f = 2.5$ ns (10% - 90%) Jig setup with no circuit under test
$V_{CC} = V_{CC}$ (AUX) $= +2.0$ V
$V_{EE} = -3.2$ V

Transient input current test circuit and waveforms





This test provides a measure of the average value of C_{IN}; also current mismatch in the line.
$V_{CC} = V_{CC}$ (AUX) $= +2.0$ V
$V_{EE} = -3.2$ V

Notes

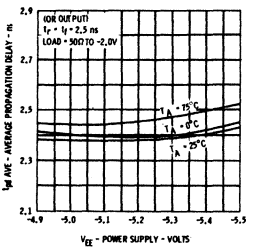
L_1 and L_2 are equal length 50 Ω impedance lines.
$R_L = R_T = 50$ Ω termination of scope.
C_L = jig and stray capacitance < 5.0pF

Logic levels for figures above are nominal values at 50 Ω fan-out determined by indicated power supplies. These values chosen to permit use of scope 50 Ω termination to ground. Decoupling 0.1 μF from ground to V_{EE}.

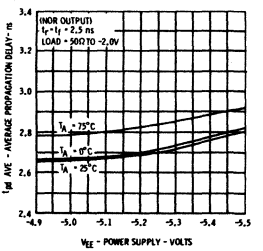
CHARACTERISTICS (continued)

TYPICAL AVERAGE PROPAGATION DELAY VERSUS POWER SUPPLY

TYPICAL AVERAGE PROPAGATION DELAY VERSUS POWER SUPPLY



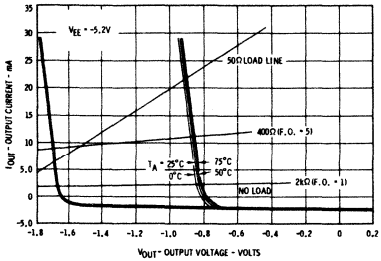
TYPICAL AVERAGE PROPAGATION DELAY VERSUS POWER SUPPLY



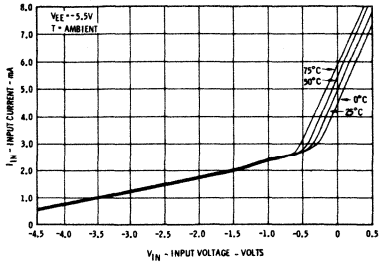
$$t_{pd\ ave} = \frac{t_{pd\ rising} + t_{pd\ falling}}{2}$$

CHARACTERISTICS (continued)

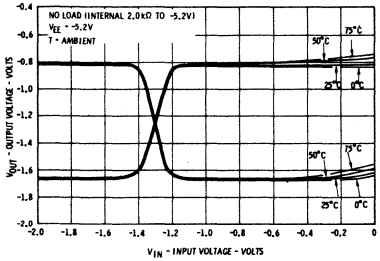
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE



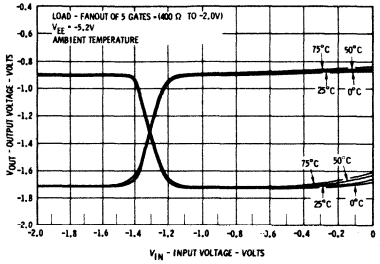
INPUT CURRENT VERSUS INPUT VOLTAGE



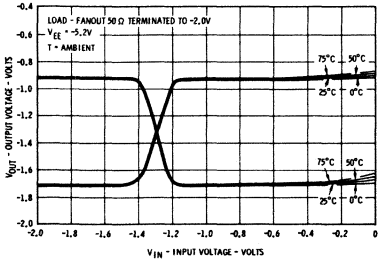
TRANSFER CHARACTERISTICS VERSUS AMBIENT TEMPERATURE



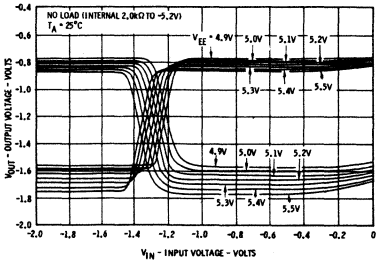
TRANSFER CHARACTERISTICS VERSUS AMBIENT TEMPERATURE



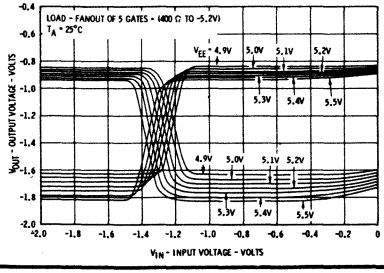
TRANSFER CHARACTERISTICS VERSUS AMBIENT TEMPERATURE



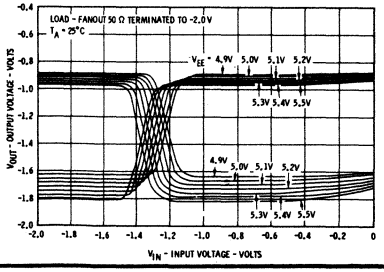
TRANSFER CHARACTERISTICS VERSUS POWER SUPPLY VARIATION



TRANSFER CHARACTERISTICS VERSUS POWER SUPPLY VARIATION



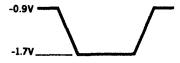
TRANSFER CHARACTERISTICS VERSUS POWER SUPPLY VARIATION



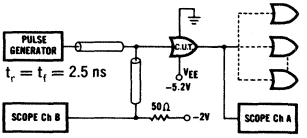
CHARACTERISTICS (continued)

TYPICAL PROPAGATION DELAY VERSUS FAN OUT

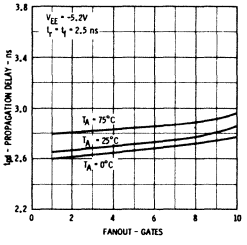
INPUT WAVEFORM



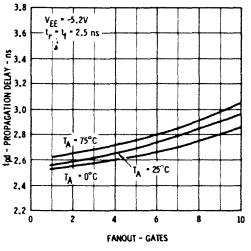
$t_r = t_f = 2.5$ ns (10% - 90%)



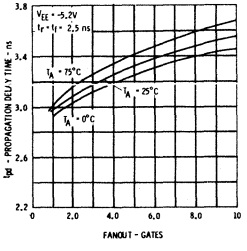
TYPICAL PROPAGATION DELAY VERSUS FANOUT t_{pd++} (OR output)



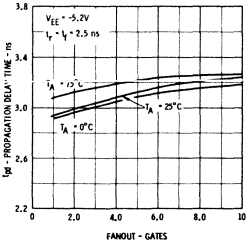
TYPICAL PROPAGATION DELAY VERSUS FANOUT t_{pd--} (OR output)



TYPICAL PROPAGATION DELAY VERSUS FANOUT t_{pd+-} (NOR output)



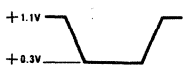
TYPICAL PROPAGATION DELAY VERSUS FANOUT t_{pd-+} (NOR output)



CHARACTERISTICS (continued)

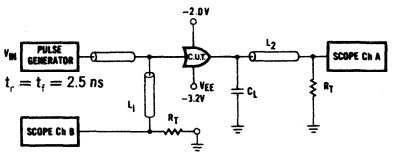
TYPICAL PROPAGATION DELAY VERSUS CAPACITIVE LOAD (in a 50 ohm system)

INPUT WAVEFORM

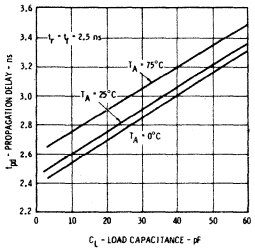


$t_r = t_f = 2.5$ ns (10% - 90%)

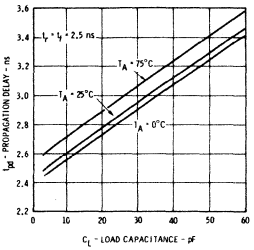
$V_{CC} = V_{CC}(AUX) = +2.0$ V
$V_{EE} = -3.2$ V
$R_T = 50\ \Omega$ Termination of scope
L_1 & L_2 = Equal length 50 Ω impedance lines



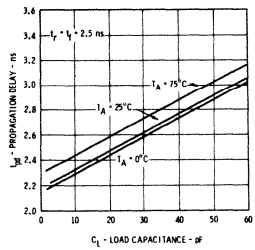
TYPICAL PROPAGATION DELAY VERSUS LOAD CAPACITANCE t_{pd+-} (NOR output)



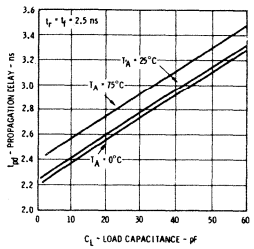
TYPICAL PROPAGATION DELAY VERSUS LOAD CAPACITANCE t_{pd-+} (NOR output)



TYPICAL PROPAGATION DELAY VERSUS LOAD CAPACITANCE t_{pd++} (OR output)



TYPICAL PROPAGATION DELAY VERSUS LOAD CAPACITANCE t_{pd--} (OR output)



OPERATING NOTES

Interconnection recommendations

All high speed CML circuits demand that special precautions be taken for optimum system performance. A ground plane must be provided for a good, low impedance, ground current return path and to transform interconnections into microstrip transmission lines. The voltage supply line should be well decoupled with small capacitors throughout each card between V_{EE} and the ground plane and by including at least one larger tantalum capacitor per card.

Typical microstrip lines have a characteristic impedance between 50 and 150 ohms with the lower being more desirable in CML systems. For local interconnects the internal 2 kΩ resistors provide adequate termination but for optimum performance lines longer than 15 cm in length should be terminated in their characteristic impedance.

Microstrip interconnections may be terminated by a resistor: $R = \frac{Z_o}{1 - NZ_o/2000}$ to a −2 V supply where Z_o is the characteristic impedance of the line and N is the number of loads. Alternately, a 2 resistor divider network may be used with $R_1 = 1.6\ R$ connected to ground and $R_2 = 2.6\ R$ connected to V_{EE}.

Coaxial cables or terminated twisted pairs of wire are required for backpanel interconnections longer than 10 cm.

Line driving capability

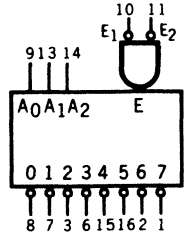
50 Ω coaxial cables properly terminated may be driven with almost no degradation in the waveform. The normal delay due to the finite speed of the signal traveling down the cable will be encountered in addition to a slight decrease in signal swing. The decrease caused by the attenuation of the cable will lower the noise immunity of the receiving circuit by the same amount.
Care must be exercised to ensure the ground potentials at the driving and receiving ends of a line are equal and no differential noise is present.

The GH family of CML silicon monolithic integrated circuits is designed for high speed instrumentation digital communication systems, central processors and computer terminals. All GH family elements incorporate a unique temperature compensation network which insures that significant parameters such as logic levels, noise margin and speed remain relatively constant over a wide temperature range.

The GHH151/9538 is a high speed one of eight decoder providing in one package the ability to activate any one of eight lines by the binary address of three input lines. In addition this device may be used as a demultiplexer by connecting data to the enable inputs.

Input and output pulldown resistors (2 kΩ) eliminate the necessity for external termination of lines up to 15 cm and unused logic inputs. Package pin locations are chosen to reduce internal noise generation and crosstalk. The GH family corresponds to the ECL9500 series.

ONE OF EIGHT DECODER



QUICK REFERENCE DATA				
Supply voltage	$-V_{EE}$		5.2	V
Operating ambient temperature range	T_{amb}		0 to +75	°C
Average propagation delay time from select input to output line	t_{pd}	typ.	4.0	ns
Output voltage HIGH state	$-V_{OH}$	nom.	880	mV
LOW state	$-V_{OL}$	nom.	1710	mV
Power consumption	P_{av}	typ.	275	mW

PACKAGE OUTLINE 16 lead ceramic dual in line (See General Section).

Note

V_{CC} = ground (pins 4 and 5)
$-V_{EE}$ = 5.2 V (pin 12)

FUNCTIONAL DESCRIPTION

The GHH151/9538 decoder accepts three binary address inputs and, under control of the enables, activates one of the eight active LOW outputs. Both of the active LOW enable input lines must be LOW to enable the outputs.
This decoder may be used as a demultiplexer by connecting a data source to one of the enable inputs. The other enable input will function as a data enable line while input A_0, A_1 and A_2 determine which of the eight output lines the data is fed to. The data will not be inverted through the demultiplexer since both the input and the outputs are active LOW. The delay through the demultiplexer from either enable input to an output is only two gate delays.

FUNCTION TABLE

INPUTS					OUTPUTS							
A_0	A_1	A_2	E_1	E_2	0	1	2	3	4	5	6	7
L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	L	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H
H	H	L	L	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	L	H	H	H	H	H	L	H	H
L	H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	L	H	H	H	H	H	H	H	L
X	X	X	H	L	H	H	H	H	H	H	H	H
X	X	X	L	H	H	H	H	H	H	H	H	H
X	X	X	H	H	H	H	H	H	H	H	H	H

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage (d.c.)	$-V_{EE}$	max. 6.0	V
(peak value)	$-V_{EEM}$	max. 8.0	V
Input voltage		0 to -6.0	V
Output current		max. 40	mA
Storage temperature		-65 to +150	°C
Operating ambient temperature		0 to +75	°C

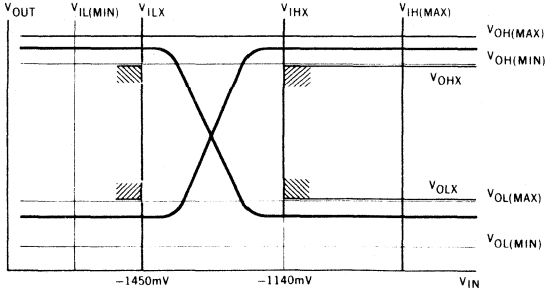
CHARACTERISTICS (d.c.) at V_{CC} = ground; $-V_{EE}$ = 5.2 V

SYMBOL	CHARACTERISTIC	LIMITS									UNITS	CONDITIONS
		0°C			+ 25°C			+ 75°C				
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
V_{OH}	Output High Voltage	-915	-850	-785	-915	-850	-785	-905	-840	-775	mV	FO = 1 Gate
		-955	-880	-805	-955	-880	-805	-955	-880	-805	mV	FO = 5 Gates
		-990	-915	-840	-990	-915	-840	-990	-915	-840	mV	R_L = 50 Ω to -2.0 V
V_{OL}	Output Low Voltage	-1755	-1670	-1585	-1755	-1670	-1585	-1755	-1670	-1585	mV	FO = 1 Gate
		-1795	-1710	-1625	-1795	-1710	-1625	-1795	-1710	-1625	mV	FO = 5 Gates
		-1785	-1700	-1615	-1785	-1700	-1615	-1785	-1700	-1615	mV	R_L = 50 Ω to -2.0 V
V_{OHX}	Output High Voltage at V_{IN} (Threshold) V_{IHX} or V_{ILX} Applied to each. Select Line Sequentially.	-925			-925			-915			mV	FO = 1 Gate
		-965			-965			-965			mV	FO = 5 Gates
		-1000			-1000			-1000			mV	R_L = 50 Ω to -2.0 V
V_{OLX}	Output Low Voltage at V_{IN} (Threshold) V_{IHX} or V_{ILX} Applied to each. Select Line Sequentially.			-1575			-1575			-1575	mV	FO = 1 Gate
				-1615			-1615			-1615	mV	FO = 5 Gates
				-1605			-1605			-1605	mV	R_L = 50 Ω to -2.0 V
$I_{IN(1)}$	Input Current at V_{IH}		2.30	3.15		2.25	3.10		2.15	3.00	mA	V_{IH} = -900 mV to each Input Sequentially
$I_{IN(0)}$	Input Current at V_{IL}		1.80	2.40		1.75	2.35		1.65	2.25	mV	V_{IL} = -1700 mV to each Input Sequentially
I_{PS}	Power Supply Current		50		42	53	71		57		mA	All Inputs Open

CHARACTERISTICS (a.c.) at V_{CC} = ground; $-V_{EE}$ = 5.2 V

SYMBOL	CHARACTERISTIC	LIMITS						UNIT	CONDITIONS
		0°C	25°C			75°C			
		TYP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
t_{pd}	Propagation Delay								
	Select Lines								R_L = 50 Ω to
	A_1	3.0		3.0	4.0		3.0		ns	Gnd
	A_0 & A_2	4.0		4.0	5.3		4.0		ns	$C_L \leq$ 5.0 pF
	Enable Lines	5.0		5.0	6.7		5.0		ns	$t_r = t_f$ = 2.5 ns
I_T	Transient Input Current			2.5	3.5				mA	

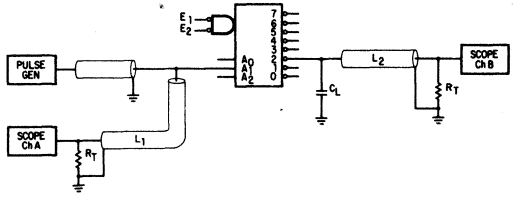
Noise margin specification points

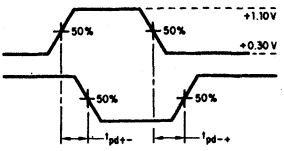


Corner points indicated on the transfer characteristics represent the worst case points (thresholds) at which the device will start to switch. The values V_{ILX} and V_{IHX} define the maximum width of the transition region.

CHARACTERISTICS (continued)

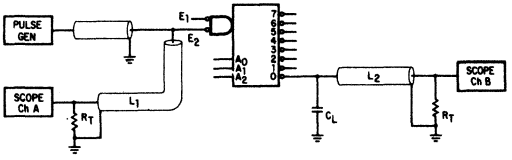
Switching times test circuit and waveforms

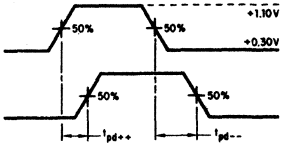




CONDITIONS
V_{CC} = + 2.0 V
V_{EE} = -3.2 V
R_L = 50 Ω = R_T (Scope input impedance)
C_L = jig and stray capacitance < 5 pF
L_1 = L_2 equal 50 Ω impedance lines
Input signal t_r = t_f = 2.5 ns (10% - 90%)
With no circuit under test

From select lines to output

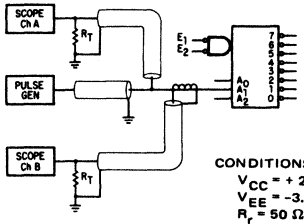


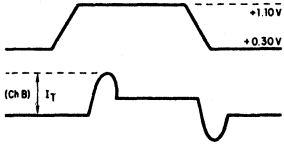


CONDITIONS
V_{CC} = + 2.0 V
V_{EE} = -3.2V
R_L = 50 Ω = R_T (Scope input impedance)
C_L = jig and stray capacitance < 5 pF
L_1 = L_2 equal 50 Ω impedance lines
Input signal t_r = t_f = 2.5 ns (10% - 90%)
With no circuit under test

From enable line to output

Transient input current test circuit and waveforms





This test provides a measure of the average value of C_{in}.

CONDITIONS
V_{CC} = + 2.0 V
V_{EE} = -3.2 V
R_r = 50 Ω (Scope input impedance)
Input signal t_r = t_f = 2.5 ns (10% - 90%)
With no circuit under test

OPERATING NOTES

Interconnection recommendations

All high speed CML circuits demand that special precautions be taken for optimum system performance. A ground plane must be provided for a good, low impedance, ground current return path and to transform interconnections into microstrip transmission lines. The voltage supply lines should be well decoupled with small capacitors throughout each card between V_{EE} and the ground plane and by including at least one larger tantalum capacitor per card.

Typical microstrip lines have a characteristic impedance between 50 and 150 ohms with the lower being more desirable in CML systems. For local interconnects the internal 2 kΩ resistors provide adequate termination but for optimum performance lines longer than 15 cm in length should be terminated in their characteristic impedance.

Microstrip interconnections may be terminated by a resistor: $R = \frac{Z_o}{1 - NZ_o/2000}$ to a −2 V supply where Z_o is the characteristic impedance of the line and N is the number of loads. Alternately, a 2 resistor divider network may be used with $R_1 = 1.6$ R connected to ground and $R_2 = 2.6$ R connected to V_{EE}.

Coaxial cables or terminated twisted pairs of wire are required for backpanel interconnections longer than 10 cm.

Line driving capability

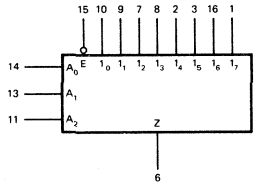
50 Ω coaxial cables properly terminated may be driven with almost no degradation in the waveform. The normal delay due to the finite speed of the signal traveling down the cable will be encountered in addition to a slight decrease in signal swing. The decrease caused by the attenuation of the cable will lower the noise immunity of the receiving circuit by the same amount.
Care must be exercised to ensure the ground potentials at the driving and receiving ends of a line are equal and no differential noise is present.

The GH family of CML silicon monolithic integrated circuits is designed for high speed instrumentation, digital communication system, central processors and computer terminals. All GH family elements incorporate a unique temperature compensation network which insures that significant parameters such as logic levels, noise margin and speed remain relatively constant over a wide temperature range.

The GHH161/9581 is a high speed eight input multiplexer providing in one package the ability to select one bit of data from up to eight sources.
In addition, the GHH161/9581 can be used as a universal function generator to generate any logic function of four variables.

Input and output pull-down resistors (2 kΩ) eliminate the necessity for external termination of lines up to 15 cm and unused logic inputs. Package pin locations are chosen to reduce internal noise generation and crosstalk. The GH family corresponds to the ECL9500 series.

EIGHT INPUT MULTIPLEXER



QUICK REFERENCE DATA				
Supply voltage	$-V_{EE}$		5.2	V
Operating ambient temperature range	T_{amb}		0 to + 75	°C
Average propagation delay time from data input to output	t_{pd}	typ.	3.2	ns
Output voltage HIGH state	$-V_{OH}$	nom.	890	mV
LOW state	$-V_{OL}$	nom.	1710	mV
Power consumption	P_{av}	typ.	260	mW

PACKAGE OUTLINE 16 lead ceramic dual in line (See General Section).

Note

V_{CC} = ground (pins 4 and 5)
$-V_{EE}$ = 5.2 V (pin 12)

FUNCTIONAL DESCRIPTION

The GHH161/9581 is fundamentally a high speed semiconductor implementation of a single-pole eight-position switch. Three address lines select one out of the eight data inputs and feed this input to the output (Z). An active LOW enable forces the output LOW if held HIGH. Data encounters only one gate delay from one of the eight inputs to the output. As the GHH161/9581 provides the ability to select from or sequence eight data sources, it may therefore be used as a parallel to serial converter by sequentially advancing through the input address combinations.
The device may also be used as a universal logic element capable of generating any function of four variables by proper manipulation of the inputs. The wired-OR outputs and the input enable permit easy expansion of several GHH161/9581 types to form multiplexers with more than eight inputs.

LOGIC FUNCTIONS

$$Z = E \cdot (I_0 \cdot \bar{A}_0 \cdot \bar{A}_1 \cdot \bar{A}_2 + I_1 \cdot A_0 \cdot \bar{A}_1 \cdot \bar{A}_2 + I_2 \cdot \bar{A}_0 \cdot A_1 \cdot \bar{A}_2 + I_3 \cdot A_0 \cdot A_1 \cdot \bar{A}_2 +$$
$$+ I_4 \cdot \bar{A}_0 \cdot \bar{A}_1 \cdot A_2 + I_5 \cdot A_0 \cdot \bar{A}_1 \cdot A_2 + I_6 \cdot \bar{A}_0 \cdot A_1 \cdot A_2 + I_7 \cdot A_0 \cdot A_1 \cdot A_2)$$

Since the enable is an active LOW input, the E in the equation implies pin 15 must be LOW to activate Z.

Function table

INPUTS											OUTPUT
A_0	A_1	A_2	$\bar{E}$	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	Z
L	L	L	L	L	X	X	X	X	X	X	X	L
L	L	L	L	H	X	X	X	X	X	X	X	H
H	L	L	L	X	L	X	X	X	X	X	X	L
H	L	L	L	X	H	X	X	X	X	X	X	H
L	H	L	L	X	X	L	X	X	X	X	X	L
L	H	L	L	X	X	H	X	X	X	X	X	H
H	H	L	L	X	X	X	L	X	X	X	X	L
H	H	L	L	X	X	X	H	X	X	X	X	H
L	L	H	L	X	X	X	X	L	X	X	X	L
L	L	H	L	X	X	X	X	H	X	X	X	H
H	L	H	L	X	X	X	X	X	L	X	X	L
H	L	H	L	X	X	X	X	X	H	X	X	H
L	H	H	L	X	X	X	X	X	X	L	X	L
L	H	H	L	X	X	X	X	X	X	H	X	H
H	H	H	L	X	X	X	X	X	X	X	L	L
H	H	H	L	X	X	X	X	X	X	X	H	H
X	X	X	H	X	X	X	X	X	X	X	X	L

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage (d.c.)	$-V_{EE}$	max.	6.0	V
(peak value)	$-V_{EEM}$	max.	8.0	V
Input voltage			0 to -6.0	V
Output current		max.	40	mA
Storage temperature	T_{stg}		-65 to + 150	°C
Operating ambient temperature	T_{amb}		0 to +75	°C

CHARACTERISTICS (d.c.) at V_{CC} = ground; $-V_{EE}$ = 5.2 V

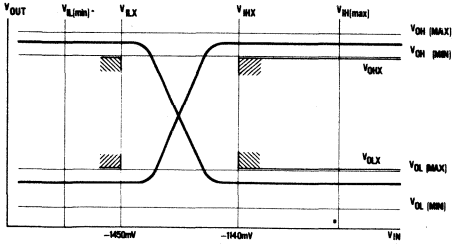
SYMBOL	CHARACTERISTIC	LIMITS									UNITS	CONDITIONS
		0°C			+25°C			+75°C				
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
V_{OH}	Output High Voltage	−905	−850	−795	−905	−850	−795	−895	−840	−785	mV	FO = 1 Gate
		−945	−890	−835	−945	−890	−835	−945	−890	−835	mV	FO = 5 Gates
		−980	−925	−870	−980	−925	−870	−980	−925	−870	mV	R_L = 50 Ω to −2.0 V
V_{OL}	Output Low Voltage	−1755	−1670	−1585	−1755	−1670	−1585	−1755	−1670	−1585	mV	FO = 1 Gate
		−1795	−1710	−1625	−1795	−1710	−1625	−1795	−1710	−1625	mV	FO = 5 Gates
		−1785	−1700	−1615	−1785	−1700	−1615	−1785	−1700	−1615	mV	R_L = 50 Ω to −2.0 V
V_{OHX}	Data Lines Output High Voltage at V_{in} = −1140 mV	−915			−915			−905			mV	FO = 1 Gate
		−955			−955			−955			mV	FO = 5 Gates
		−990			−990			−990			mV	R_L = 50 Ω to −2.0 V
V_{OLX}	Data Lines Output Low Voltage at V_{in} = −1450 mV			−1575			−1575			−1575	mV	FO = 1 Gate
				−1615			−1615			−1615	mV	FO = 5 Gates
				−1605			−1605			−1605	mV	R_L = 50 Ω to −2.0 V
V_{IHX}	Select Lines Input High Threshold Voltage	−1140			−1140			−1140			mV	Guaranteed Input High Voltage
V_{ILX}	Select Lines Input Low Voltage			−1450			−1450			−1450	mV	Guaranteed Input Low Voltage
$I_{IN(I)}$	Input Current at V_{IH}		2.30	3.15		2.25	3.10		2.15	3.00	mA	V_{IH} = −900 mV to each Input Sequentially
$I_{IN(0)}$	Input Current at V_{IL}		1.80	2.40		1.75	2.35		1.65	2.25	mA	V_{IL} = −1700 mV to each Input Sequentially
I_{PS}	Power Supply Current		48		40	50	67		55		mA	All Inputs Open

CHARACTERISTICS (a.c.) at V_{CC} = ground; $-V_{EE}$ = 5.2 V

SYMBOL	CHARACTERISTIC	LIMITS							UNIT	CONDITIONS
		0°C	25°C			75°C				
		TYP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
t_{pd}	Propagation Delay									
	Data Lines	3.2		3.2	4.3		3.2		ns	R_L = 50 Ω to Gnd
	Select Lines	5.5		5.5	7.5		5.5		ns	C_L < 5.0 pF
	Enable Lines	3.5		3.5	4.8		3.5		ns	$t_r = t_f$ = 2.5 ns
I_T	Transient Input Current			2.5	3.5				mA	

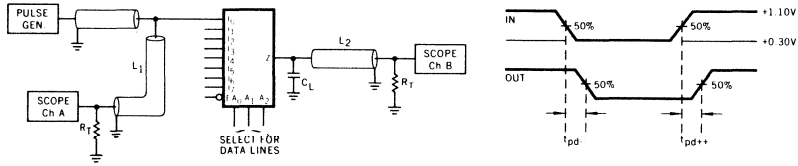
CHARACTERISTICS (continued)

Noise margin specification points



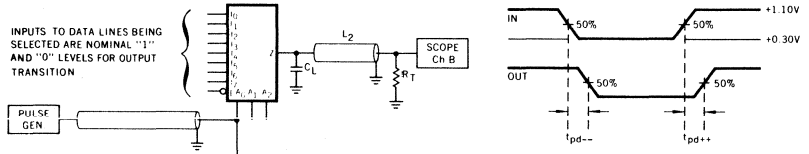
Corner points indicated on the transfer characteristics represent the worst case points (thresholds) at which the device will start to switch. The values V_{ILX} and V_{IHX} define the maximum width of the transition region.

Switching times test circuits and waveforms



CONDITIONS
$V_{CC} = +2.0$ V
$V_{EE} = -3.2$ V
$R_L = 50\ \Omega = R_T$ (Scope input impedance)
C_L = jig and stray capacitance <5 pF
$L_1 = L_2$ equal 50 Ω impedance lines
Input signal $t_r = t_f = 2.5$ ns (10% - 90%)
With no circuit under test

From data lines to output

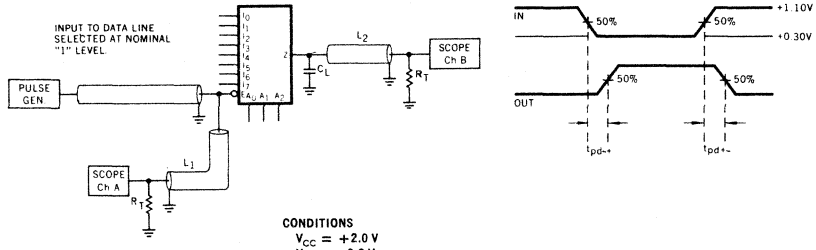


CONDITIONS
$V_{CC} = +2.0$ V
$V_{EE} = -3.2$ V
$R_L = 50\ \Omega = R_T$ (Scope input impedance)
C_L = jig and stray capacitance <5 pF
$L_1 = L_2$ equal 50 Ω impedance lines
Input signal $t_r = t_f = 2.5$ ns (10% - 90%)
With no circuit under test

From select lines to output

CHARACTERISTICS (continued)

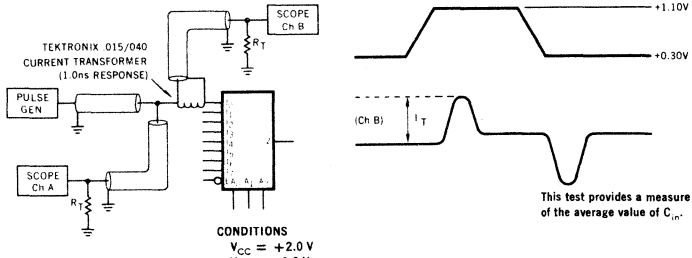
Switching times test circuits and waveforms (continued)



CONDITIONS
V_{CC} = +2.0 V
V_{EE} = −3.2 V
R_L = 50 Ω = R_T (Scope input impedance)
C_L = jig and stray capacitance <5 pF
L_1 = L_2 equal 50 Ω impedance lines
Input signal t_r = t_f = 2.5 ns (10% - 90%)
With no circuit under test

From enable to output

Transient input current test circuit and waveforms



This test provides a measure of the average value of C_{in}.

CONDITIONS
V_{CC} = +2.0 V
V_{EE} = −3.2 V
R_T = 50 Ω (Scope input impedance)
Input signal t_r = t_f = 2.5 ns (10% - 90%)
With no circuit under test

OPERATING NOTES

Interconnection recommendations

All high speed CML circuits demand that special precautions be taken for optimum system performance. A groundplane must be provided for a good, low impedance, ground current return path and to transform interconnections into microstrip transmission lines. The voltage supply lines should be well decoupled with small capacitors throughout each card between V_{EE} and the ground plane and by including at least one larger tantalum capacitor per card.

Typical microstrip lines have a characteristic impedance between 50 and 150 ohms with the lower being more desirable in CML systems. For local interconnects the internal 2 kΩ resistors provide adequate termination but for optimum performance lines longer than 15 cm in length should be terminated in their characteristic impedance.

Microstrip interconnections may be terminated by a resistor: $R = \frac{Z_o}{1 - NZ_o/2000}$ to a −2 V supply where Z_o is the characteristic impedance of the line and N is the number of loads. Alternately, a 2 resistor divider network may be used with $R_1 = 1.6\ R$ connected to ground and $R_2 = 2.6\ R$ connected to V_{EE}.

Coaxial cables or terminated twisted pairs of wire are required for backpanel interconnections longer than 10 cm.

Line driving capability

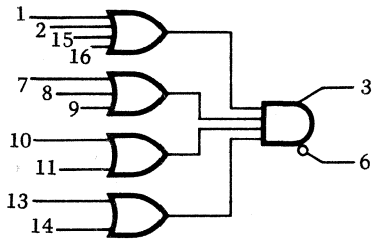
50 Ω coaxial cables properly terminated may be driven with almost no degradation in the waveform. The normal delay due to the finite speed of the signal traveling down the cable will be encountered in addition to a slight decrease in signal swing. The decrease caused by the attenuation of the cable will lower the noise immunity of the receiving circuit by the same amount.
Care must be exercised to ensure the ground potentials at the driving and receiving ends of a line are equal and no differential noise is present.

The GH family of CML silicon monolithic integrated circuits is designed for high speed instrumentation, digital communication systems, central processors and computer terminals. All GH family elements incorporate a unique temperature compensation network which insures that significant parameters such as logic levels, noise margin and speed remain relatively constant over a wide temperature range.

The GHH171/9505 is an OR-AND gate achieving slightly over one basic gate delay the AND of four different ORed functions. The NOR output of the four OR gates are ORed to derive the OR-NAND function.

Input and output pull-down resistors (2 kΩ) eliminate the necessity for external termination of lines up to 15 cm and unused logic inputs. Package pin locations are chosen to reduce internal noise generation and crosstalk. The GH family corresponds to the ECL9500 series.

FOUR WIDE OR-AND/OR-NAND GATE



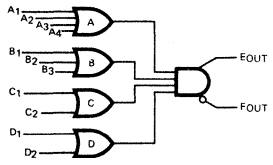
QUICK REFERENCE DATA				
Supply voltage	$-V_{EE}$		5.2	V
Operating ambient temperature range	T_{amb}		0 to + 75	°C
Average propagation delay time	t_{pd}	typ.	2.7	ns
Output voltage HIGH state	$-V_{OH}$	nom.	885	mV
LOW state	$-V_{OL}$	nom.	1760	mV
Power consumption	P_{av}	typ.	315	mW

PACKAGE OUTLINE 16 lead ceramic dual in-line (See General Section).

Note

V_{CC} = ground (pins 4 and 5)
$-V_{EE}$ = 5.2 V (pin 12)

LOGIC DIAGRAM



LOGIC FUNCTION

$E = A_N \cdot B_N \cdot C_N \cdot D_N$

$F = \overline{A_N \cdot B_N \cdot C_N \cdot D_N}$

Where:

$A_N = A_1 + A_2 + A_3 + A_4$.

$B_N = B_1 + B_2 + B_3$

$C_N = C_1 + C_2$

$D_N = D_1 + D_2$

FUNCTIONAL DESCRIPTION

The GHH171/9505 OR-AND gate combines two of the most often used functions in logic into one package to obtain maximum utilization of power and pin connections with minimum logic delay.

The AND of four OR gates is obtained by connecting the four collectors of the OR gates together with one collector load resistor and one emitter follower output device. High speed and temperature compensated output levels are maintained by a special controlled clamp at the collectors. This prevents saturation and loss of noise immunity as different logic conditions are encountered.

The NAND function is obtained by connecting the four NOR output emitter followers together at the output. In this way, maximum speed is maintained with optimum use of package pins. This output is temperature compensated by an additional pull-down transistor on each NOR gate collector.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134).

Supply voltage (d.c.)	$-V_{EE}$	max.	6.0	V
(peak value)	$-V_{EEM}$	max.	8.0	V
Input voltage			0 to -6.0	V
Output current		max.	40	mA
Storage temperature	T_{stg}		-65 to + 150	°C
Operating ambient temperature	T_{amb}		0 to + 75	°C

CHARACTERISTICS (d.c.) at V_{CC} = ground; $-V_{EE}$ = 5.2 V; T_{amb} = 0 to +75 °C

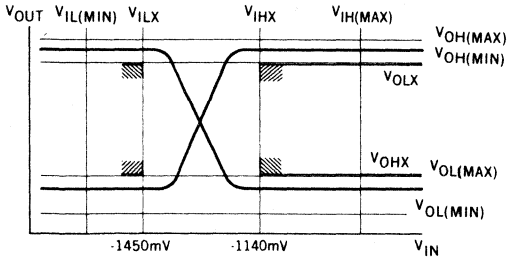
SYMBOL	CHARACTERISTIC	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	CONDITIONS	
V_{OH}	Output Voltage High	−920	−850	−770	mV	F.O. = 1 Gate	$V_{IN} = V_{IH}$ = −900 mV
		−960	−885	−790	mV	F.O. = 5 Gates	
		−995	−905	−805	mV	R_L = 50 Ω to −2.0 V	
$V_{OL(OR-AND)}$	Output Voltage Low	−2055	−1750	−1595	mV	F.O. = 1 Gate	$V_{IN} = V_{IL}$ = −1700 mV
		−2055	−1760	−1630	mV	F.O. = 5 Gates	
		−2055	−1755	−1625	mV	R_L = 50 Ω to −2.0 V	
$V_{OL(OR-NAND)}$	Output Voltage Low	−1805	−1750	−1595	mV	F.O. = 1 Gate	$V_{IN} = V_{IH}$ = −900 mV
		−1825	−1760	−1630	mV	F.O. = 5 Gates	
		−1815	−1755	−1625	mV	R_L = 50 Ω to −2.0 V	
V_{OHX}	Output Voltage High	−1005			mV	R_L = 50 Ω to −2.0 V	$V_{IN} = V_{IHX}$ = −1140 V for OR-AND $V_{IN} = V_{ILX}$ = −1450 V for OR-NAND
V_{OLX}	Output Voltage Low			−1615	mV	R_L = 50 Ω to −2.0 V	$V_{IN} = V_{ILX}$ = −1450 V for OR-AND $V_{IN} = V_{IHX}$ = −1140 V for OR-NAND
V_{IHX}	Input High Threshold Voltage	−1140			mV	Guaranteed Input High Voltage	
V_{ILX}	Input Low Threshold Voltage			−1450	mV	Guaranteed Input Low Voltage	
$I_{IN(1)}$	Input Current at V_{IH}			3.15	mA	V_{IH} = −900 mV to Each Input Sequentially	
$I_{IN(0)}$	Input Current at V_{IL}			2.40	mA	V_{IL} = −1700 mV to Each Input Sequentially	
I_{PS}	Power Supply Current	43	61	81	mA	All Inputs Open	

CHARACTERISTICS (a.c.) at V_{CC} = ground; $-V_{EE}$ = 5.2 V

SYMBOL	CHARACTERISTIC	LIMITS 0°C TYP	LIMITS 25°C MIN	LIMITS 25°C TYP	LIMITS 25°C MAX	LIMITS 75°C MIN	LIMITS 75°C TYP	LIMITS 75°C MAX	UNITS	CONDITIONS
	Propagation Delay									
t_{pd}	t_{pd++}	2.8		2.8	3.7		2.8		ns	R_L = 50 Ω to −2.0 V
	t_{pd--}	2.5		2.5	3.3		2.5		ns	C_L = 5.0 pF
	t_{pd+-}	2.4		2.4	3.2		2.4		ns	$t_r = t_f$ = 2.5 ns
	t_{pd-+}	2.4		2.4	3.2		2.4		ns	
I_T	Transient Input Current			2.0	3.5				mA	

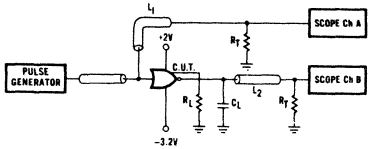
CHARACTERISTICS (continued)

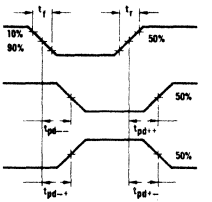
Noise margin specification points



Corner points indicated on the transfer characteristics represent the worst case points (thresholds) at which the device will start to switch. The values V_{ILX} and V_{IHX} define the maximum width of the transition region.

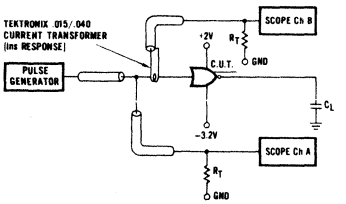
Switching times test circuit and waveforms

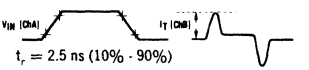




L_1 and L_2 = equal length 50 Ω impedance lines
$R_L = R_T$ = 50 Ω Termination of Scope
C_L = Jig and Stray Capacitance < 5.0 pF
$t_r = t_f$ = 2.5 ns (10% - 90%) Jig setup with no circuit under test
$V_{CC} = V_{CC}$ (AUX) = +2.0 V
V_{EE} = −3.2 V

Transient input current test circuit and waveforms

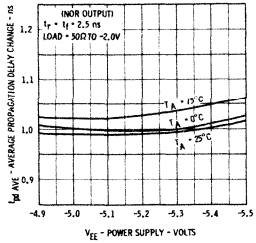




This test provides a measure of the average value of C_{IN}; also current mismatch in the line.
$V_{CC} = V_{CC}$ (AUX) = +2.0 V
V_{EE} = −3.2 V

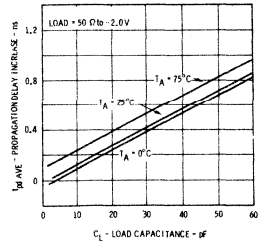
CHARACTERISTICS (continued)

TYPICAL AVERAGE PROPAGATION DELAY CHANGE VERSUS POWER SUPPLY



$$t_{pd\ AVE} = \frac{t_{pd\ rising} + t_{pd\ falling}}{2}$$

TYPICAL PROPAGATION DELAY INCREASE VERSUS LOAD CAPACITANCE t_{pd} AVE (OR output)



APPLICATION INFORMATION

Logic equations

The GHH171/9505 is useful in implementing a large variety of logic equations with minimum propagation delay. As an example the equation for carry lookahead is:

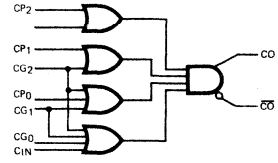
$CO = CG_2 + CG_1 \cdot CP_2 + CG_0 \cdot CP_1 \cdot CP_2 + C_{IN} \cdot CP_0 \cdot CP_1 \cdot CP_2$

An equivalent form of this equation is:

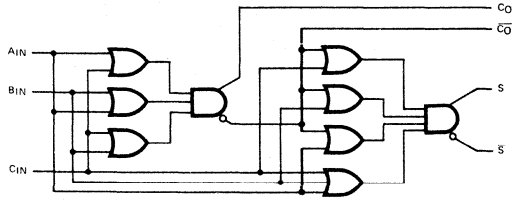
$\overline{CO} = \overline{CP_2} + \overline{CG_2} \cdot \overline{CP_1} + \overline{CG_1} \cdot \overline{CG_2} \cdot \overline{CP_0} + \overline{CG_0} \cdot \overline{CG_1} \cdot \overline{CG_2} \cdot \overline{C_{IN}}$

By DeMorgan's theorem this may be written as:

$CO = CP_2 \cdot (CG_2 + CP_1)\ (CG_1 + CG_2 + CP_0)\ (CG_0 + CG_1 + CG_2 + C_{IN})$



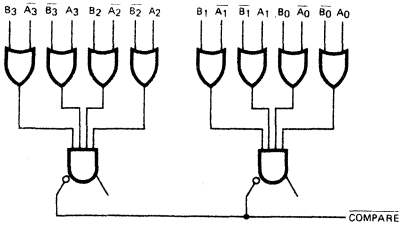
Adder



Two GHH171/9505 types may be used to build a fast full adder

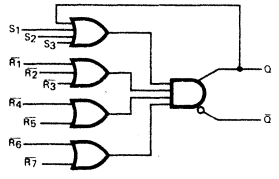
APPLICATION INFORMATION (continued)

Compare circuit

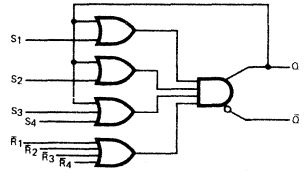


GHH171/9505 types may be used to generate a compare circuit capable of handling two bit per GHH171/9505.

Latches



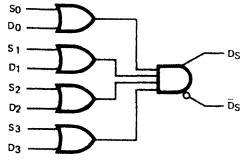
$S = S_1 + S_2 + S_3$ $\quad \bar{R} = (\bar{R}_1 + \bar{R}_2 + \bar{R}_3)(\bar{R}_4 + \bar{R}_5)(\bar{R}_6 + \bar{R}_7)$ $\quad R = R_1 \cdot R_2 \cdot R_3 + R_4 \cdot R_5 + R_6 \cdot R_7$



$S = S_1 \cdot S_2 \cdot (S_3 + S_4)$ $\quad \bar{R} = (\bar{R}_1 + \bar{R}_2 + \bar{R}_3 + \bar{R}_4)$ $\quad R = R_1 \cdot R_2 \cdot R_3 \cdot R_4$

The GHH171/9505 may be used to store one bit of information by connecting it as a latch. Many configuration of set and reset inputs are possible.

Multiplexer



The GHH171/9505 may be used as a 4-input multiplexer. A logic "0" on the selected S_N will allow D_N to be selected.
All other S_N must be a logic "1".

OPERATING NOTES

Interconnection recommendations

All high speed CML circuits demand that special precautions be taken for optimum system performance. A ground plane must be provided for a good, low impedance, ground current return path and to transform interconnections into microstrip transmission lines. The voltage supply lines should be well decoupled with small capacitors throughout each card between V_{EE} and the ground plane and by including at least one larger tantalum capacitor per card.

Typical microstrip lines have a characteristic impedance between 50 and 150 ohms with the lower being more desirable in CML systems. For local interconnects the internal 2 kΩ resistors provide adequate termination but for optimum performance lines longer than 15 cm in length should be terminated in their characteristic impedance.

Microstrip interconnections may be terminated by a resistor: $R = \frac{Z_o}{1 - NZ_o/2000}$ to a −2 V supply where Z_o is the characteristic impedance of the line and N is the number of loads. Alternately, a 2 resistor divider network may be used with $R_1 = 1.6\ R$ connected to ground and $R_2 = 2.6\ R$ connected to V_{EE}.

Coaxial cables or terminated twisted pairs of wire are required for backpanel interconnections longer than 10 cm.

Line driving capability

50 Ω coaxial cables properly terminated may be driven with almost no degradation in the waveform. The normal delay due to the finite speed of the signal traveling down the cable will be encountered in addition to a slight decrease in signal swing. The decrease caused by the attenuation of the cable will lower the noise immunity of the receiving circuit by the same amount.
Care must be exercised to ensure the ground potentials at the driving and receiving ends of a line are equal and no differential noise is present.

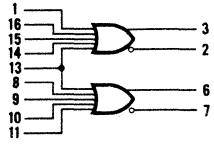
The GH family of CML silicon monolithic integrated circuits is designed for high speed instrumentation, digital communication systems, central processors and computer terminals. All GH family elements incorporate a unique temperature compensation network which insures that significant parameters such as logic levels, noise margin and speed remain relatively constant over a wide temperature range.

The GHH181/95H02, GHH191/95H03 and GHH201/95H04 are OR/NOR high speed gates employing a non-saturating current switch emitter follower configuration.

Input and output pull-down resistors (2 kΩ) eliminate the necessity for external termination of lines up to 15 cm and unused logic inputs. Package pin locations are chosen to reduce internal noise generation and crosstalk. The GH family corresponds to the ECL9500 series.

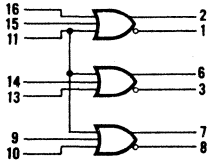
HIGH SPEED OR/NOR GATES

GHH181/95H02



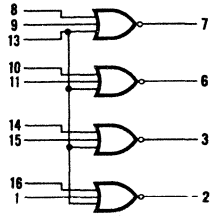
Dual 4-input OR/NOR with enable input

GHH191/95H03



Triple 2-input OR/NOR with enable input

GHH201/95H04



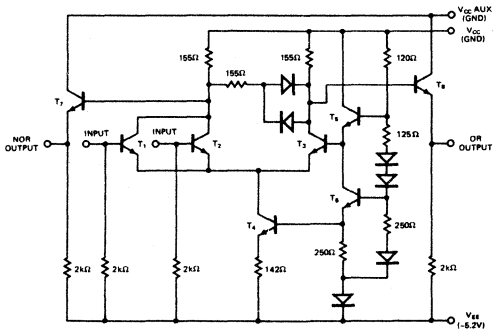
Quadruple 2-input OR/NOR with enable input

QUICK REFERENCE DATA				
Supply voltage	$-V_{EE}$		5.2	V
Operating ambient temperature range	T_{amb}		0 to + 75	°C
Average propagation delay time	t_{pd}		1.7	ns
Output voltage HIGH state	$-V_{OH}$	nom.	910	mV
LOW state	$-V_{OL}$	nom.	1740	mV
Power consumption per gate				
GHH181/95H02	P_{av}	typ.	88	mW
GHH191/95H03	P_{av}	typ.	85	mW
GHH201/95H04	P_{av}	typ.	81	mW

PACKAGE OUTLINE 16 lead ceramic dual in-line (See General Section).

Note
$\overline{V_{CC}}$ = ground (pins 4 and 5)
$-V_{EE}$ = 5.2 V (pin 12)

CIRCUIT DIAGRAM



FUNCTIONAL DESCRIPTION

The GH gates are based on the conventional emitter coupled configuration. Additional circuit complexity is incorporated to improve system operating characteristics. This includes temperature compensation networks to insure that logic levels and thresholds, set by the on chip bias driver are essentially independent of temperature. On chip output emitter follower and input pull-down resistors (2 kΩ) reduce external components normally required for short line termination and unused logic inputs. A current source in the tail of the differential amplifier equalizes ONE (HIGH) and ZERO (LOW) level noise margins by removing the NOR side saturation knee, and also improves saturation temperature dependency.

Defining logic "ONE" as $-V_{OH}$ = 910 mV (typ.) and logic "ZERO" as $-V_{OL}$ = 1740 mV (typ.), the elements perform the logical NOR and OR functions (positive logic).

An input enable line common to all gates in each package is provided for additional logic flexibility.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage (d.c.)	$-V_{EE}$	max.	6.0	V
(peak value)	$-V_{EEM}$	max.	8.0	V
Input voltage			0 to − 6.0	V
Output current		max.	40	mA
Storage temperature	T_{stg}		−65 to + 150	°C
Operating ambient temperature	T_{amb}		0 to + 75	°C

CHARACTERISTICS (d.c.) at V_{CC} = ground; $-V_{EE}$ = 5.2 V; T_{amb} = 0 to +75 °C

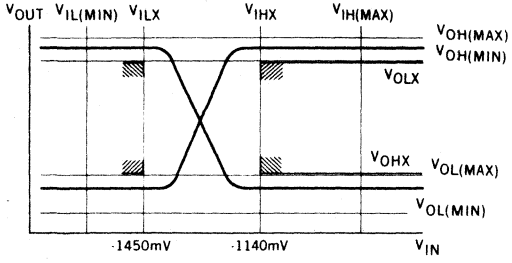
SYMBOL	CHARACTERISTIC	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS		CONDITIONS
V_{OH}	Output Voltage High		−860 −910 −950		mV	FO = 1 Gate FO = 5 Gates 50 Ω to −2.0 V	$V_{IN} = V_{IL}$ = −1700 mV for NOR Gate $V_{IN} = V_{IH}$ = −900 mV for OR Gate
V_{OL}	Output Voltage Low		−1690 −1740 −1720		mV	FO = 1 Gate FO = 5 Gates 50 Ω to −2.0 V	$V_{IN} = V_{IH}$ = −900 mV for NOR Gate $V_{IN} = V_{IL}$ = −1700 mV for OR Gate
V_{OHX}	Output Voltage High at $V_{IN} = V_{IX}$ (Threshold)	−930 −970 −1010			mV	FO = 1 Gate FO = 5 Gates 50 Ω to −2.0 V	$V_{IN} = V_{ILX}$ = −1450 mV for NOR Gate $V_{IN} = V_{IHX}$ = −1140 mV for OR Gate
V_{OLX}	Output Voltage Low at $V_{IN} = V_{IX}$ (Threshold)			−1605 −1655 −1635	mV	FO = 1 Gate FO = 5 Gates 50 Ω to −2.0 V	$V_{IN} = V_{ILX}$ = −1450 mV for OR Gate $V_{IN} = V_{IHX}$ = −1140 mV for NOR Gate
V_{IHX}	Guaranteed Input High Threshold Voltage	−1140			mV		Guaranteed Input High Threshold Voltage
V_{ILX}	Guaranteed Input Low Threshold Voltage			−1450	mV		Guaranteed Input Low Threshold Voltage
$V_{IN(H)}$	Input Current High		2.40	3.58	mA		V_{IN} = −900 mV to Common Enable Input
$V_{IN(H)}$	Input Current High		2.25	3.16	mA		V_{IN} = −900 mV to Other Inputs Sequentially
$V_{IN(L)}$	Input Current Low		1.75	2.46	mA		V_{IN} = −1700 mV to Each Input Sequentially
I_{PS}	Power Supply Current GHH181/95H02 GHH191/95H03 GHH201/95H04	 26 36 48	 34 49 62	 45 64 80	mA		All Inputs & Outputs Open

CHARACTERISTICS (a.c.) at V_{CC} = ground; $-V_{EE}$ = 5.2 V

SYMBOL	CHARACTERISTIC	LIMITS 0°C TYP.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 75°C TYP.	UNITS	CONDITIONS
t_{pd}	Propagation Delay 10% − 50%						ns	
	t_{pd} − −	1.6	−	1.6	2.4	1.8		R_L = 50 Ω to −2 V
	t_{pd} + +	1.7	−	1.7	2.4	1.9		C_L <5 pF
	t_{pd} − +	1.6	−	1.6	2.4	1.8		$t_r = t_f$ = 2.2 ns (10 − 90%)
	t_{pd} + −	1.8	−	1.8	2.4	2.0		
t_f	Fall Time 10% − 90%	2.2	1.4	2.2	3.0	2.2	ns	
t_r	Rise Time 10% − 90%	2.2	1.4	2.2	3.0	2.2		

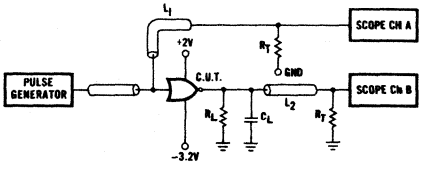
CHARACTERISTICS (continued)

Noise margin specification points

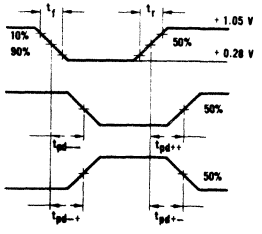


Corner points indicated on the transfer characteristics represent the worst case points (thresholds) at which the device will start to switch. The values V_{ILX} and V_{IHX} define the maximum width of the transition region.

Switching times test circuit and waveforms



L_1 and L_2 = equal length 50 Ω impedance lines
$R_L = R_T$ = 50 Ω Termination of Scope
C_L = Jig and Stray Capacitance <5.0 pF



$t_r = t_f$ = 2.4 ns (10% - 90%)
Jig setup with no circuit under test.
$V_{CC} = V_{CC(AUX)}$ = +2.0 V
V_{EE} = -3.2 V

Logic levels are nominal values at 50 Ω fan-out determined by indicated power supplies. These values chosen to permit use of scope 50 Ω termination to ground.

Decoupling 0.1 μF from ground to V_{EE}.

OPERATING NOTES

Interconnection recommendations

All high speed CML circuits demand that special precautions be taken for optimum system performance. A ground plane must be provided for a good, low impedance, ground current return path and to transform interconnections into microstrip transmission lines. The voltage supply lines should be well decoupled with small capacitors throughout each card between V_{EE} and the ground plane and by including at least one larger tantalum capacitor per card.

Typical microstrip lines have a characteristic impedance between 50 and 150 ohms with the lower being more desirable in CML systems. For local interconnects the internal 2 kΩ resistors provide adequate termination but for optimum performance lines longer than 15 cm in length should be terminated in their characteristic impedance.

Lines up to 30 cm may be left unterminated if a degraded waveform can be tolerated with the resultant decrease in speed and increase in ringing.

Microstrip interconnections may be terminated by a resistor: $R = \frac{Z_o}{1 - NZ_o/2000}$ to a −2 V supply where Z_o is the characteristic impedance of the line and N is the number of loads. Alternately, a 2 resistor divider network may be used with $R_1 = 1.6\ R$ connected to ground and $R_2 = 2.6\ R$ connected to V_{EE}.

Series terminating resistors decrease noise immunity and slow rise and fall times, but can still be used if these effects are tolerable.

Coaxial cables or terminated twisted pairs of wire are required for backpanel interconnections longer than 10 cm.

Line driving capability

50 Ω coaxial cables properly terminated may be driven with almost no degradation in the waveform. The normal delay due to the finite speed of the signal traveling down the cable will be encountered in addition to a slight decrease in signal swing. The decrease caused by the attenuation of the cable will lower the noise immunity of the receiving circuit by the same amount.
Care must be exercised to ensure the ground potentials at the driving and receiving ends of a line are equal and no differential noise is present.

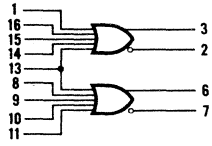
The GH family of CML silicon monolithic integrated circuits is designed for high speed instrumentation, digital communication systems, central processors and computer terminals. All GH family elements incorporate a unique temperature compensation network which insures that significant parameters such as logic levels, noise margin and speed remain relatively constant over a wide temperature range.

The GHH211/95L22, GHH221/95L23 and GHH231/95L24 are OR/NOR low power gates employing a non-saturating current switch emitter follower configuration to achieve high speed.

High input impedance and open outputs allow effective usage of terminated line technology and large wired-OR lines. Package pin locations are chosen to reduce internal noise generation and crosstalk. The GH family corresponds to the ECL9500 series.

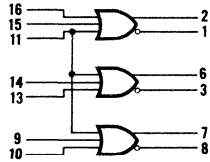
LOW POWER OR/NOR GATES

GHH211/95L22



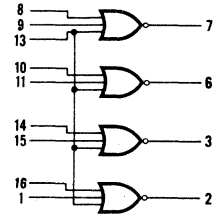
Dual 4-input OR/NOR with enable input

GHH221/95L23



Triple 2-input OR/NOR with enable input

GHH231/95L24



Quadruple 2-input NOR with enable input

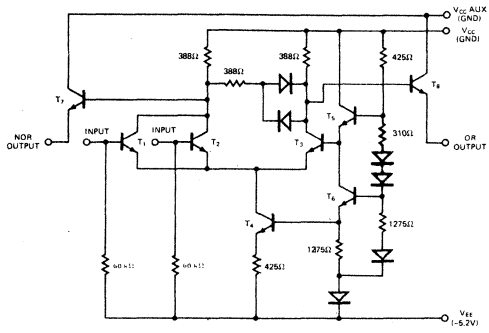
QUICK REFERENCE DATA				
Supply voltage	$-V_{EE}$		5.2	V
Operating ambient temperature range	T_{amb}	0 to +75		°C
Average propagation delay time	t_{pd}		2.0	ns
Output voltage HIGH state	$-V_{OH}$	max.	960	mV
LOW state	$-V_{OL}$	max.	1720	mV
Power consumption per gate				
GHH211/95L22	P_{av}	typ.	27	mW
GHH221/95L23	P_{av}	typ.	23	mW
GHH231/95L24	P_{av}	typ.	21	mW

PACKAGE OUTLINE 16 lead ceramic dual in-line (See General Section).

Note

V_{CC} = ground (pins 4 and 5)
$-V_{EE}$ = 5.2 V (pin 12)

CIRCUIT DIAGRAM



FUNCTIONAL DESCRIPTION

The GH gates are based on the conventional emitter coupled configuration. Additional circuit complexity is incorporated to improve system operating characteristics. This includes temperature compensation networks to insure that logic levels and thresholds, set by the on chip bias driver, are essentially independent of temperature. A current source in the tail of the differential amplifier equalizes ONE (HIGH) and ZERO (LOW) level noise margins by removing the NOR side saturation knee, and also improves saturation temperature dependency.
Defining logic "ONE" as $-V_{OH}$ = 960 mV (typ.) and logic "ZERO" as $-V_{OL}$ = 1720 mV (typ.) the elements perform the logical NOR and OR functions (positive logic). An input enable line common to all gates in each package is provided for additional logic flexibility.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134).

Supply voltage (d.c.)	$-V_{EE}$	max.	6.0	V
(peak voltage)	$-V_{EEM}$	max.	8.0	V
Input voltage			0 to −6.0	V
Output current		max.	40	mA
Storage temperature	T_{stg}		−65 to +150	°C
Operating ambient temperature	T_{amb}		0 to +75	°C

CHARACTERISTICS (d.c.) at V_{CC} = ground; $-V_{EE}$ = 5.2 V; T_{amb} = 0 to +75 °C

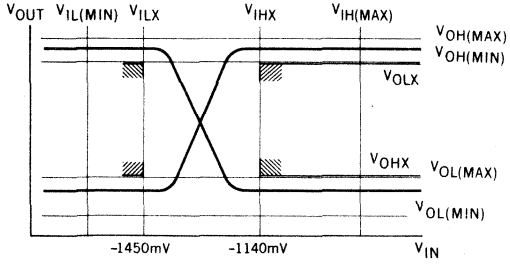
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS	
		MIN.	TYP.	MAX.			
V_{OH}	Output Voltage High		−960		mV	50 Ω to −2.0 V	$V_{IN} = V_{IL}$ = −1700 mV for NOR Gate $V_{IN} = V_{IH}$ = −900 mV for OR Gate
V_{OL}	Output Voltage Low		−1720		mV	50 Ω to −2.0 V	$V_{IN} = V_{IL}$ = −1700 mV for OR Gate $V_{IN} = V_{IH}$ = −900 mV for NOR Gate
V_{OHX}	Output Voltage High at $V_{IN} = V_{IX}$ (Threshold)	−1040			mV	50 Ω to −2.0 V	$V_{IN} = V_{ILX}$ = −1450 mV for NOR Gate $V_{IN} = V_{IHX}$ = −1140 mV for OR Gate
V_{OLX}	Output Voltage Low at $V_{IN} = V_{IX}$ (Threshold)			−1615	mV	50 Ω to −2.0 V	$V_{IN} = V_{ILX}$ = −1450 mV for OR Gate $V_{IN} = V_{IHX}$ = −1140 mV for NOR Gate
V_{IHX}	Guaranteed Input High Threshold Voltage	−1140			mV		Guaranteed Input High Threshold Voltage
V_{ILX}	Guaranteed Input Low Threshold Voltage			−1450	mV		Guaranteed Input Low Threshold Voltage
$V_{IN(H)}$	Input Current High		0.14	0.30	mA		V_{IN} = −900 mV to Common Enable Input
$V_{IN(H)}$	Input Current High		0.06	0.20	mA		V_{IN} = −900 mV to Other Inputs Sequentially
$V_{IN(L)}$	Input Current Low		.035	.125	mA		V_{IN} = −1700 mV to Each Input Sequentially
I_{PS}	Power Supply Current				mA		V_{EE} = −5.2 V, V_{CC} = GND All Inputs and Outputs Open
	GHH211/95L22	7.0	10.5	15			
	GHH221/95L23	9.0	13	18			
	GHH231/95L24	11	16	22			

CHARACTERISTICS (a.c.) at V_{CC} = ground; $-V_{EE}$ = 5.2 V

SYMBOL	CHARACTERISTICS	LIMITS				UNITS	CONDITIONS
		0°C	25°C		75°C		
		TYP.	MIN.	TYP.	MAX.	TYP.	
t_{pd}	Propagation Delay 10% – 50%						ns
	t_{pd} − −	2.0		2.0	3.0	2.2	P_L = 50 Ω to −2 V
	t_{pd} + +	2.0		2.0	3.0	2.2	C_L <5 pF
	t_{pd} − +	2.0		2.0	3.0	2.2	$t_r = t_f$ = 2.2 ns (10 – 90%)
	t_{pd} + −	2.0		2.0	3.0	2.2	
t_f	Fall Time 10% – 90%	3.0		3.0	4.5	3.0	ns
t_r	Rise Time 10% – 90%	3.0		3.0	4.5	3.0	

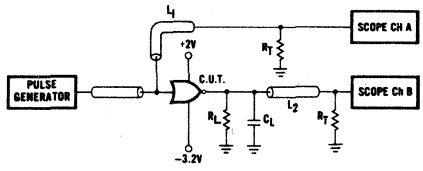
CHARACTERISTICS (continued)

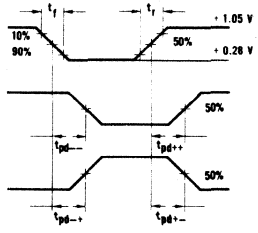
Noise margin specification points



Corner points indicated on the transfer characteristics represent the worst case points (thresholds) at which the device will start to switch. The values V_{ILX} and V_{IHX} define the maximum width of the transition region.

Switching times test circuit and waveforms





L_1 and L_2 = equal length 50 Ω impedance lines
$R_L = R_T$ = 50 Ω Termination of Scope C
C_L = Jig and Stray Capacitance < 5.0 pF

$t_r = t_f$ = 2.2 ns (10% - 90%)
Jig setup with no circuit under test.
$V_{CC} = V_{CC(AUX)}$ = +2.0 V
V_{EE} = -3.2 V

Logic levels are nominal values at 50 Ω fan-out determined by indicated power supplies. These values chosen to permit use of scope 50 Ω termination to ground. Decoupling 0.1 μF from ground to V_{EE}.

OPERATING NOTES

Interconnection recommendations

All high speed CML circuits demand that special precautions be taken for optimum system performance. A ground plane must be provided for a good, low impedance, ground current return path and to transform interconnections into microstrip transmission lines. The voltage supply line should be well decoupled with small ceramic capacitors throughout each card between V_{EE} and the ground plane and by including at least one larger tantalum capacitor per card.

Typical microstrip lines have a characteristic impedance between 50 and 150 ohms with the lower being more desirable in CML systems.

Microstrip interconnections may be terminated by a resistor to a −2.0 V supply. Devices may be wired using series type termination, but must have additional 510 Ω resistors from each output to V_{EE} or terminate through the appropriate value resistor to −2.0 V. The high impedance inputs allow high fan-outs and open outputs allow wired-OR.

Care must be taken to avoid glitches in the threshold region of the waveform occuring at certain combinations of line length and series resistor value.

Coaxial cables or terminated twisted pairs of wire are required for backpanel interconnections longer than 10 cm.

Line driving capability

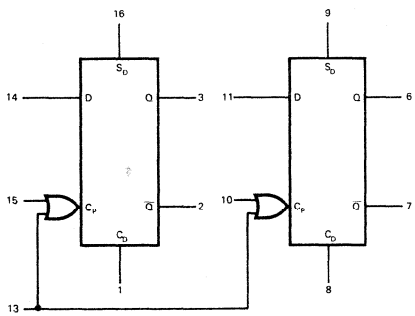
50 Ω coaxial cables properly terminated may be driven with almost no degradation in the waveform. The normal delay due to the finite speed of the signal traveling down the cable will be encountered in addition to a slight decrease in signal swing. The decrease caused by the attenuation of the cable will lower the noise immunity of the receiving circuit by the same amount. Care must be exercised to ensure the ground potentials at the driving and receiving ends of a line are equal and no differential noise is present.

The GH family of CML silicon monolithic integrated circuits is designed for high speed instrumentation, digital communication systems, central processors and computer terminals. All GH family elements incorporate a unique temperature compensation network which insures that significant parameters such as logic levels, noise margin and speed remain relatively constant over a wide temperature range.

The GHJ101/9528 is a high speed dual D-type flip-flop allowing easy implementation of high speed counters, registers and control circuits.

Input and output pull-down resistors (2 kΩ) eliminate the necessity for external termination of lines up to 15 cm and unused logic inputs. Package pin locations are chosen to reduce internal noise generation and crosstalk. The GH family corresponds to the ECL9500 series.

HIGH SPEED DUAL D-TYPE FLIP-FLOP



QUICK REFERENCE DATA				
Supply voltage	$-V_{EE}$		5.2	V
Operating ambient temperature	T_{amb}		0 to +75	°C
Toggle rate	f	typ.	160	MHz
Output voltage HIGH state	$-V_{OH}$	nom.	890	mV
LOW state	$-V_{OL}$	nom.	1710	mV
Power consumption per package	P_{av}	typ.	330	mW

PACKAGE OUTLINE 16 lead ceramic dual in-line (See General Section).

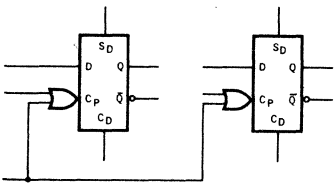
Note

V_{CC} = ground (pins 4 and 5)
$-V_{EE}$ = 5.2 V (pin 12)

FUNCTIONAL DESCRIPTION

Each D flip-flop consists of both a master and a slave. While the clock is LOW, the slave is held steady, but the information on the D input is permitted to enter the master. The next clock transition from LOW to HIGH locks the master in its present state making it insensitive to the D input and connects the slave to the master causing the new information to be reflected on the outputs. The following clock transition from HIGH to LOW again locks the slave and permits information to flow into the master. Logic races are avoided by offsetting the master and slave thresholds to avoid simultaneous switching when LOW speed edges are encountered in the system. The internal clock is the OR of two clock inputs, one common to both flips-flops. The outputs will only switch following a LOW to HIGH transition of the ORed clock (unless the direct set or clear inputs are activated). The ORed clock permits the use of one input as a clock pulse input and the other as an active LOW enable. If one clock input is held HIGH, clock pulses on the other input will not be seen by the flip-flop. To maintain synchronous operating, however, the clock input used as an enable should only be changed while the clock is HIGH.

LOGIC DIAGRAM



FUNCTION TABLES

SYNCHRONOUS OPERATION

D TABLE	
D_n	$Q_n + 1^*$
L	L
H	H
$^*S_D \cdot C_D$ = Low	

ASYNCHRONOUS OPERATION

$S_D \cdot C_D$ TABLE			
C_D	S_D	Q	$\overline{Q}$
L	L	See D Table	See D Table
L	H	H	L
H	L	L	H
H	H	Not Allowed	

RATINGS Limiting values in accordance with the Absolute Maximum System(IEC134).

Supply voltage (d.c.)	$-V_{EE}$	max.	6.0	V
(peak value)	$-V_{EEM}$	max.	8.0	V
Input voltage			0 to −6.0	V
Output current		max.	40	mA
Storage temperature	T_{stg}		−65 to +150	°C
Operating ambient temperature	T_{amb}		0 to +75	°C

CHARACTERISTICS (d.c.) at V_{CC} = ground; $-V_{EE}$ = 5.2 V

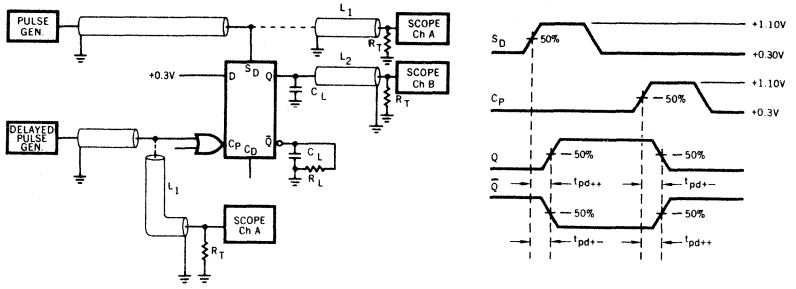
SYMBOL	CHARACTERISTIC	LIMITS									UNITS	CONDITIONS
		0°C			+25°C			+75°C				
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP	MAX.		
V_{OH}	Output High Voltage	−905	−850	−795	−905	−850	−795	−895	−840	−785	mV	FO = 1 Gate
		−945	−890	−835	−945	−890	−835	−945	−890	−835	mV	FO = 5 Gates
		−980	−925	−870	−980	−925	−870	−980	−925	−870	mV	R_L = 50 Ω to −2.0 V
V_{OL}	Output Low Voltage	−1755	−1670	−1585	−1755	−1670	−1585	−1755	−1670	−1585	mV	FO = 1 Gate
		−1795	−1710	−1625	−1795	−1710	−1625	−1795	−1710	−1625	mV	FO = 5 Gates
		−1785	*−1700*	*−1615*	*−1785*	*−1700*	*−1615*	*−1785*	*−1700*	*−1615*	mV	*R_L = 50 Ω to −2.0 V*
V_{IHX}	Input High Threshold Voltage	−1140			−1140			−1140			mV	Guaranteed Input High
V_{ILX}	Input Low Threshold Voltage			−1450			−1450			−1450	mV	Guaranteed Input Low
$I_{IN(1)}$	Input Current at V_{IH}		2.30	3.15		2.25	3.10		2.15	3.00	mA	V_{IH} = 900 mV to each
	Common Clock Input		4.60	6.30		4.50	6.20		4.30	6.00		input sequentially
$I_{IN(0)}$	Input Current at V_{IL}		1.80	2.40		1.75	2.35		1.65	2.25	mA	V_{IL} = 1700 mV to each
	Common Clock Input		3.60	4.80		3.50	4.70		3.30	4.50		input sequentially
I_{PS}	Power Supply Current	46	62	84	51	64	85	52	66	90	mA	All inputs open

CHARACTERISTICS (a.c.) at V_{CC} = ground; $-V_{EE}$ = 5.2 V

SYMBOL	CHARACTERISTIC	LIMITS									UNITS	CONDITIONS
		0°C			+25°C			+75°C				
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
I_T	Transient Input Current					2.5	3.5				mA	
	Common Clock					3.5	4.5				mA	
t_{pd}	Clock Input											V_{CC} = 2.0 V
	t_{pd++}		3.6			3.6	4.8		3.6		ns	V_{EE} = −3.2 V
	t_{pd+-}		3.6			3.6	4.8		3.6		ns	
	S_D & C_D Input											R_L = 50 Ω to Gnd
	t_{pd++}		3.6			3.6	4.8		3.6		ns	C_L < 5 pF
	t_{pd+-}		3.6			3.6	4.8		3.6		ns	$t_r = t_f$ = 2.5 ns
	Toggle Rate				110	160					MHz	

CHARACTERISTICS (continued)

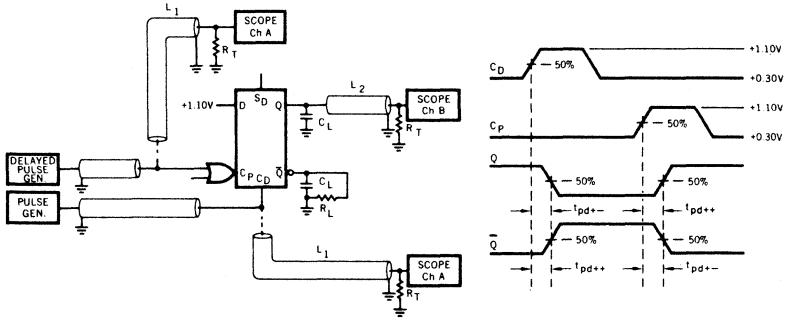
S_D asynchronous input switching times test circuit and waveforms



CONDITIONS

$V_{CC} = +2.0$ V
$V_{EE} = -3.2$ V
$R_L = 50\ \Omega = R_T$ (Scope input impedance)
C_L = Jig and stray capacitance < 5 pF
$L_1 = L_2$ equal 50 Ω impedance lines
Input signal $t_r = t_f = 2.5$ ns (10% - 90%)
with no circuit under test

C_D asynchronous input switching time test circuit and waveforms

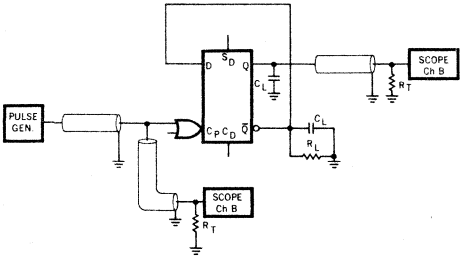


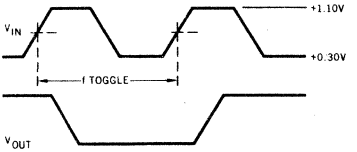
CONDITIONS

$V_{CC} = +2.0$ V
$V_{EE} = -3.2$ V
$R_L = 50\ \Omega = R_T$ (Scope input impedance)
C_L = Jig and stray capacitance < 5 pF
$L_1 = L_2$ equal 50 Ω impedance lines
Input signal $t_r = t_f = 2.5$ ns (10% - 90%)
with no circuit under test

CHARACTERISTICS (continued)

Toggle rate test circuit and waveforms

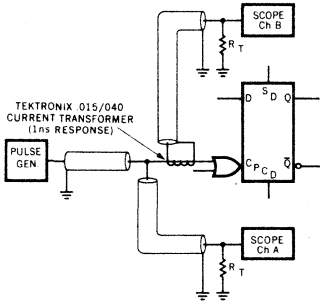


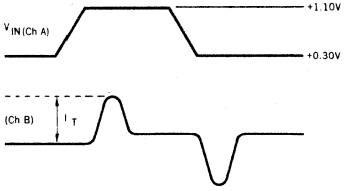


CONDITIONS

V_{CC} = +2.0 V
V_{EE} = −3.2 V
R_L = 50 Ω = R_T (Scope input impedance)
C_L = Jig and stray capacitance < 5 pF
Pulse Gen. — EH 122 or equivalent

Transient input current test circuit and waveforms





This test provides a measure of the average value of C_{IN}.

CONDITIONS

V_{CC} = +2.0 V
V_{EE} = −3.2 V
R_T = 50 Ω (Scope input impedance)
Input signal $t_r = t_f$ = 2.5 ns (10% - 90%) with no circuit under test

OPERATING NOTES

Interconnection recommendations

All high speed CML circuits demand that special precautions be taken for optimum system performance. A groundplane must be provided for a good, low impedance, ground current return path and to transform interconnections into microstrip transmission lines. The voltage supply lines should be well decoupled with small capacitors throughout each card between V_{EE} and the ground plane and by including at least one larger tantalum capacitor per card.

Typical microstrip lines have a characteristic impedance between 50 and 150 ohms with the lower being more desirable in CML systems. For local interconnects the internal 2 kΩ resistors provide adequate termination but for optimum performance lines longer than 15 cm in length should be terminated in their characteristic impedance.

Microstrip interconnections may be terminated by a resistor: $R = \frac{Z_o}{1 - NZ_o/2000}$ to a −2 V supply where Z_o is the characteristic impedance of the line and N is the number of loads. Alternately, a 2 resistor divider network may be used with $R_1 = 1.6$ R connected to ground and $R_2 = 2.6$ R connected to V_{EE}.

Coaxial cables or terminated twisted pairs of wire are required for backpanel interconnections longer than 10 cm.

Line driving capability

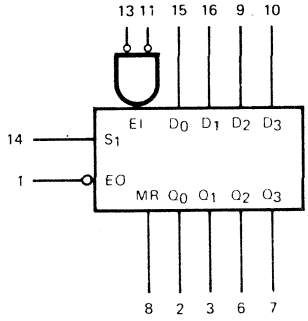
50 Ω coaxial cables properly terminated may be driven with almost no degradation in the waveform. The normal delay due to the finite speed of the signal traveling down the cable will be encountered in addition to a slight decrease in signal swing. The decrease caused by the attenuation of the cable will lower the noise immunity of the receiving circuit by the same amount.
Care must be exercised to ensure the ground potentials at the driving and receiving ends of a line are equal and no differential noise is present.

The GH family of CML silicon monolithic integrated circuits is designed for high speed instrumentation, digital communication systems, central processors and computer terminals. All GH family elements incorporate a unique temperature compensation network which insures that significant parameters such as logic levels, noise margin and speed remain relatively constant over a wide temperature range.

The GHJ111/9534 is a quadruple D-latch capable of storing four bits of information simultaneously. This element is designed as a storage buffer for high speed register in arithmetic logic units and a data buffer in communication system. The common enable inputs and a common output enable allow maximum logic flexibility. A common select input selects "D" type or "Set" type of operation. A common reset clears the device so that the 1's catching feature may be used when desired.

Input and output pull-down resistors (2 kΩ) eliminate the necessity for external termination of lines up to 15 cm and unused logic inputs. Package pin locations are chosen to reduce internal noise generation and crosstalk. The GH family corresponds to the ECL9500 series.

RESETTABLE QUADRUPLE 'D' LATCH WITH I/O ENABLE



QUICK REFERENCE DATA				
Supply voltage	$-V_{EE}$		5.2	V
Operating ambient temperature range	T_{amb}		0 to +75	°C
Average propagation delay time from data input to output	t_{pd}	typ.	4.3	ns
Output voltage HIGH state	$-V_{OH}$	nom.	890	mV
LOW state	$-V_{OL}$	nom.	1710	mV
Power consumption	P_{av}	typ.	415	mW

PACKAGE OUTLINE 16 lead ceramic dual in-line (See General Section).

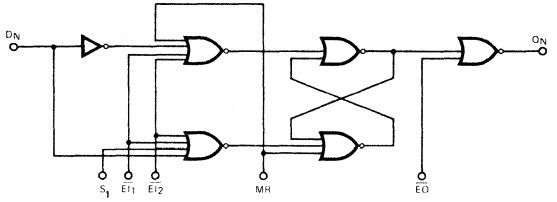
Note

V_{CC} = ground (pins 4 and 5)
$-V_{EE}$ = 5.2 V (pin 12)

FUNCTIONAL DESCRIPTION

Data can be entered into the latch whenever both input enable inputs ($\overline{EI}$) are LOW. If either of the input enables goes HIGH, the data present in the latch at that time is held and is no longer affected by the data input. Data may be read-out of the latches whenever the output enable ($\overline{EO}$) is LOW. If the output enable goes HIGH, then the outputs are forced LOW, but the data is undisturbed. This function allows many GHH111/9534 types to be wired-OR together and read-out when selected. Information may be fed into the latch and stored while the outputs are held LOW. If the S_1 input is held HIGH, the GHJ111/9534 becomes a quadruple set-reset latch with separate sets (D_N) and a common reset (MR). In this mode, if both input enables are LOW, the latches are ones catching. Again if either input enable goes HIGH, the data present in the latch is held and is no longer affected by the data input. If at any time the master reset goes HIGH, all latches are forced to "0". If the output enable goes HIGH, only the outputs will be forced to "0". The data remains undisturbed.

LOGIC DIAGRAM (for one latch)



D_N = Data inputs
Q_N = Data outputs
S_1 = Select
MR = Master Reset
$\overline{EO}$ = Output Enable
$\overline{EI}$ = Input Enable

RATINGS Limting values in accordance with the Absolute Maximum System (IEC134).

Supply voltage (d.c.)	$-V_{EE}$	max.	6.0	V
(peak value)	$-V_{EEM}$	max.	8.0	V
Input voltage			0 to −6.0	V
Output current		max.	40	mA
Storage temperature	T_{stg}		−65 to +150	°C
Operating ambient temperature	T_{amb}		0 to +75	°C

CHARACTERISTICS (d.c.) at V_{CC} = ground; $-V_{EE}$ = 5.2 V ; T_{amb} = 0 to +75 °C

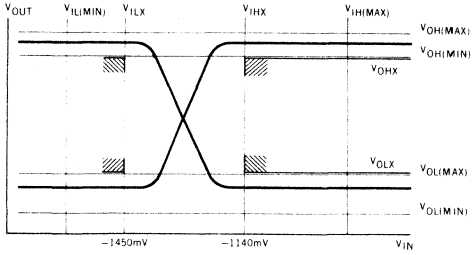
SYMBOL	CHARACTERISTIC	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	CONDITIONS	
V_{OH}	Output High Voltage	−905 −945 −980	−850 −890 −925	−785 −835 −870	mV	FO = 1 Gate FO = 5 Gates 50 Ω to −2.0 V	V_{IN} = −0.900 V (D operation)
V_{OL}	Output Low Voltage	−1755 −1795 −1785	−1670 −1710 −1700	−1585 −1625 −1615	mV	FO = 1 Gate FO = 5 Gates 50Ω to −2.0 V	V_{IN} = −1.700 V (D operation)
V_{OHC}	Output High Corner Point	−915 −955 −990			mV	FO = 1 Gate FO = 5 Gates 50 Ω to −2.0 V	$V_{IN} = V_{IHX}$ (D Input) $V_{IN} = V_{ILX}$ (EO Input)
V_{OLC}	Output Low Corner Point			−1575 −1615 −1605	mV	FO = 1 Gate FO = 5 Gates 50 Ω to −2.0 V	$V_{IN} = V_{ILX}$ (D Input) $V_{IN} = V_{IHX}$ (EO Input)
V_{IHX}	Input High Level	−1140			mV	Guaranteed Input High Threshold Voltage	
V_{ILX}	Input Low Level			−1450	mV	Guaranteed Input Low Threshold Voltage	
$I_{IN(H)}$	Input Current at V_{IH}		2.25	3.15	mA	V_{IN} = −900 mV to Each Input Sequentially	
$I_{IN(L)}$	Input Current at V_{IL}		1.75	2.40	mA	V_{IN} = −1700 mV to Each Input Sequentially	
I_{PS}	Power Supply Current		80		mA	V_{EE} = −5.2 V, All Inputs Open	

CHARACTERISTICS (a.c.) at V_{CC} = ground; $-V_{EE}$ = 5.2 V

SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN	0°C TYP	0°C MAX	25°C MIN	25°C TYP	25°C MAX	75°C MIN	75°C TYP	75°C MAX	UNITS
t_{pd}	Propagation Delay										
	DATA INPUT										
	t_{pd--}		4.3			4.3			4.6		ns
	t_{pd++}		4.3			4.3			4.6		ns
	OUTPUT ENABLE										
	t_{pd-+}		3.4			3.4			3.6		ns
	t_{pd++}		3.4			3.4			3.6		ns
	MR INPUT										
	t_{pd-+}		5.6			5.6			6.0		ns
	t_{pd+-}		5.6			5.6			6.0		ns
	EI INPUT										
	t_{pd-+}		5.6			5.6			6.0		ns
	SELECT INPUT										
	t_{pd-+}		5.6			5.6			6.0		ns
	Transient Input Current					2.5	3.5				mA
I_T	Master Reset					5.0	6.0				mA
	Output Enable					3.5	4.5				mA

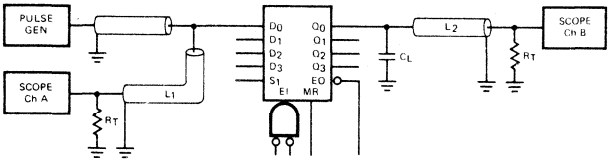
CHARACTERISTICS (continued)

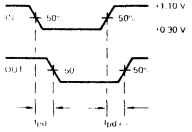
Noise margin specification points



Corner points indicated on the transfer characteristics represent the worst case points (thresholds) at which the device will start to switch. The values V_{ILX} and V_{IHX} define the maximum width of the transition region.

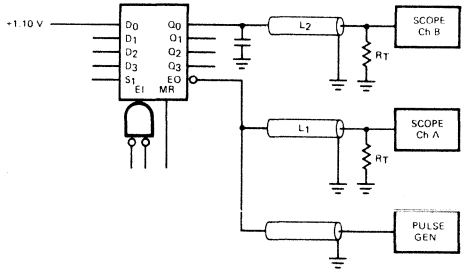
Switching times test circuits and waveforms

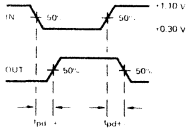




CONDITIONS
V_{CC} = +2.0 V
V_{EE} = −3.2 V
R_L = 50 Ω = R_T (Scope input impedance)
C_L = jig and stray capacitance < 5 pF
L_1 = L_2 equal 50 Ω impedance lines
Input signal t_r = t_f = 2.5 ns (10% − 90%)
With no circuit under test

From data to output

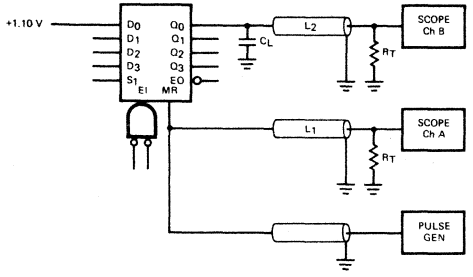


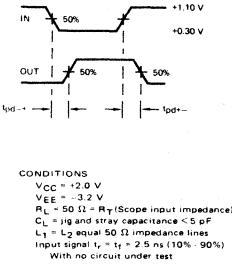


CONDITIONS
V_{CC} = +2.0 V
V_{EE} = −3.2 V
R_L = 50 Ω = R_T (Scope input impedance)
C_L = jig and stray capacitance < 5 pF
L_1 = L_2 equal 50 Ω impedance lines
Input signal t_r = t_f = 2.5 ns (10% − 90%)
With no circuit under test

From output enable to output

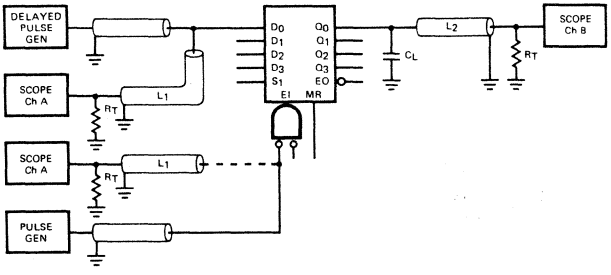
CHARACTERISTICS (continued)

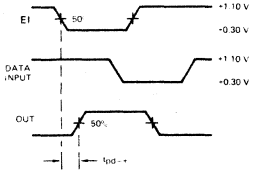




CONDITIONS
V_{CC} = +2.0 V
V_{EE} = −3.2 V
R_L = 50 Ω = R_T (Scope input impedance)
C_L = jig and stray capacitance < 5 pF
L_1 = L_2 equal 50 Ω impedance lines
Input signal t_r = t_f = 2.5 ns (10% - 90%)
With no circuit under test

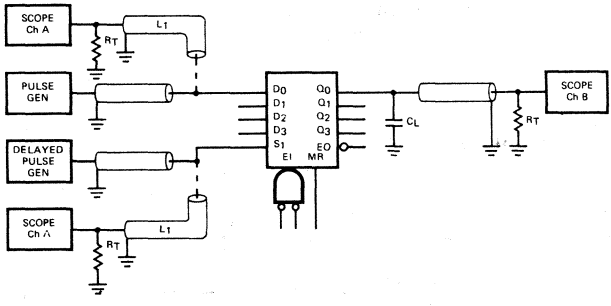
From master reset to output

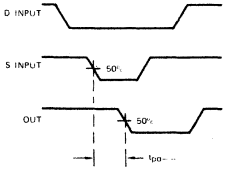




CONDITIONS
V_{CC} = +2.0 V
V_{EE} = −3.2 V
R_L = 50 Ω = R_T (Scope input impedance)
C_L = jig and stray capacitance < 5 pF
L_1 = L_2 equal 50 Ω impedance lines
Input signal t_r = t_f = 2.5 ns (10% - 90%)
With no circuit under test

From input enable to output



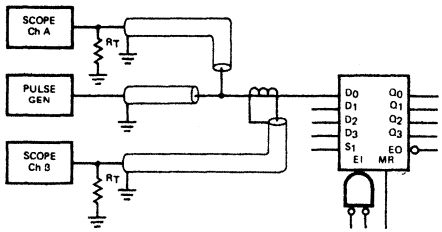


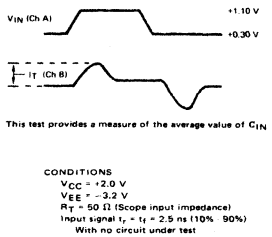
CONDITIONS
V_{CC} = +2.0 V
V_{EE} = −3.2 V
R_L = 50 Ω = R_T (Scope input impedance)
C_L = jig and stray capacitance < 5 pF
L_1 = L_2 equal 50 Ω impedance lines
Input signal t_r = t_f = 2.5 ns (10% - 90%)
With no circuit under test

From select to output

CHARACTERISTICS (continued)

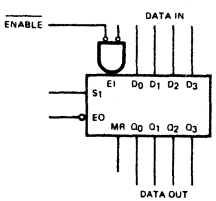
Transient input current test circuit and waveforms





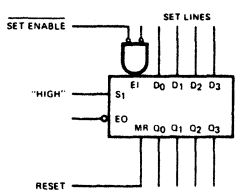
APPLICATION INFORMATION

4 BIT STORAGE LATCH



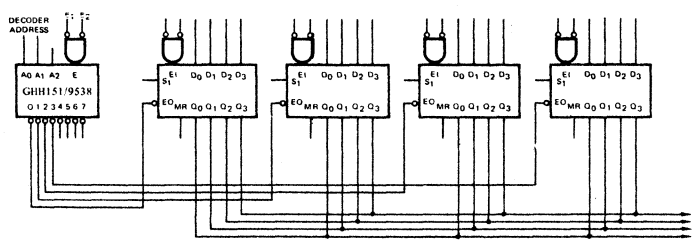
The figure illustrates the use of the GHJ111/9534 as a D-type storage latch.
Data is stored in the latch when the enable line is HIGH.

QUAD SET-RESET LATCH



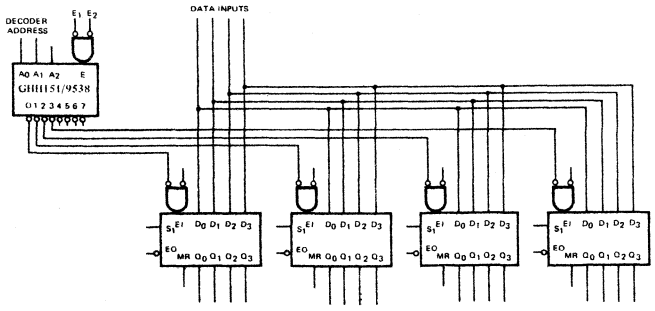
This figure illustrates the use of the GHJ111/9534 as a quadruple set-reset latch. If while the enable is LOW, a "HIGH" appears at an input ($\overline{D_N}$) the latch sets and stays set even if the input returns to a "LOW". A "HIGH" on the master reset removes all "HIGH's" from the latch.

REGISTER MULTIPLEXING



APPLICATION INFORMATION (continued)

REGISTER DEMULTIPLEXING



OPERATING NOTES

Interconnection recommendations

All high speed CML circuits demand that special precautions be taken for optimum system performance. A ground plane must be provided for a good, low impedance, ground current return path and to transform interconnections into microstrip transmission lines. The voltage supply lines should be well decoupled with small capacitors throughout each card between V_{EE} and the ground plane and by including at least one larger tantalum capacitor per card.

Typical microstrip lines have a characteristic impedance between 50 and 150 ohms with the lower being more desirable in CML systems. For local interconnects the internal 2 kΩ resistors provide adequate termination but for optimum performance lines longer than 15 cm in length should be terminated in their characteristic impedance.

Microstrip interconnections may be terminated by a resistor: $R = \frac{Z_o}{1 - NZ_o/2000}$ to a −2 V supply where Z_o is the characteristic impedance of the line and N is the number of loads. Alternately, a 2 resistor divider network may be used with $R_1 = 1.6$ R connected to ground and $R_2 = 2.6$ R connected to V_{EE}.

Coaxial cables or terminated twisted pairs of wire are required for backpanel interconnections longer than 10 cm.

Line driving capability

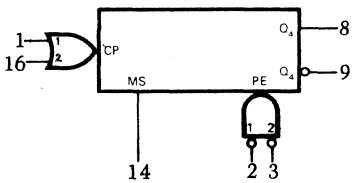
50 Ω coaxial cables properly terminated may be driven with almost no degradation in the waveform. The normal delay due to the finite speed of the signal traveling down the cable will be encountered in addition to a slight decrease in signal swing. The decrease caused by the attenuation of the cable will lower the noise immunity of the receiving circuit by the same amount.
Care must be exercised to ensure the ground potentials at the driving and receiving ends of a line are equal and no differential noise is present.

The GH family of CML silicon monolithic integrated circuits is designed for high speed instrumentation, digital communication systems, central processors and computer terminals. All GH family elements incorporate a unique temperature compensation network which insures that significant parameters such as logic levels, noise margin and speed remain relatively constant over a wide temperature range.

The GHJ121/95H90 is a high speed prescaler designed specifically for communication and instrumentation applications. In its simplest use this device will divide by 10 any clock frequency up to 320 MHz.

By using the GHJ121/95H90 with other control logic, a divide by "N" counter can be constructed.

DIVIDE BY 10/11 PRESCALER



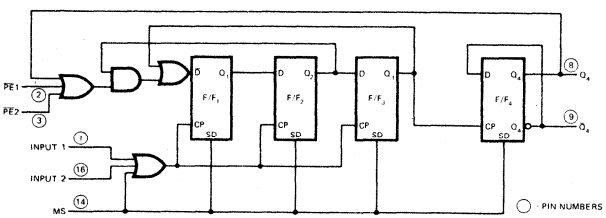
QUICK REFERENCE DATA			
Supply voltage	$-V_{EE}$	5.2	V
Operating ambient temperature range	T_{amb}	0 to +75	°C
Output voltage HIGH state	$-V_{OH}$	nom. 910	mV
LOW state	$-V_{OL}$	nom. 1740	mV
Maximum clock frequency	f_{max}	typ. 320	MHz
Power consumption	P_{av}	typ. 470	mW

PACKAGE OUTLINE 16 lead ceramic dual in-line (See General Section).

Note

V_{CC} = ground (pins 4 and 5)
$-V_{EE}$ = 5.2 V (pin 12)

LOGIC DIAGRAM



COUNT SEQUENCE

Q_1	Q_2	Q_3	Q_4
H	H	H	H
L	H	H	H
L	L	H	H
L	L	L	H
H	L	L	H
H	H	L	H
L	H	H	L
L	L	H	L
L	L	L	L
H	L	L	L
H	H	L	L

NOTE: "HHHH" is set state and additional state for ÷11 mode.

Pin names

$\overline{CP}_1$, $\overline{CP}_2$: Dual "OR" clock inputs (active HIGH)
$\overline{PE}_1$, $\overline{PE}_2$: Prescale by 11 (eleven) "AND" enable inputs (active LOW)
MS : Asynchronous master set (active HIGH)
Q_4 : Assertion output
$\overline{Q}_4$: Negative output

FUNCTIONAL DESCRIPTION

The GHJ121/95H90 acts as a controllable (divide by 10/divide by 11) prescaler accepting clock pulses of up to 320 MHz. Output Q_4 is LOW for 5 incoming clock pulses and HIGH for the subsequent 5 or 6 incoming clock pulses, the decision between the two modes being made by the state of the two active LOW PE inputs. If both $\overline{PE}_1$ and $\overline{PE}_2$ are LOW 5.4 ns before the rising edge of Q_4, then Q_4 will stay HIGH for 6 incoming clock pulses (divide by 11). If either $\overline{PE}_1$, or $\overline{PE}_2$ is HIGH before the rising edge of Q_4, the output will stay HIGH for 5 clock pulses (divide by 10). The two input "OR" clock inputs can be used to combine two independent clock sources or one input can act as a clock enable (active LOW). A master set is provided to initialize the prescaler. This input, when activated, overrides the clock and forces the prescaler into the HHHH state with Q_4 forced HIGH and $\overline{Q}_4$ forced LOW. The prescaler will divide by 11 the first count cycle after being master set.

MODE SELECTION TABLE

$\overline{PE}_1$	$\overline{PE}_2$	PRESCALER MODULO
		Divide By
L	L	11
L	H	10
H	L	10
H	H	10

Note
When using the GHJ121/95H90 as a modulo 10 prescaler, the $\overline{Q}$ output may be connected to a $\overline{PE}$ input.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134).

Supply voltage (d.c.)	$-V_{EE}$	max.	6.0	V
(peak value)	$-V_{EEM}$	max.	8.0	V
Input voltage			0 to −6.0	V
Output current		max.	40	mA
Storage temperature	T_{stg}		−65 to +150	°C
Operating ambient temperature	T_{amb}		0 to +75	°C

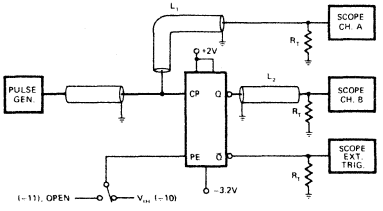
CHARACTERISTICS (d.c.) at V_{CC} = ground; $-V_{EE}$ = 5.2 V ; T_{amb} = 0 to +75 °C

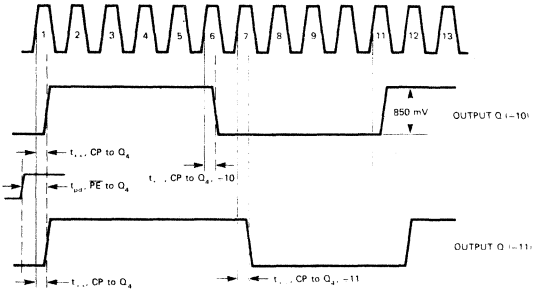
SYMBOL	CHARACTERISTIC	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	CONDITIONS	
V_{OH}	Output Voltage High		−860 −910 −950		mV	FO= 1 Gate FO= 5 Gates R_L = 50 Ω to −2.0V	$V_{IN} = V_{IL}$ (−1700mV) or V_{IH} = (−900mV) as per Count Sequence
V_{OL}	Output Voltage Low		−1690 −1740 −1720		mV	FO= 1 Gate FO= 5 Gates R_L = 50 Ω to −2.0V	$V_{IN} = V_{IL}$ (−1700mV) or V_{IH} = (−900mV) as per Count Sequence
V_{OHC}	Output Voltage High at $V_{IN} = V_{IX}$ (threshold)	−930 −970 −1010			mV	FO= 1 Gate FO= 5 Gates R_L = 50 Ω to −2.0V	$V_{IN} = V_{ILX}$ or V_{IHX} as per Count Sequence
V_{OLC}	Output Voltage Low at $V_{IN} = V_{IX}$ (threshold)			−1605 −1655 −1635	mV		$V_{IN} = V_{ILX}$ or V_{IHX} as per Count Sequence
V_{IHX}	Input High Threshold Voltage	−1140			mV		Guaranteed Input High Threshold Voltage
V_{ILX}	Input Low Threshold Voltage			−1450	mV		Guaranteed Input Low Threshold Voltage
$I_{IN(H)}$	Input Current High		2.40	3.65	mA		V_{IN} = −900mV to MS Input (Pin 14)
$I_{IN(H)}$	Input Current High		2.25	3.15	mA		V_{IN} = −900mV to other Inputs Sequentially
$I_{IN(L)}$	Input Current Low		1.75	2.40	mA		V_{IN} = −1700 mV to Each Input Sequentially
I_{PS}	Power Supply Current	66	90	119	mA		All Inputs Open

CHARACTERISTICS (a.c.) at V_{CC} = ground; $-V_{EE}$ = 5.2 V

SYMBOL	CHARACTERISTIC	LIMITS 0°C TYP.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 75°C MIN.	LIMITS 75°C TYP.	LIMITS 75°C MAX.	UNITS	CONDITIONS
t_{pd}	Propagation Delay(50%-50%)									Output
	CP to Q_4, t_{pd++}	4.9		5.1	6.8		5.5		ns	R_L = 50Ω to −2.0V
	CP to Q_4, t_{pd--}	4.9		5.1	6.8		5.5		ns	C_L = 5.0pF
	MS to Q_4, t_{pd++}	5.3		5.7	7.6		6.5		ns	Input
	$\overline{PE}$ to Q_4, t_{pd++}	5.2		5.4			5.8		ns	$t_r = t_f$ = 2.2±0.1 ns (10%-90%)
t_r	Output Rise Time (10%-90%)	2.4	1.2	2.4	3.6		2.4		ns	
t_f	Output Fall Time (10%-90%)	2.4	1.2	2.4	3.6		2.4		ns	
t_{ri}=t_{fi}	Clock Input Transition Time	30			25			25	ns	Input t_r, t_f for correct operation
f_{max}	Maximum Clock Frequency	320	220	320			270		MHz	Sine Wave of 800mVpp about −1300mV

Switching times test circuit and waveforms





CONDITIONS
V_{CC} = +2.0 V
V_{EE} = −3.2 V
R_L = 50 Ω = R_T (Scope input impedance)
C_L = Jig and stray capacitance <5 pF
L_1 = L_2 equal 50 Ω impedance lines
Input signal t_r = t_f = 2.5 ns (10% - 90%)
with no circuit under test

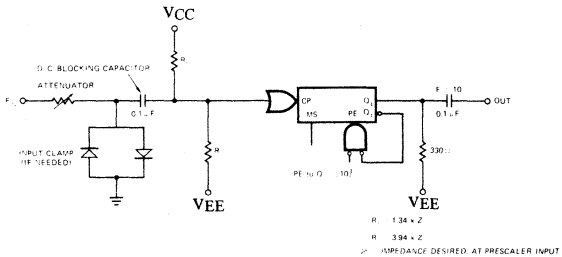
CLOCK PULSE CONDITIONS
V_{IH} = +1050 mV
V_{IL} = +280 mV
t_r = t_f = 2.2 ± 0.1 ns (10% - 90%)

APPLICATION INFORMATION

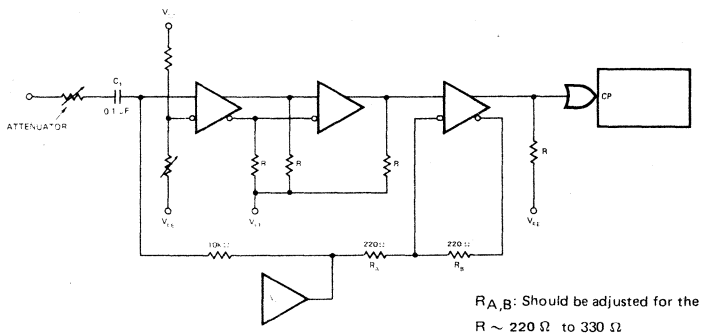
Prescaler

In its simplest application, as a divide-by-ten prescaler, the GHJ121/95H90 extends the frequency range of TTL frequency counters and phase locked systems to over 300 MHz. For this and other r.f. applications the input bias should be set close to the clock threshold. This improves a.c. sensitivity but it also increases noise sensitivity. A preamplifier is often a better way to improve sensitivity, especially in frequency counters. Care should be taken to avoid overdriving the prescaler input which would saturate the input transistor and seriously degrade the frequency resolution. Excessive input voltages might also damage the device (See also Ratings).

Divide by ten r.f. prescaler



Prescaler with r.f. preamplifier



$R_{A,B}$: Should be adjusted for the desired Hysteresis
R ~ 220 Ω to 330 Ω

GHY101/9582

APPLICATION INFORMATION (continued)

Programmable divider for frequency synthesizers

An integral part of most frequency synthesizers is a programmable divider. In a conventional design these become bulky, expensive and power consuming when implement for frequencies above the TTL range. The GH121/95H90 is especially designed for a technique called "pulse swallowing" which allows a device like the GHJ121/95H90 to be controlled by a relatively slow TTL presetable counter. This technique offers the advantage of prescaling and does not sacrifice resolution. The only drawback is that there is a clearly defined minimum divide ratio below which the system does not function.

Pulse swallowing uses three functional blocks:
- A variable modulo prescaler, controllable between modulo K and K + 1
- A swallow counter which controls the prescaler
- A programmable counter

The swallow counter determines the number of times that the prescaler divides by K + 1, effectively swallowing one additional input for each output pulse to the programmable counter.

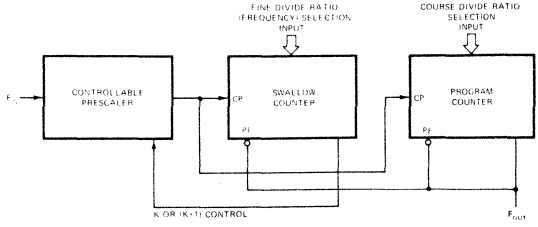
As an example, consider a divider (K = 10) that is programmed by decade switches. Inverting nine's complement decade switches are required since the switch must ground the counter input in order to insert a zero. At the beginning of a divide cycle the swallow counter and the program counter are loaded with the nine's complement of the desired ratio and the count from there to their respective terminal states. If a ratio of 83 is desired, the swallow counter is preset to 6 and the program counter to 9991. The programmable counter will produce a terminal count output after 8 pulses from the prescaler, but since the swallow counter was preset to 6, the prescaler will have divided by 11 three times, by 10 the other five times. As a result, the output pulse will occur after 83 input pulses.

The prescaler modulo (K) is chosen to bring the prescaler output frequency into the range of TTL. Higher modulo prescalers (20/21, 100/101) can be implemented by additional flip-flop and counters.

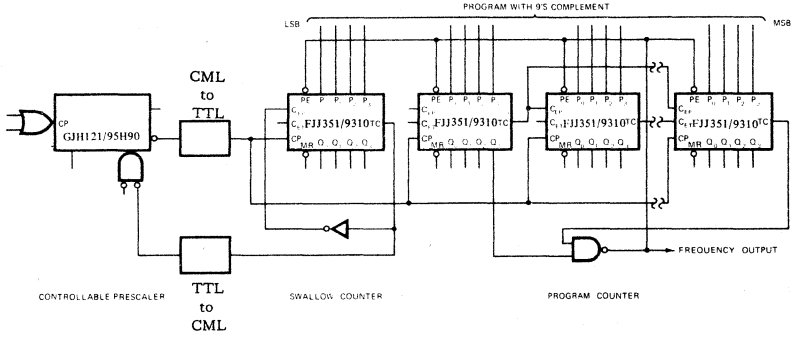
An important speed parameters to be considered is the delay in the 10/11 prescaler control path. The delay through the CML/TTL interfaces, the TTL logic and back through the TTL/CML interface must be less than $10/F_{in} - t_{pd}$ from Q_4 to P_E.

APPLICATION INFORMATION (continued)

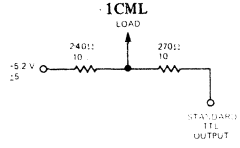
Pulse swallowing programmable divider



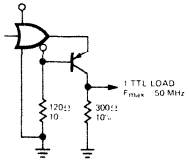
High speed programmable divider (utilizing 10/11 prescaler)



TTL to CML
Common Power Supply.



CML to TTL
Common Power Supply.



OPERATING NOTES

Interconnection recommendations

All high speed CML circuits demand that special precautions be taken for optimum system performance. A groundplane must be provided for a good, low impedance, ground current return path and to transform interconnections into microstrip transmission lines. The voltage supply lines should be well decoupled with small capacitors throughout each card between V_{EE} and the ground plane and by including at least one larger tantalum capacitor per card.

Typical microstrip lines have a characteristic impedance between 50 and 150 ohms with the lower being more desirable in CML systems. For local interconnects the internal 2 kΩ resistors provide adequate termination but for optimum performance lines longer than 15 cm in length should be terminated in their characteristic impedance.

Microstrip interconnections may be terminated by a resistor: $R = \frac{Z_o}{1 - NZ_o/2000}$ to a −2 V supply where Z_o is the characteristic impedance of the line and N is the number of loads. Alternately, a 2 resistor divider network may be used with $R_1 = 1.6\ R$ connected to ground and $R_2 = 2.6\ R$ connected to V_{EE}.

Coaxial cables or terminated twisted pairs of wire are required for backpanel interconnections longer than 10 cm.

Line driving capability

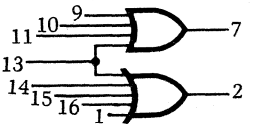
50 Ω coaxial cables properly terminated may be driven with almost no degradation in the waveform. The normal delay due to the finite speed of the signal traveling down the cable will be encountered in addition to a slight decrease in signal swing. The decrease caused by the attenuation of the cable will lower the noise immunity of the receiving circuit by the same amount.
Care must be exercised to ensure the ground potentials at the driving and receiving ends of a line are equal and no differential noise is present.

The GH family of CML silicon monolithic integrated circuits is designed for high speed instrumentation, digital communication systems, central processors and computer terminals. All GH family elements incorporate a unique temperature compensation network which insures that significant parameters such as logic levels, noise margin and speed remain relatively constant over a wide temperature range.

The GHL101/9595 is a high speed logic converter for use in systems using both the high speed of CML and the many available functions of TTL. The device requires the −5.2 V V_{EE} supply of CML and the +5.0 V V_{CC} of TTL. The TTL fan-out may be expanded by adding more pull-down current at the TTL output pin. By allowing the logic converter to function as a logic gate, the normally wasted time of logic conversion may be used in the logic implementation with the through delay generally less than that found in TTL circuits. Input pull-down resistors (2 kΩ) allow unused inputs to be left open.

The GH family corresponds to the ECL9500 series.

DUAL HIGH SPEED CML TO TTL CONVERTER



CML inputs TTL outputs

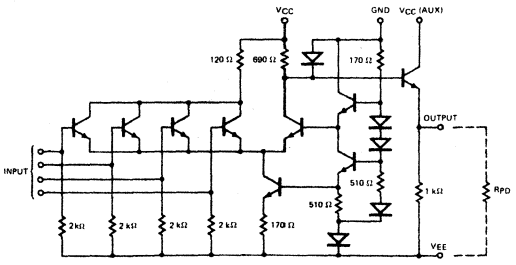
QUICK REFERENCE DATA				
Supply voltages	V_{CC}		5.0	V
	$-V_{EE}$		5.2	V
Operating ambient temperature range	T_{amb}		0 to +75	°C
Average propagation delay time	t_{pd}	typ.	6.0	ns
Output voltage HIGH state	V_{OH}	min.	2.4	V
LOW state	V_{OL}	max.	0.4	V
Power consumption per package	P_{av}	typ.	375	mW

PACKAGE OUTLINE 16 lead ceramic dual in-line (See General Section).

Note

V_{CC} = ground (pins 4 and 5)
$-V_{EE}$ = 5.2 V (pin 12)

CIRCUIT DIAGRAM (one half)



External pull-down resistors to V_{EE}: R_{PD}
(Recommended for best speed and noise immunity).

LOGIC FUNCTION

The device performs the OR function and consequently there is no inversion through each converter. An input enable line control to both converters is provided for additional logic flexibility.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134).

Supply voltages (d.c.)	V_{CC}	max.	6.0	V
(peak value)	V_{CCM}	max.	8.0	V
(d.c.)	$-V_{EE}$	max.	6.0	V
(peak value)	$-V_{EEM}$	max.	8.0	V
Input voltage		0 to	−6.0	V
Output current		max.	40	mA
Storage temperature	T_{stg}	−65 to	+150	°C
Operating ambient temperature	T_{amb}	0 to	+75	°C

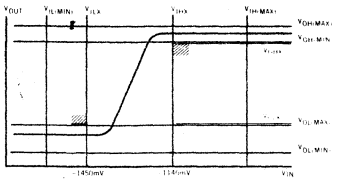
CHARACTERISTICS (d.c.) at $V_{CC} = V_{CC\ (AUX)} = 5.0\ V \pm 5\%$; $-V_{EE} = 5.2\ V \pm 5\%$; $T_{amb} = 0$ to $+75\ ^{o}C$

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN.	TYP.	MAX.		
V_{OH}	Output Voltage High	2.40	3.90		V	$R_{PD} = 360\ \Omega$ to V_{EE} $V_{IN} = -1140$ mV (V_{IHX}) or More Positive (for V_{OH})
V_{OL}	Ouput Voltage Low	−2.0	−1.5	0.4	V	F.O. = 1 ($I_S = 1.6$ mA), No External R_{PD} $V_{IN} = -1450$ mV (V_{ILX}) or More Negative (for V_{OL})
$I_{IN(H)}$	Input Current High		2.25	3.10	mA	$V_{IH} = -900$ mV
$I_{IN(L)}$	Input Current Low		1.75	2.35	mA	$V_{IL} = -1700$ mV
I_{PS}	Power Supply Current	28	37	44	mA	All Inputs Open

CHARACTERISTICS (a.c.) at $V_{CC} = V_{CC\ (AUX)} = 5\ V$; $-V_{EE} = 5.2\ V$; $T_{amb} = 25\ ^{o}C$

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN.	TYP.	MAX.		
t_{pd}	Propagation Delay		6.0	8.0	ns	
t_r	Rise Time	3.0	6.0	8.0	ns	$C_L < 5.0$ pF
t_f	Fall Time	3.0	6.0	8.0	ns	$t_r = t_f = 2.5$ ns (10%–90%)
I_T	Transient Input Current		2.0	3.5	mA	
	Enable Line	2.8	2.8	5.7	mA	

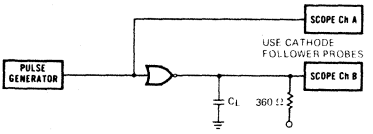
Noise margin specification points



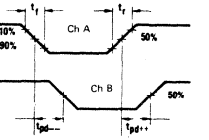
Corner points indicated on the transfer characteristics represent the worst case points (thresholds) at which the device will start to switch. The values V_{ILX} and V_{IHX} define the maximum width of the transition region.

CHARACTERISTICS (continued)

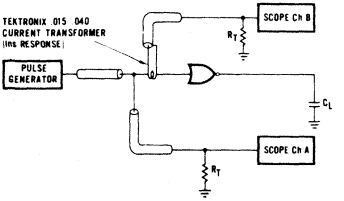
Switching times test circuit and waveforms

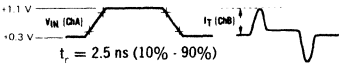


$t_r = t_f$ = 2.5 ns (10% - 90%)
Jig setup with no circuit under test
$V_{CC} = V_{CC}$ (AUX) = +5.0 V
V_{EE} = −5.2 V
C_L = Jig and Stray Capacitance <5.0 pF



Transient input current test circuit and waveforms





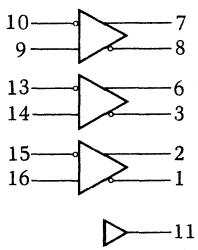
This test provides a measure of the average value of C_{IN}; also current mismatch in the line.
$V_{CC} = V_{CC}$ (AUX) = +5.0 V
V_{EE} = −5.2 V
R_T = 50 Ω Termination of Scope
C_L = Jig and Stray Capacitance <5.0 pF

The GH family of CML silicon monolithic integrated circuits is designed for high speed instrumentation, digital communication systems, central processors and computer terminals. All GH family elements incorporate a unique temperature compensation network which insures that significant parameters such as logic levels, noise margin and speed remain relatively constant over a wide temperature range.

The GHY101/9582 is a circuit comprising three differential input amplifiers, each with both the true and complement outputs. With appropriate connection of the base pins, the device will function as a differential line receiver, Schmitt trigger, high speed comparator, broad band video, i.f. or r.f. amplifier (or oscillator). Reference voltage is made available to allow use of this device as a high input impedance buffer gate.

The GH family corresponds to the ECL9500 series.

LINE RECEIVER/AMPLIFIER



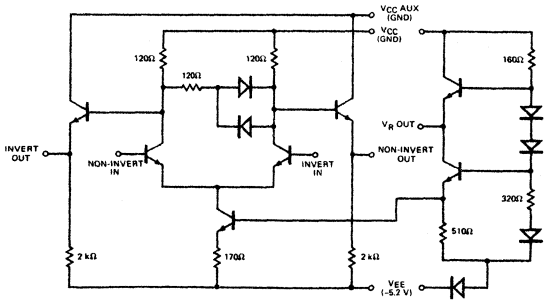
QUICK REFERENCE DATA				
Supply voltage	$-V_{EE}$		5.2	V
Operating ambient temperature range	T_{amb}	0 to	+75	°C
Average propagation delay time	t_{pd}	typ.	2.4	ns
Output voltage HIGH state	$-V_{OH}$	nom.	890	mV
LOW state	$-V_{OL}$	nom.	1710	mV
Power consumption per package	P_{av}	typ.	250	mW

PACKAGE OUTLINE 16 lead ceramic dual in-line (See General Section).

Note

V_{CC} = ground (pins 4 and 5)
$-V_{EE}$ = 5.2 V (pin 12)

CIRCUIT DIAGRAM for one amplifier and the bias driver



For maximum Bandwidth, an additional R_L to V_{EE} of 220 ohms on each output will permit a bandwidth of >80 MHz at 3 dB.
Unused inputs must be grounded.

FUNCTIONAL DESCRIPTION

The GHY101/9582 consits of three differential amplifiers with emitter-follower outputs and a bias driver. This device is designed to be used as a line receiver in applications requiring a medium gain, high bandwidth limiting differential amplifier. The GHY101/9582 is used primarily to receive data from balanced twisted pairs. Any GH gate with differential outputs may be used to drive the twisted pair line, terminated in its characteristic impedance (about 125 Ω).
A voltage divider is formed between the high level gate output, the terminating resistor and the pull-down resistor on the low level gate output. Typically, the voltage swing across the terminating resistor is 260 mV, but any input voltage swing in excess of 160 mV ensure the output levels due to the voltage gain of the circuit. The output of a line receiver is similar to a standard GH gate.
Very long lines may be used with excellent results and the only restriction on line length is series line resitance. A twisted pair transmission line is recommended for clock distribution in high speed systems since distribution skew time may be balanced out by adjusting line lenghts (propagation delay times approximately 1.0 ns per 20 cm of line).
The GHY101/9582 can also be used in many linear applications. The minimum differential voltage gain is 6 with a 3 dB bandwidth of typically 70 MHz.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134).

Supply voltage (d.c.)	$-V_{EE}$	max.	6.0	V
(peak value)	$-V_{EEM}$	max.	8.0	V
Input voltage		0 to	−6.0	V
Output current		max.	40	mA
Storage temperature	T_{stg}	−65 to	+150	°C
Operating ambient temperature	T_{amb}	0 to	+75	°C

DEFINITION OF TERMS

DIFFERENTIAL VOLTAGE GAIN – The ratio of the change in the differential output voltage to the change in voltage between the input terminals producing it.

BANDWIDTH – The frequency at which the differential gain is 3 dB below its low frequency value.

RISE TIME – The time required for an output voltage step to change from 10% to 90% of its final value.

PROPAGATION DELAY – The interval between the application of an input voltage step and its arrival at either output, measured at 50% of the final value.

INPUT RESISTANCE – The resistance seen looking into either input terminal with the other grounded.

INPUT OFFSET CURRENT – The difference between the currents into the two input terminals.

INPUT BIAS CURRENT – The average of the two input currents.

INPUT VOLTAGE RANGE – The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

COMMON MODE REJECTION RATIO – The ratio of a change in input common mode voltage to the resulting change in output offset voltage referred to the input.

SUPPLY VOLTAGE REJECTION RATIO – The ratio of a change in supply voltage to the resulting change in output offset voltage referred to the input.

OUTPUT COMMON MODE VOLTAGE – The average of the voltages at the two output terminals.

OUTPUT VOLTAGE SWING – The peak-to-peak output swing that can be obtained without clipping. This includes the unbalance caused by output offset voltage.

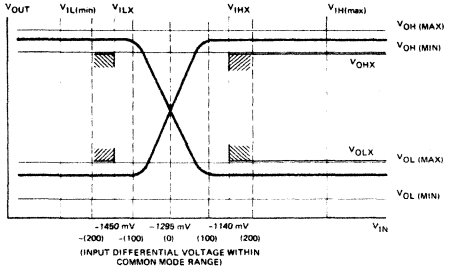
OUTPUT SINK CURRENT – The peak negative current available at either output of the amplifier.

OUTPUT SOURCE CURRENT – Peak positive current available at either output of the amplifier.

OUTPUT RESISTANCE – The resistance seen looking into either output terminal.

CHARACTERISTICS

Noise margin specification points



Corner points indicated on the transfer characteristics represent the worst case points (thresholds) at which the device will start to switch. The values V_{ILX} and V_{IHX} define the maximum width of the transition region.

CHARACTERISTICS For digital applications of the GHY101/9582

D.C. at V_{CC} = ground; $-V_{EE}$ = 5.2 V; T_{amb} = 0 to +75 °C

SYMBOL	CHARACTERISTIC	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	CONDITIONS (Measured with $\overline{\text{Inputs}}$: $\bar{A}_1, \bar{A}_2, \bar{A}_3$; connected to V_R)
V_{OH}	Output Voltage High	−900	−850	−800	mV	F.O. = 1 Gate V_{IL} = −1700 mV for NOR Gate
		−940	−890	−840	mV	F.O. = 5 Gates V_{IH} = −900 mV for OR Gate
		−975	−925	−875	mV	50Ω to −2.0 V
V_{OL}	Output Voltage Low	−1745	−1670	−1595	mV	F.O. = 1 Gate V_{IL} = −1700 mV for OR Gate
		−1785	−1710	−1635	mV	F.O. = 5 Gates V_{IH} = −900 mV for NOR Gate
		−1775	−1700	−1625	mV	50Ω to −2.0 V
V_{OHX}	Ouptut Voltage High at V_{IN} (threshold)	−910			mV	F.O. = 1 Gate V_{ILX} = −1450 mV for NOR Gate } To Each Input Sequentially
		−950			mV	F.O. = 5 Gates V_{IHX} = −1140 mV for OR Gate } To Each Input Sequentially
		−985			mV	50Ω to −2.0 V
V_{OLX}	Ouptut Voltage Low at V_{IN} (threshold)			−1585	mV	F.O. = 1 Gate V_{ILX} = −1450 mV for OR Gate } To Each Input Sequentially
				−1625	mV	F.O. = 5 Gates V_{IHX} = −1140 mV for NOR Gate } To Each Input Sequentially
				−1615	mV	50Ω to −2.0 V
I_{PS}	Power Supply Current	35	48	65	mA	All Inputs Open Except A_1, A_2, A_3 to V_R

A.C. at V_{CC} = ground; $-V_{EE}$ = 5.2 V

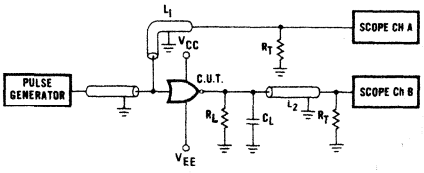
SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	0°C TYP.	0°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+75°C MIN.	+75°C TYP.	+75°C MAX.	UNITS	CONDITIONS
t_{pd}	Propagation Delay											
	t_{pd--}		2.3			2.3	3.5		2.5		ns	
			2.2			2.2	3.5		2.4		ns	R_L = 50Ω to −2.0 V
			2.4			2.4	3.5		2.6		ns	C_L <5.0 pF
			2.5			2.5	3.2		2.7		ns	$t_r = t_f$ = 2.5 ns
t_r	Rise Time		3.0		1.5	3.0	4.5		3.0		ns	
t_f	Fall Time		3.0		1.5	3.0	4.5		3.0		ns	

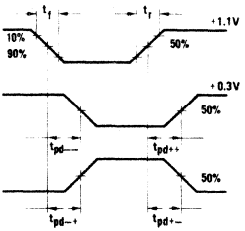
CHARACTERISTICS For linear applications of the GHY101/9582
V_{CC} = ground; $-V_{EE}$ = 5.2 V; T_{amb} = 25 °C

PARAMETER (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Voltage Gain		6.0	7.0		V/V
Bandwidth	Open output		70		MHz
Risetime	R_S = 50Ω		2.5		ns
Propagation Delay	R_S = 50Ω		2.4		ns
Input Resistance			1.3		kΩ
Input Capacitance				5.0	pF
Input Offset Current			7.0		μA
Input Bias Current			40		μA
Input Offset Voltage			5.0		mV
Input Voltage Range	Around V_R	±1.3			V
Common Mode Rejection Ratio	V_{cm} = ±1 V, f ≤ 100 kHz Around V_R	60			dB
Supply Voltage Rejection Ratio	ΔV_S = ±0.5 V	60			dB
Output Common Mode Voltage			−1.3		V
Output Voltage Swing		0.8			Vpp
Output Sink Current		1.3	2.0		mA
Output Source Current				40	mA
Output Resistance			10	20	Ω

CHARACTERISTICS (continued)

Switching times test circuit and waveforms

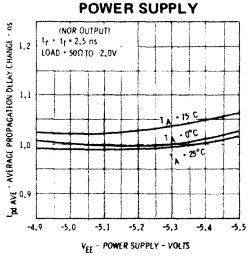




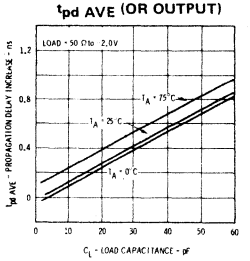
L_1 and L_2 = equal length 50Ω impedance lines
$R_L = R_T$ = 50Ω Termination of Scope
C_L = Jig and Stray Capacitance $<$5,0 pF

$t_r = t_f$ = 2.5 ns (10% – 90%) Jig setup with no circuit under test
$V_{CC} = V_{CC}$ (AUX) = +2.0 V
V_{EE} = –3.2 V

TYPICAL AVERAGE PROPAGATION DELAY CHANGE VERSUS POWER SUPPLY

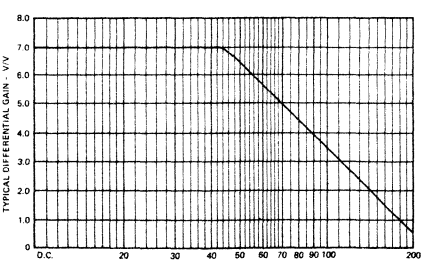


TYPICAL PROPAGATION DELAY INCREASE VERSUS LOAD CAPACITANCE t_{pd} AVE (OR OUTPUT)



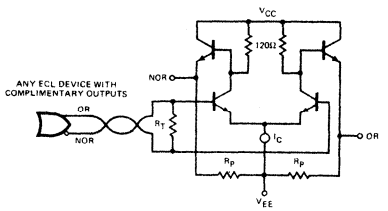
$$t_{pd\ ave} = \frac{t_{pd\ rising} + t_{pd\ falling}}{2}$$

Typical differential gain versus frequency



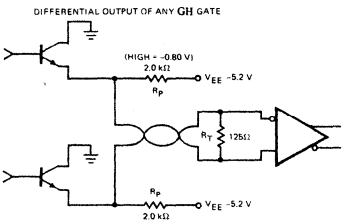
APPLICATION INFORMATION

Twisted pair line receiver



$100\Omega < R_T < 150\Omega$
Driver worst-case R_E = 2.2 kΩ @ R_T = 100Ω
Differential gain = 7.0 V/V
Common mode rejection > 60 dB
Common mode voltage rejection range
(voltages between driver and receiver grounds) = +1.5 V
-1.0 V

Line receiver d.c. equivalent circuit



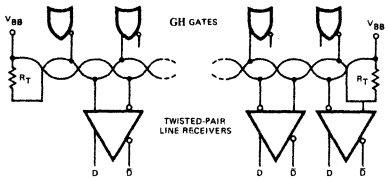
V_R = VOLTAGE DROP ACROSS R_T (TERMINATING RESISTOR)

$$V_R = \frac{(5.2\text{ V} - 0.80\text{ V})\,(R_T)}{2\text{ k}\Omega + R_T}$$

$$= \frac{(4.40)\,(125)}{2125}$$

$$= 260\text{ mV}$$

Data bus driving



System Design Criteria

1. A minimum of two emitter pull-down resistors is recommended in the driver gates.
2. R_T should be Z_{out} of the twisted pair line: 100 to 125 ohms
3. Either OR or NOR outputs may drive the line.
4. All driver gates are ORed together.
5. The line receiver output is Data or $\overline{\text{Data}}$ depending upon the input and output configurations.
6. V_{BB} should be able to source 6.0 mA or sink 7.0 mA total current. This is accomplished by the addition of a 500Ω resistor from V_R (Pin 11) to V_{EE}.

OPERATING NOTES

Interconnection recommendations

All high speed CML circuits demand that special precautions be taken for optimum system performance. A ground plane must be provided for a good, low impedance, ground current return path and to transform interconnections into microstrip transmission lines. The voltage supply lines should be well decoupled with small capacitors throughout each card between V_{EE} and the ground plane and by including at least one larger tantalum capacitor per card.

Typical microstrip lines have a characteristic impedance between 50 and 150 ohms with the lower being more desirable in CML systems. For local interconnects the internal 2 kΩ resistors provide adequate termination but for optimum performance lines longer than 15 cm in length should be terminated in their characteristic impedance.

Microstrip interconnections may be terminated by a resistor: $R = \frac{Z_o}{1 - NZ_o/2000}$ to a −2 V supply where Z_o is the characteristic impedance of the line and N is the number of loads. Alternately, a 2 resistor divider network may be used with $R_1 = 1.6\ R$ connected to ground and $R_2 = 2.6\ R$ connected to V_{EE}.

Coaxial cables or terminated twisted pairs of wire are required for backpanel interconnections longer than 10 cm.

Line driving capability

50 Ω coaxial cables properly terminated may be driven with almost no degradation in the waveform. The normal delay due to the finite speed of the signal traveling down the cable will be encountered in addition to a slight decrease in signal swing. The decrease caused by the attenuation of the cable will lower the noise immunity of the receiving circuit by the same amount.
Care must be exercised to ensure the ground potentials at the driving and receiving ends of a line are equal and no differential noise is present.

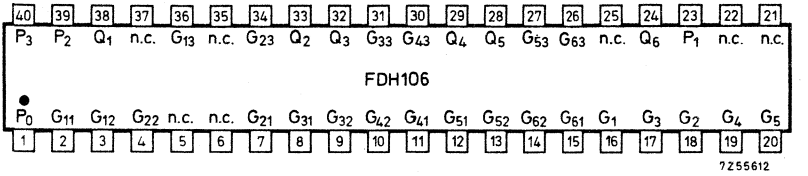
MOS

FD family
SAJ100B

FDH106	arithmetic/logic array
FDH116	control logic array
FDH126	carry array
FDH136	AND-OR gating array
FDH146	variable gate array
FDH156	fixed logic array
FDJ106	register array
FDN106	quadruple 32-bit dynamic SHIFT REGISTER
FDN116	quadruple 32-bit dynamic SHIFT REGISTER
FDN126	variable length 1 to 64-bit dynamic SHIFT REGISTER
FDN136	variable length 1 to 64-bit dynamic SHIFT REGISTER
FDN146	256-bit dynamic SHIFT REGISTER (in 14 lead DIL)
FDN146A	256-bit dynamic SHIFT REGISTER (in TO-100)
FDN156	256-bit dynamic SHIFT REGISTER (in 14 lead DIL)
FDN156A	256-bit dynamic SHIFT REGISTER (in TO-100)
FDN166A	512-bit recirculating dynamic SERIAL MEMORY
FDN186	quadruple 16-bit dynamic SHIFT REGISTER
FDN196A	dual 256-bit dynamic SHIFT REGISTER
FDN206	200-bit dynamic SHIFT REGISTER (in 14 lead DIL)
FDN206A	200-bit dynamic SHIFT REGISTER (in TO-99)
FDN216A	512-bit dynamic SHIFT REGISTER (in TO-100)
FDN216B	512-bit dynamic SHIFT REGISTER (in 14 lead DIL)
FDN506	dual 32-bit static SHIFT REGISTER (in 14 lead DIL)
FDN516A	dual 32-bit static SHIFT REGISTER (in TO-100)
FDN526A	dual 100-bit static SHIFT REGISTER (in TO-100)
FDN536A	dual 100-bit static SHIFT REGISTER (in TO-100)
FDN536B	dual 100-bit static SHIFT REGISTER (in 14 lead DIL)
FDQ106	READ/WRITE random access memory, 128-bit, 64 word, 2-bits per word
FDR116Z	READ-ONLY memory, 512 word, 5-bits per word (bit pattern to customer's specification)
FDR116Z1	READ-ONLY memory, 512 word, 5-bits per word (with fixed bit pattern for alpha numerical 5x7 dot code matrix character generator)
FDR116Z2	CHARACTER GENERATOR (5x7 dot matrix; row scan system)
FDR126Z	READ-ONLY memory, 256 word, 10-bits per word (bit pattern to customer's specification)
FDR126Z1	READ-ONLY memory, 256 word, 10-bits per word (with fixed bit pattern for conversion from ASCII to selectric line code and vica versa)
FDR131Z	READ-ONLY memory, 512 word, 8-bits per word (bit pattern to customer's specification)
FDR131Z1	READ-ONLY memory, 512 word, 8-bits per word (with fixed bit pattern for conversion from ASCII to EBCDIC code and vica versa)
FDR131Z2	CHARACTER GENERATOR (5x7 dot matrix; column scan system)
FDR146Z	READ-ONLY memory, 512 word, 10-bits per word (bit pattern to customer's specification)
FDR146Z1	CHARACTER GENERATOR (7x9 dot matrix; column scan system)
FDR146Z2	CHARACTER GENERATOR upper and lower case (5x7 dot matrix; row scan system)
SAJ100B	MOS frequency divider

The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

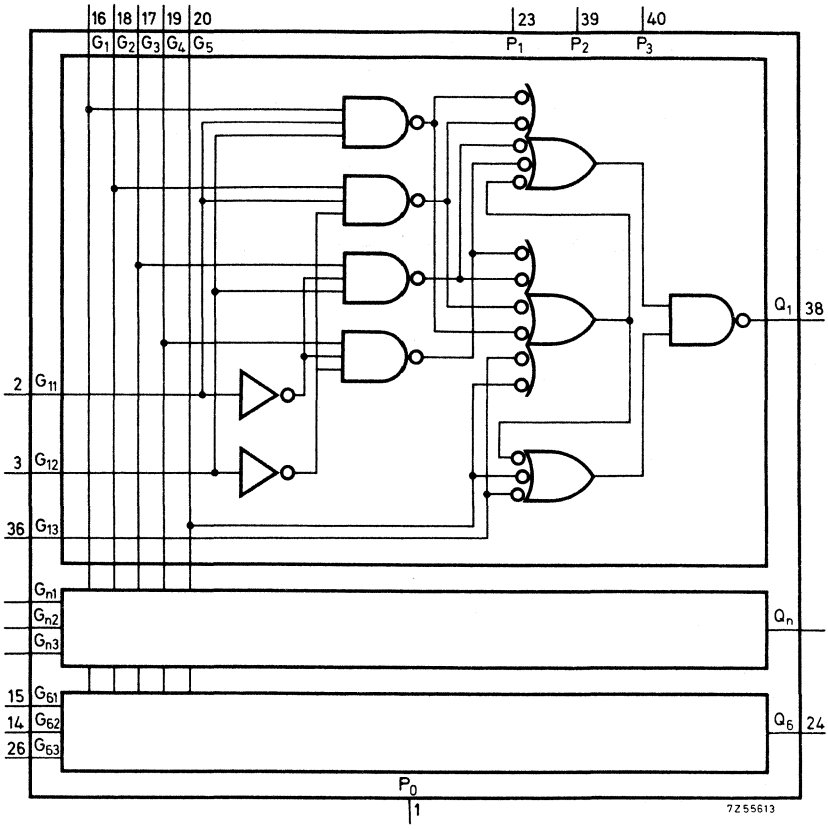
ARITHMETIC/LOGIC ARRAY



P_0 and metal lid on top of the package are connected

QUICK REFERENCE DATA				
Supply voltage	V_{P1}	−24 to −28		V
Operating ambient temperature	T_{amb}	−55 to +85		°C
Average propagation delay				
C_L = 50 pF	t_{pd}	typ.	250	ns
D.C. noise margin	M_H, M_L	>	1.0	V
Average power consumption per function at 1 MHz switching rate	P_{av}	typ.	35	mW

PACKAGE OUTLINE: 40 lead ceramic dual in-line (See General Section)


16 18 17 19 20
G1 G2 G3 G4 G5
23 39 40
P1 P2 P3
2 G11
3 G12
36 G13
Gn1
Gn2
Gn3
15 G61
14 G62
26 G63
Q1 38
Qn
Q6 24
P0
1
7Z55613

GENERAL DESCRIPTION

The FDH106 consists of six, identical, 3-input gate networks. Five coded control lines determine the function of the six gate networks. Each network may function as a full adder/subtractor, or, if used as a 2-input gate, it can provide all logic functions of 2 variables.
Thus one of 32 different functions can be selected by the control lines; the selected function is available six times.
The output voltage swing is determined by the output buffer supply voltage. All inputs are protected against over-voltage caused by static charges.
Inputs G_1 to G_5 have pull-down resistors connected to P_3, so that they assume the LOW state when left floating.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage on all inputs, outputs and supply terminals with reference to P_0		+0.5 to −30	V
Power dissipation up to T_{amb} = 25 °C	P_{tot}	max. 1	W
Junction temperature	T_j	max. 150	°C
Storage temperature	T_{stg}	−65 to +150	°C
Total current through terminal P_3	$-I_{P3}$	max. 40	mA
Output current per output	$\pm I_Q$	max. 20	mA

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	= 125	°C/W

FUNCTION TABLE

G_5 G_4 G_3 G_2 G_1	logic equation (positive logic)	logic function	
		positive logic	negative logic
L L L L L	Q_n = HIGH	–	–
L L L L H	$Q_n = \overline{G_{n1}} + \overline{G_{n2}}$	NAND	NOR
L L L H L	$Q_n = \overline{G_{n1}} + G_{n2}$	–	–
L L L H H	$Q_n = \overline{G_{n1}}$	Complement G_{n1}	Complement G_{n1}
L L H L L	$Q_n = G_{n1} + G_{n2}$	OR	AND
L L H L H	$Q_n = \overline{G_{n1}} \cdot G_{n2} + G_{n1} \cdot \overline{G_{n2}}$	exclusive-OR	comparator
L L H H L	$Q_n = G_{n2}$	transfer G_{n2}	transfer G_{n2}
L L H H H	$Q_n = \overline{G_{n1}} \cdot G_{n2}$	–	–
L H L L L	$Q_n = G_{n1} + \overline{G_{n2}}$	–	–
L H L L H	$Q_n = \overline{G_{n2}}$	Complement G_{n2}	Complement G_{n2}
L H L H L	$Q_n = \overline{G_{n1}} \cdot \overline{G_{n2}} + G_{n1} \cdot G_{n2}$	comparator	exclusive-OR
L H L H H	$Q_n = \overline{G_{n1}} \cdot \overline{G_{n2}}$	NOR	NAND
L H H L L	$Q_n = G_{n1}$	transfer G_{n1}	transfer G_{n1}
L H H L H	$Q_n = G_{n1} \cdot \overline{G_{n2}}$	–	–
L H H H L	$Q_n = G_{n1} \cdot G_{n2}$	AND	OR
L H H H H	Q_n = LOW	–	–

FUNCTION TABLE (continued)

G_5 G_4 G_3 G_2 G_1	logic equation (positive logic)	logic function	
		positive logic	negative logic
H L L L L	$Q_n = \overline{G_{n3}}$	Complement G_{n3}	Complement G_{n3}
H L L L H	$Q_n = \overline{G_{n1}} \cdot \overline{G_{n3}} + \overline{G_{n2}} \cdot \overline{G_{n3}} + G_{n1} \cdot G_{n2} \cdot G_{n3}$	–	–
H L L H L	$Q_n = \overline{G_{n1}} \cdot \overline{G_{n3}} + G_{n2} \cdot \overline{G_{n3}} + G_{n1} \cdot \overline{G_{n2}} \cdot G_{n3}$	–	–
H L L H H	$Q_n = G_{n1} \cdot G_{n3} + \overline{G_{n1}} \cdot \overline{G_{n3}}$	comparator	exclusive-OR
H L H L L	$Q_n = G_{n1} \cdot \overline{G_{n3}} + G_{n2} \cdot \overline{G_{n3}} + \overline{G_{n1}} \cdot \overline{G_{n2}} \cdot G_{n3}$	–	–
H L H L H	$Q_n = G_{n1} \cdot G_{n2} \cdot G_{n3} + G_{n1} \cdot \overline{G_{n2}} \cdot \overline{G_{n3}} + + \overline{G_{n1}} \cdot G_{n2} \cdot \overline{G_{n3}} + \overline{G_{n1}} \cdot \overline{G_{n2}} \cdot G_{n3}$	add	add
H L H H L	$Q_n = G_{n2} \cdot \overline{G_{n3}} + \overline{G_{n2}} \cdot G_{n3}$	exclusive-OR	comparator
H L H H H	$Q_n = G_{n1} \cdot G_{n3} + \overline{G_{n2}} \cdot G_{n3} + \overline{G_{n1}} \cdot G_{n2} \cdot \overline{G_{n3}}$	–	–
H H L L L	$Q_n = G_{n1} \cdot \overline{G_{n3}} + \overline{G_{n2}} \cdot \overline{G_{n3}} + \overline{G_{n1}} \cdot G_{n2} \cdot G_{n3}$	–	–
H H L L H	$Q_n = G_{n2} \cdot G_{n3} + \overline{G_{n2}} \cdot \overline{G_{n3}}$	comparator	exclusive-OR
H H L H L	$Q_n = G_{n1} \cdot G_{n2} \cdot \overline{G_{n3}} + G_{n1} \cdot \overline{G_{n2}} \cdot G_{n3} + + \overline{G_{n1}} \cdot G_{n2} \cdot G_{n3} + \overline{G_{n1}} \cdot \overline{G_{n2}} \cdot \overline{G_{n3}}$	subtract	subtract
H H L H H	$Q_n = G_{n1} \cdot G_{n3} + G_{n2} \cdot G_{n3} + \overline{G_{n1}} \cdot \overline{G_{n2}} \cdot \overline{G_{n3}}$	–	–
H H H L L	$Q_n = G_{n1} \cdot \overline{G_{n3}} + \overline{G_{n1}} \cdot G_{n3}$	exclusive-OR	comparator
H H H L H	$Q_n = \overline{G_{n1}} \cdot G_{n3} + G_{n2} \cdot G_{n3} + G_{n1} \cdot \overline{G_{n2}} \cdot \overline{G_{n3}}$	–	–
H H H H L	$Q_n = \overline{G_{n1}} \cdot G_{n3} + \overline{G_{n2}} \cdot G_{n3} + G_{n1} \cdot G_{n2} \cdot \overline{G_{n3}}$	–	–
H H H H H	$Q_n = G_{n3}$	transfer G_{n3}	transfer G_{n3}

CHARACTERISTICS

Test conditions: V_{P1} = −24 to −28 V; V_{P2} = V_{P3} = −12 to −14 V (see note 1); T_{amb} = −55 to +85 °C; P_0 = grounded; standard load: 50 pF in parallel with 1 MΩ to P_0.

	Symbol	min.	typ.[1]	max.	conditions and references
Input logic levels					
HIGH	V_{GH}	−2	0	+0.3 V	
LOW	V_{GL}	−28	–	−9 V	
Output levels					
HIGH	V_{QH}	−1.0	–	0 V	
LOW	V_{QL}	−14	–	−10 V	
Input capacitance					
G_1;G_2;G_3;G_4;G_5	C_{G1} to C_{G5}	–	5.5	7 pF	bias: V_G=0V; f=1MHz
all other inputs	C_{G11} to C_{G63}	–	3.5	5 pF	bias: V_G=0V; f=1MHz
Input leakage current	$-I_{GL}$	–	–	1 µA	V_G=−15V; T_{amb}=25°C; all other terminals at V_{P0}
Output resistance					
HIGH	R_{QH}	–	1.0	– kΩ	V_Q = −1 V
LOW	R_{QL}	–	2.0	– kΩ	V_Q = −10 V
Supply current (see note 2)	$-I_{P1}$	–	4.6	7.0 mA	f=1MHz; T_{amb}=25°C
	$-I_{P2}$	–	2.0	2.5 mA	
	$-I_{P3}$	–	4.2	6.0 mA	
Output transition times:					
fall time	t_{THL}	–	150	– ns	
rise time	t_{TLH}	–	150	– ns	
Delay times:					
fall time	t_{DHL}	–	250	400 ns	see note 3
rise time	t_{DLH}	–	250	400 ns	
Control input sink current	$-I_{G1}$ to $-I_{G5}$	–	32	– µA	bias: V_G = −2 V

Note 1: V_{P2} is independent of circuit operation and is used for output LOW only.

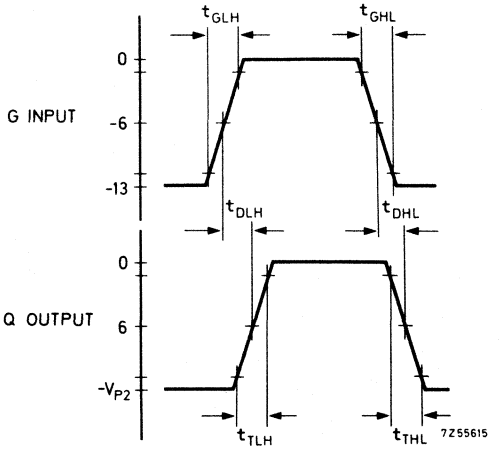
Note 2: Output buffer power supply current is almost entirely dependent on the external load.

Note 3: Delays are measured at −6 V levels of input and output signals.

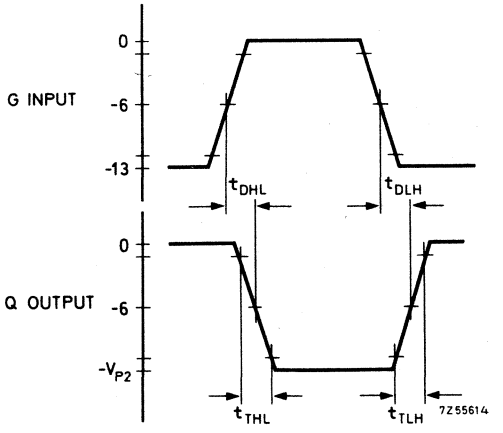
[1]) All typ. values under test conditions: V_{P1} = −26 V; V_{P2} = −13 V; T_{amb} = 25 °C.

CHARACTERISTICS (continued)

TIMING DIAGRAMS



non-inverting function



inverting function

Measurements performed under the following conditions:

V_{P1} = −24 to −28 V; V_{P2} = V_{P3} = −12 to −14 V; t_{GLH} = t_{GHL} = 150 ns.

Note: The indicated points on the vertical axis are specified in the glossary of terms.

CHARACTERISTICS (continued)

GLOSSARY OF TERMS

1. Input signal rise time: t_{GLH}
   The time between the 90% and 10% voltage points as the input pulse goes from LOW to HIGH.

2. Input signal fall time: t_{GHL}
   The time between the 10% and 90% voltage points as the input pulse goes from HIGH to LOW.

3. Rise delay time: t_{DLH}
   The delay between the time the input arrives at its −6 V point and the time the output passes −6 V when going from LOW to HIGH.

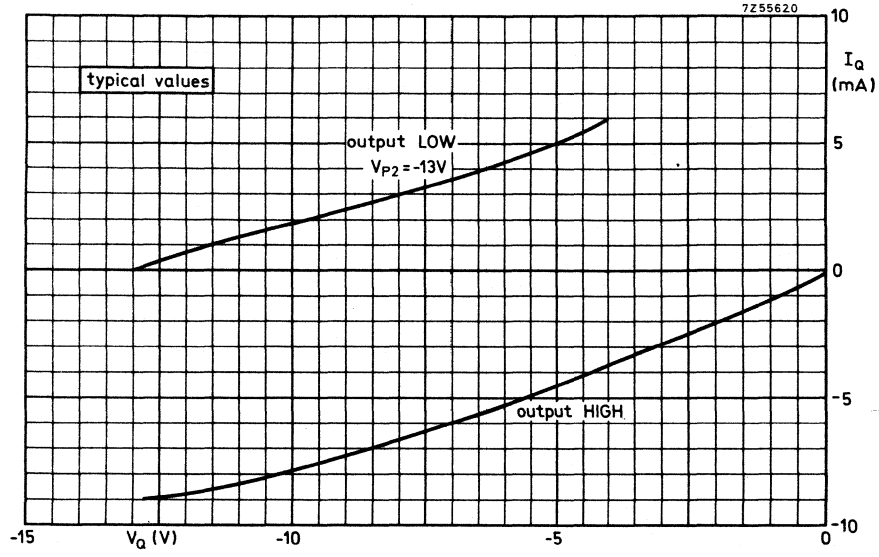
4. Fall delay time: t_{DHL}
   The delay between the time the input arrives at its −6 V point and the time the output passes −6 V when going from HIGH to LOW.

5. Output rise transition time: t_{TLH}
   The time between the 90% and 10% voltage points as the output goes from LOW to HIGH.

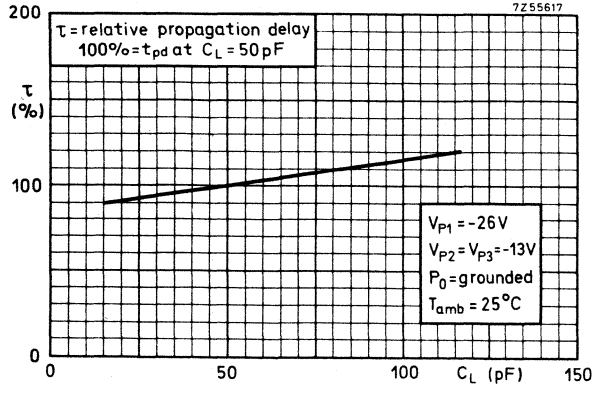
6. Output fall transition time: t_{THL}
   The time between the 10% and 90% voltage points as the output goes from HIGH to LOW.

OUTPUT BUFFER DESCRIPTION

The FDH106 utilizes push-pull output buffers which exhibit the V_Q versus I_Q output curves, for both HIGH and LOW output, shown below.

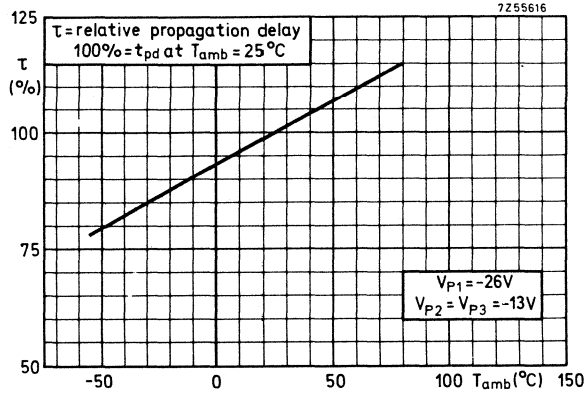


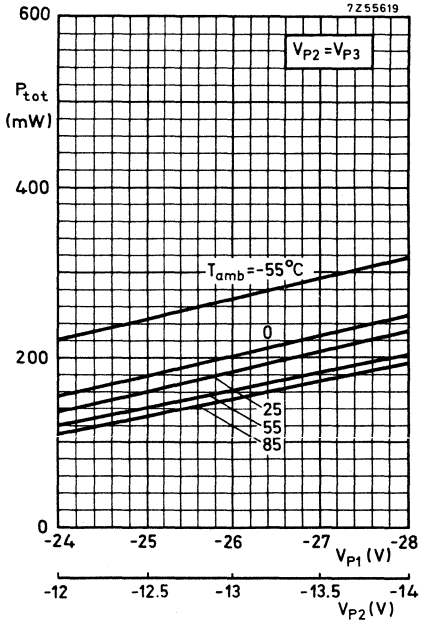
TYPICAL PERFORMANCE at load of C_L in parallel with 1 MΩ to P_0.



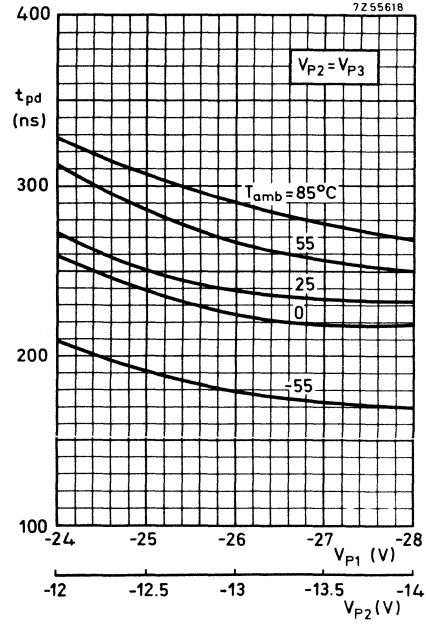
TYPICAL PERFORMANCE (continued)

Test conditions: P_0 = grounded; standard load: 50 pF in parallel with 1 MΩ to P_0.





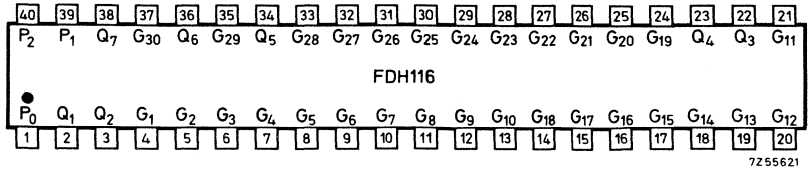
Power dissipation as a function of the supply voltages V_{P1} and V_{P2}



Propagation delay as a function of the supply voltages V_{P1} and V_{P2}

The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

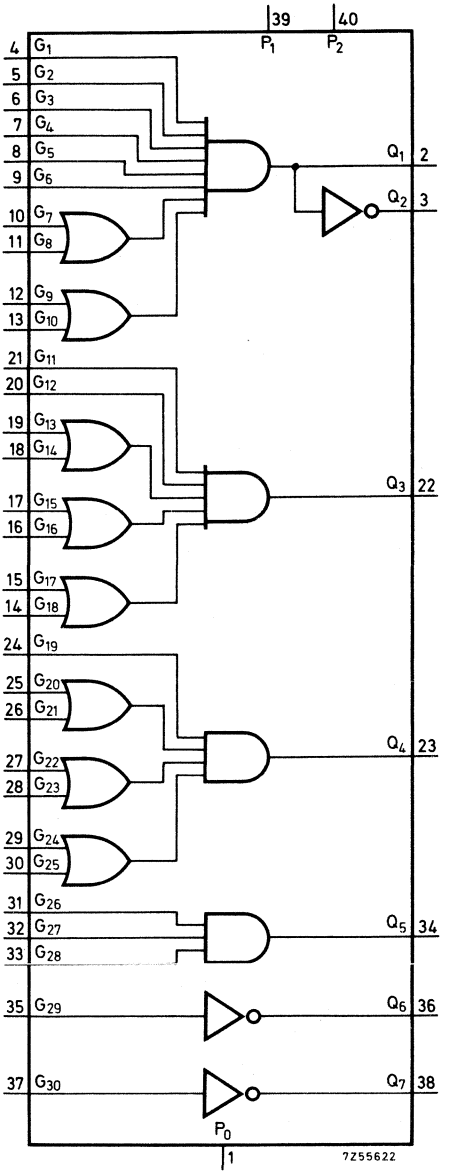
CONTROL LOGIC ARRAY



P_0 and metal lid on top of the package are connected.

QUICK REFERENCE DATA			
Supply voltage	V_{P1}	−24 to −28	V
Operating ambient temperature	T_{amb}	−55 to +85	°C
Power dissipation (f = 1 MHz)	P_{tot}	typ. 150	mW
Average propagation delay	t_{pd}	typ. 250	ns
D.C. noise margin	M_H; M_L	> 1.0	V

PACKAGE OUTLINE 40 lead ceramic dual in-line (See General Section)


39
40
P1
P2
4 G1
5 G2
6 G3
7 G4
8 G5
9 G6
10 G7
11 G8
12 G9
13 G10
21 G11
20 G12
19 G13
18 G14
17 G15
16 G16
15 G17
14 G18
24 G19
25 G20
26 G21
27 G22
28 G23
29 G24
30 G25
31 G26
32 G27
33 G28
35 G29
37 G30
Q1 2
Q2 3
Q3 22
Q4 23
Q5 34
Q6 36
Q7 38
P0
1
7Z55622

GENERAL DESCRIPTION

The FDH116 contains all the logic functions shown in the diagram and described in the logic function on page 4. It is intended to perform the control logic in all MOS digital systems. The output voltage swing is determined by the output buffer supply voltage. All inputs are protected against over-voltage caused by static charges.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage on all inputs, outputs and supply terminals with reference to P_0		+0.5 to −30		V
Power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Junction temperature	T_j	max.	150	°C
Storage temperature	T_{stg}	−65 to	+150	°C
Total current through terminal P_2	$-I_{P2}$	max.	40	mA
Output current (per output)	$\pm I_Q$	max.	20	mA

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$	=	125	°C/W

LOGIC FUNCTIONS

Positive logic

$$Q_1 = G_1 \cdot G_2 \cdot G_3 \cdot G_4 \cdot G_5 \cdot G_6 \cdot (G_7 + G_8) \cdot (G_9 + G_{10})$$

$$Q_2 = \overline{G_1 \cdot G_2 \cdot G_3 \cdot G_4 \cdot G_5 \cdot G_6 \cdot (G_7 + G_8) \cdot (G_9 + G_{10})}$$

$$Q_3 = G_{11} \cdot G_{12} \cdot (G_{13} + G_{14}) \cdot (G_{15} + G_{16}) \cdot (G_{17} + G_{18})$$

$$Q_4 = G_{19} \cdot (G_{20} + G_{21}) \cdot (G_{22} + G_{23}) \cdot (G_{24} + G_{25})$$

$$Q_5 = G_{26} \cdot G_{27} \cdot G_{28}$$

$$Q_6 = \overline{G_{29}}$$

$$Q_7 = \overline{G_{30}}$$

Negative logic

$$Q_1 = G_1 + G_2 + G_3 + G_4 + G_5 + G_6 + G_7 \cdot G_8 + G_9 \cdot G_{10}$$

$$Q_2 = \overline{G_1 + G_2 + G_3 + G_4 + G_5 + G_6 + G_7 \cdot G_8 + G_9 \cdot G_{10}}$$

$$Q_3 = G_{11} + G_{12} + (G_{13} \cdot G_{14}) + (G_{15} \cdot G_{16}) + (G_{17} \cdot G_{18})$$

$$Q_4 = G_{19} + (G_{20} \cdot G_{21}) + (G_{22} \cdot G_{23}) + (G_{24} \cdot G_{25})$$

$$Q_5 = G_{26} + G_{27} + G_{28}$$

$$Q_6 = \overline{G_{29}}$$

$$Q_7 = \overline{G_{30}}$$

CHARACTERISTICS

Test conditions: V_{P1} = −24 to −28 V; V_{P2} = −12 to −14 V (see note 1); T_{amb} = −55 to +85 °C; P_0 = grounded; standard load: 50 pF in parallel with 1 MΩ to P_0.

	Symbol	min.	typ. [1])	max.		Conditions and references
Input logic levels						
HIGH	V_{GH}	−2	–	+0.3	V	
LOW	V_{GL}	−28	–	−9	V	
Output levels						
HIGH	V_{QH}	−1.0	–	0	V	
LOW	V_{QL}	−14	–	−10	V	
Input capacitance						
G_{29}; G_{30}	C_{G29}, C_{G30}	–	5	7	pF	bias: V_G = 0 V
all other inputs	C_{G1} to C_{G28}	–	3.5	5	pF	f = 1 MHz
Input leakage current	$-I_{GL}$	–	–	1	μA	V_G = −15 V; all other terminals at V_{P0}; T_{amb} = 25 °C
Output resistance						
HIGH	R_{QH}	–	1	–	kΩ	V_Q = −1 V
LOW	R_{QL}	–	2	–	kΩ	V_Q = −10 V
Supply currents	$-I_{P1}$	–	4.6	6.5	mA	f=1MHz; T_{amb}=25°C; see note 2
	$-I_{P2}$	–	2.3	3.0	mA	
Output transition times:						
fall time	t_{THL}	–	150	–	ns	
rise time	t_{TLH}	–	150	–	ns	
Delay times:						
G → Q_1; Q_3; Q_4; Q_5	t_{DHL}, t_{DLH}	–	150	250	ns	see note 3
G → Q_6; Q_7	t_{DHL}, t_{DLH}	–	125	250	ns	
G → Q_2	t_{DHL}, t_{DLH}	–	175	300	ns	

1) All typ. values measured at: T_{amb} = 25 °C; V_{P1} = −26 V; V_{P2} = −13 V

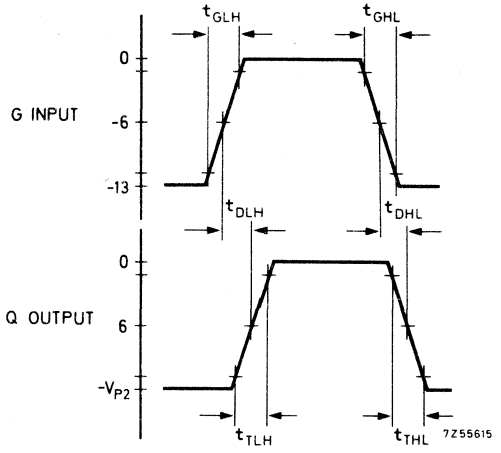
Note 1: V_{P2} is independent of circuit operation and is used for output LOW only.

Note 2: Output buffer power supply current is almost entirely dependent on the external load.

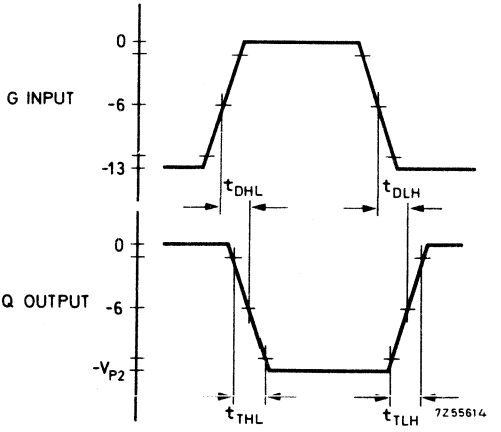
Note 3: Delays are measured at −6 V levels of input and output signals.
(see also timing diagram on page 6).

CHARACTERISTICS (continued)

TIMING DIAGRAMS



non-inverting function



inverting function

Measurements performed under the following conditions:

V_{P1} = −24 to −28 V; V_{P2} = −12 to −14 V; $t_{GLH} = t_{GHL}$ = 150 ns.

Note: The indicated points on the vertical axis are specified in the glossary of terms.

CHARACTERISTICS (continued)

GLOSSARY OF TERMS

1. **Input signal rise time:** t_{GLH}
   The time between the 90 % and 10 % voltage points as the input pulse goes from LOW to HIGH.

2. **Input signal fall time:** t_{GHL}
   The time between the 10 % and 90 % voltage points as the input pulse goes from HIGH to LOW.

3. Rise delay time: t_{DLH}
   The delay between the time the input arrives at its -6 V point and the time the output passes −6 V when going from LOW to HIGH.

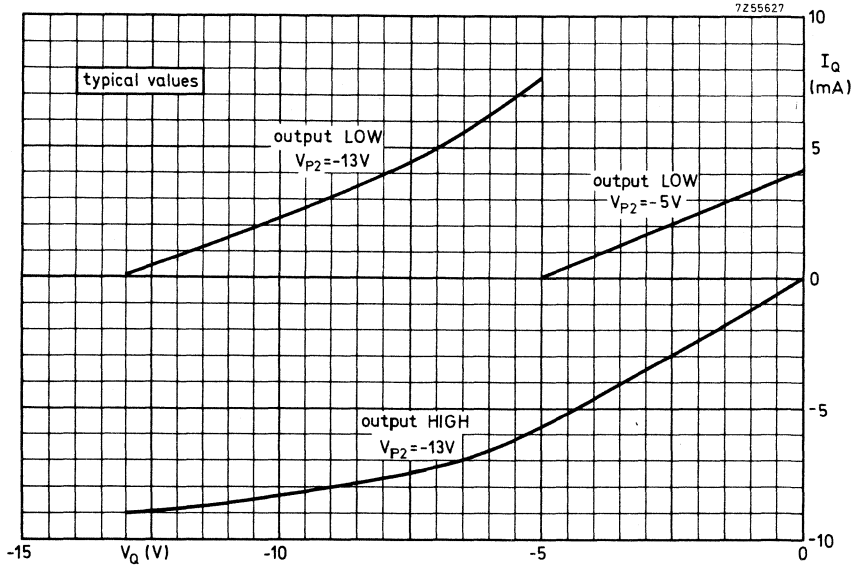
4. Fall delay time: t_{DHL}
   The delay between the time the input arrives at its −6 V point and the time the output passes −6 V when going from HIGH to LOW.

5. Output rise transition time: t_{TLH}
   The time between the 90 % and 10 % voltage points as the output goes from LOW to HIGH.

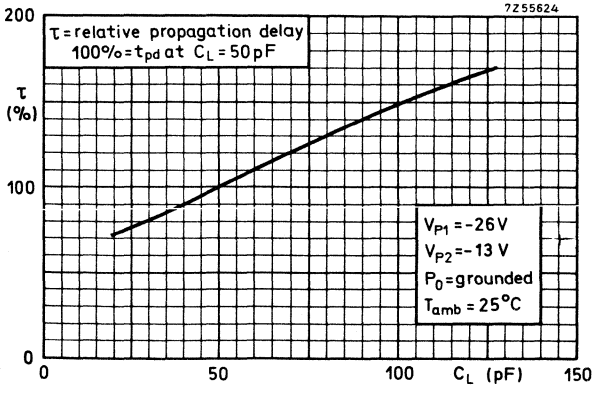
6. Output fall transition time: t_{THL}
   The time between the 10 % and 90 % voltage points as the output goes from HIGH to LOW.

OUTPUT BUFFER DESCRIPTION

The FDH116 utilizes push-pull output buffers which exhibit the V_Q versus I_Q output curves, for both HIGH and LOW output, shown below.

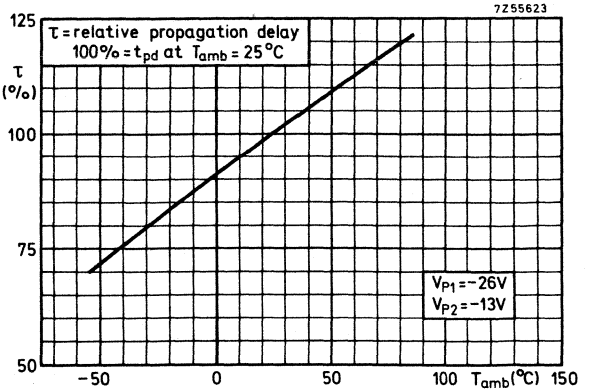


TYPICAL PERFORMANCE at load of C_L in parallel with 1 MΩ to P_0.

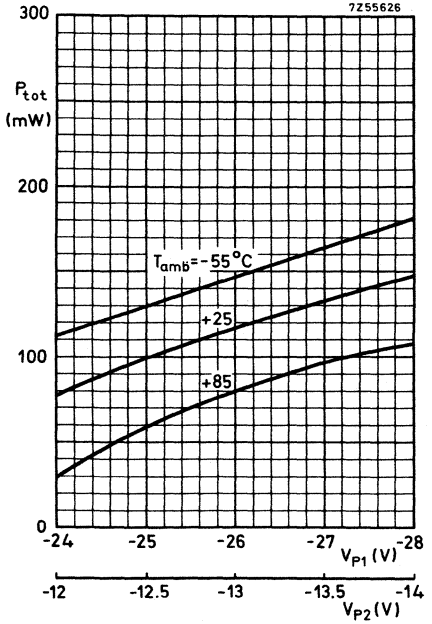


TYPICAL PERFORMANCE (continued)

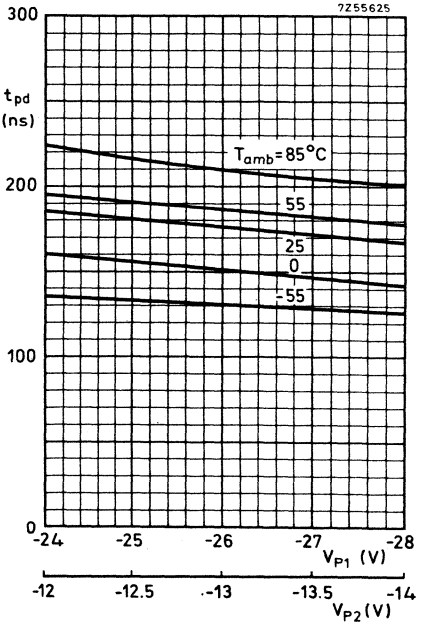
Test conditions: P_0 = grounded; standard load of 50 pF in parallel with 1 MΩ to P_0.



Rated proparation delay as a function of ambient temperature.



Power dissipation as a function of the supply voltage V_{P_1} and V_{P_2}

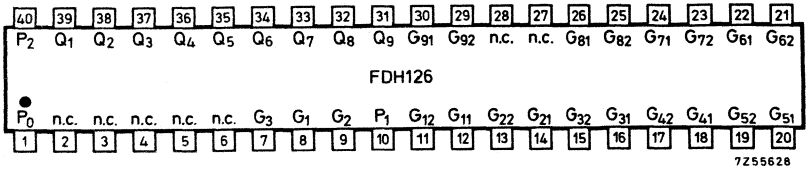


Propagation delay of Q_2 (slowest output) as a function of the supply voltages V_{P_1} and V_{P_2}.

Note: output buffer power dissipation not included, since it is entirely dependent of loading conditions

The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

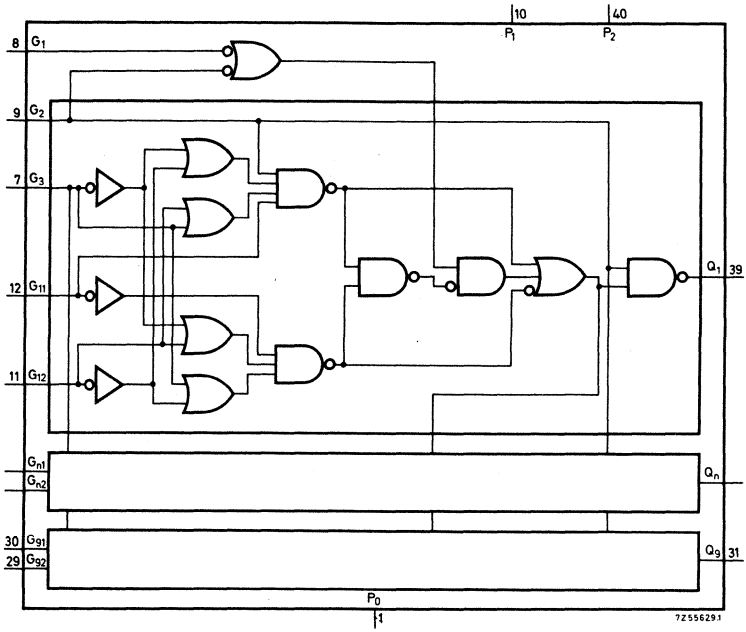
CARRY ARRAY



P_0 and metal lid on top of the package are connected.

QUICK REFERENCE DATA				
Supply voltage	V_{P1}	−24 to −28		V
Operating ambient temperature	T_{amb}	−55 to +85		°C
Average propagation delay C_L = 50 pF; T_{amb} = 25 °C	t_{pd}	typ.	250	ns
D.C. noise margin	M_H, M_L	>	1.0	V
Power dissipation (f = 1 MHz)	P_{tot}	typ.	260	mW

PACKAGE OUTLINE 40 lead ceramic dual in-line (See General Section)


10
P1
40
P2
8 G1
9 G2
7 G3
12 G11
11 G12
Gn1
Gn2
30 G91
29 G92
Q1 39
Qn
Q9 31
P0
1
7Z556293

GENERAL DESCRIPTION

The FDH126 contains CARRY propagation circuits for a nine stage binary adder/subtractor. It can be cascaded for longer word lengths.
The device is intended to cooperate with the FDH106; e.g. three FDH106 and two FDH126 packages can be put together to make an 18-bit parallel adder/subtractor.
By combining all the CARRY circuits in the same package, a very fast CARRY propagation is obtained.
All inputs are protected against over-voltage caused by static changes.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage on all inputs, outputs and supply terminals with reference to P_0		+0.5 to	−30	V
Power dissipation up to T_{amb} = 70 °C	P_{tot}	max.	1	W
Junction temperature	T_j	max.	150	°C
Storage temperature	T_{stg}	−65 to	+150	°C
Total current through terminal P_2	$-I_{P2}$	max.	40	mA
Current per output	$\pm I_Q$	max.	20	mA

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$	=	125	°C/W

FUNCTION TABLE

G_2	G_3	Q_{n-1}	G_{n1}	G_{n2}	Q_n
H	X	H	H	X	H
H	H	H	L	H	L
H	H	H	L	L	H
H	H	L	H	H	L
H	H	L	H	L	H
H	X	L	L	X	L
H	L	H	L	H	H
H	L	H	L	L	L
H	L	L	H	H	H
H	L	L	H	L	L
L	X	X	X	X	L

For n = 1:

$Q_{n-1} = G_1$

H = HIGH state (the less negative voltage)
L = LOW state (the more negative voltage)
X = state is immaterial

LOGIC FUNCTION

Positive logic:

$$Q_n = G_2 \cdot \{G_{n1} \cdot (\overline{G_3} \cdot G_{n2} + G_3 \cdot \overline{G_{n2}}) + Q_{n-1}\,(G_{n1} + \overline{G_3} \cdot G_{n2} + G_3 \cdot \overline{G_{n2}})\}$$

Negative logic:

$$Q_n = G_2 + G_{n1} \cdot (G_3 \cdot G_{n2} + \overline{G_3} \cdot \overline{G_{n2}}) + Q_{n-1}\,(G_{n1} + G_3 \cdot G_{n2} + \overline{G_3} \cdot \overline{G_{n2}})$$

CHARACTERISTICS

Test conditions: V_{P1} = −24 to −28 V; V_{P2} = −12 to −14 V; T_{amb} = −55 to +85 °C
P_0 = grounded; standard load for Q_8 and Q_9: 50 pF in parallel with 1MΩ to P_0; for Q_1 to Q_7 , 25 pF in parallel with 1MΩ to P_0.

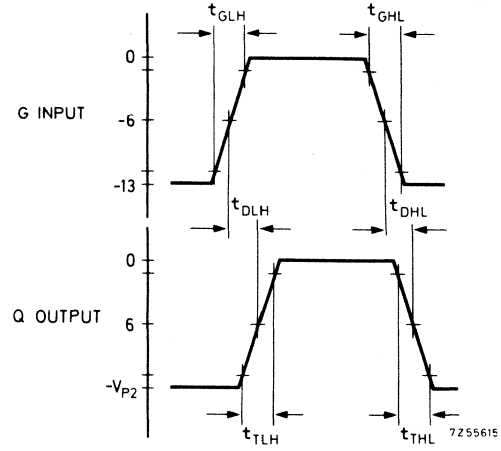
	Symbol	min.	typ.[1]	max.		Conditions and references
Input logic levels						
HIGH	V_{GH}	−2	0	+0.3	V	
LOW	V_{GL}	−28	–	−9	V	
Output levels						
HIGH	V_{QH}	−1.0	–	0	V	
LOW	V_{QL}	−14	–	−10	V	
Input capacitance						
G_1; G_{11} to G_{92}	C_G	–	4.5	6.0	pF	bias: V_G=0 V; f=1 MHz
G_2	C_{G2}	–	6.8	9.0	pF	
G_3	C_{G3}	–	9.5	12.5	pF	
Input leakage current	$-I_{GL}$	–	–	1	μA	V_G=−15 V; T_{amb}=25 °C; all other terminals at V_{P0}
Output resistance						
Q_1 to Q_7	R_{QH}	–	1.4	–	kΩ	V_Q = −1 V
	R_{QL}	–	3.7	–	kΩ	V_Q = −10 V
Q_8; Q_9	R_{QH}	–	0.5	–	kΩ	V_Q = −1 V
	R_{QL}	–	1.7	–	kΩ	V_Q = −10 V
Supply currents	$-I_{P1}$	–	8.0	13.0	mA	f = 1 MHz; T_{amb} = 25 °C
	$-I_{P2}$	–	4.0	6.0	mA	
Output transition times:						
fall time	t_{THL}	–	150	–	ns	
rise time	t_{TLH}	–	100	–	ns	
Delay times: (any input to output)						
fall time	t_{DHL}	–	250	500	ns	see note
rise time	t_{DLH}	–	250	500	ns	

[1]) All typ. values measured at: V_{P1} = −26 V; V_{P2} = −13 V; T_{amb} = 25 °C.

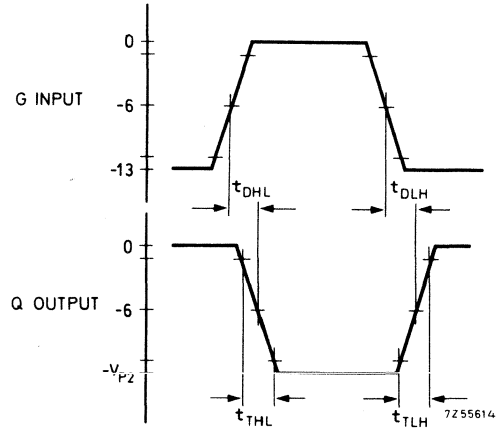
Note: Delays are measured at −6 V levels of input and output signals.
(see also timing diagrams on page 6)

CHARACTERISTICS (continued)

TIMING DIAGRAMS



non-inverting function



inverting function

Measurements performed under the following conditions:

V_{P1} = −24 to −28 V; V_{P2} = −12 to −14 V; $t_{GLH} = t_{GHL}$ = 150 ns.

Note: The indicated points on the vertical axis are specified in the glossary of terms.

CHARACTERISTICS (continued)

GLOSSARY OF TERMS

1. Input signal rise time: t_{GLH}
   The time between the 90% and 10% voltage points as the input pulse goes from LOW to HIGH.

2. Input signal fall time: t_{GHL}
   The time between the 10% and 90% voltage points as the input pulse goes from HIGH to LOW.

3. Rise delay time: t_{DLH}
   The delay between the time the input arrives at its −6 V point and the time the output passes −6 V when going from LOW to HIGH.

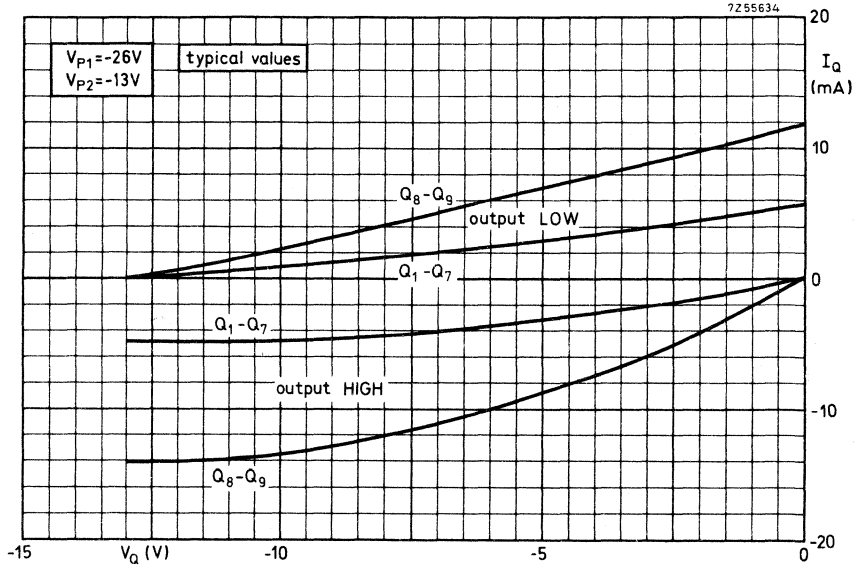
4. Fall delay time: t_{DHL}
   The delay between the time the input arrives at its −6 V point and the time the output passes −6 V when going from HIGH to LOW.

5. Output rise transition time: t_{TLH}
   The time between the 90% and 10% voltage points as the output goes from LOW to HIGH.

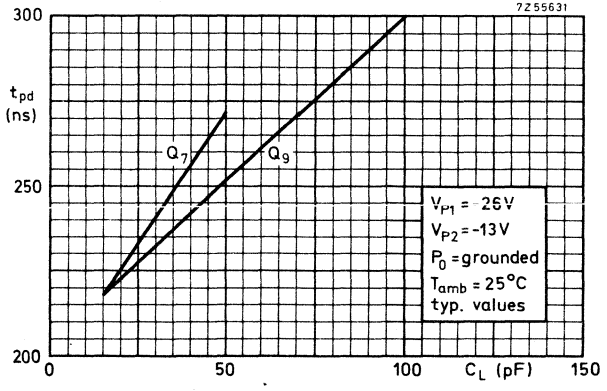
6. Output fall transition time: t_{THL}
   The time between the 10% and 90% voltage points as the output goes from HIGH to LOW.

OUTPUT BUFFER DESCRIPTION

The FDH126 utilizes push-pull output buffers which exhibit the V_Q versus I_Q output curves, for both HIGH and LOW output, shown below.

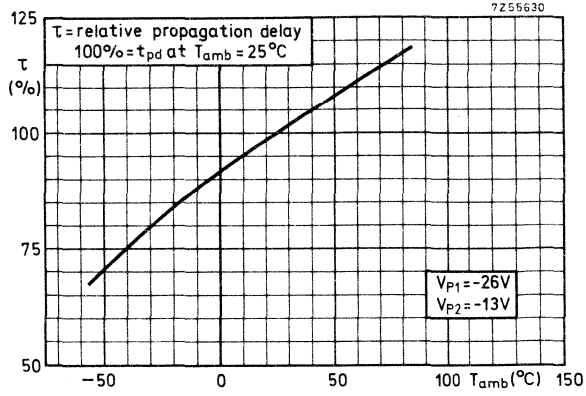


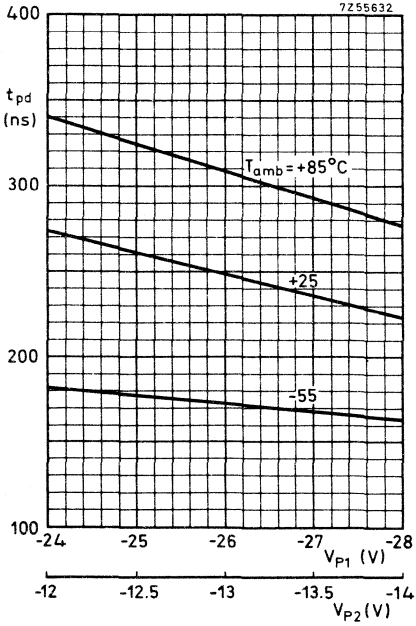
TYPICAL PERFORMANCE at load: C_L in parallel with 1 MΩ to P_0.



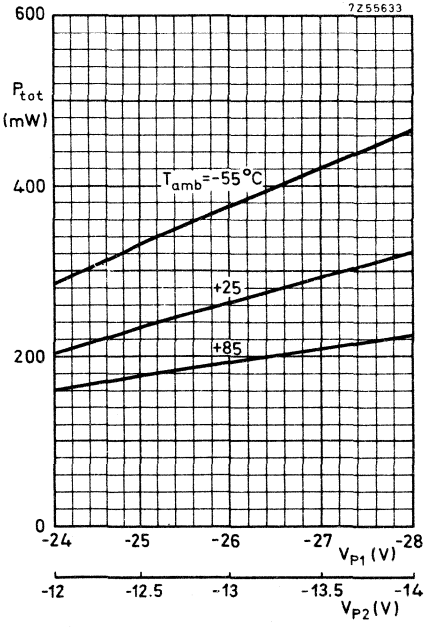
TYPICAL PERFORMANCE (continued)

Test conditions: P_0 = grounded; standard load: 50 pF in parallel with 1 MΩ to P_0.





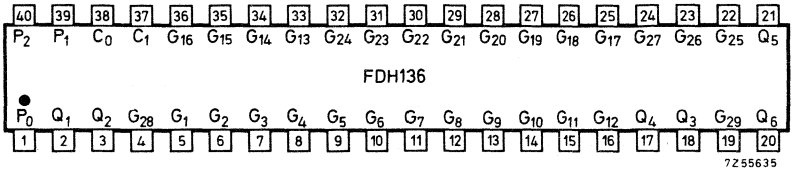
Power dissipation as a function of the supply voltages V_{P1} and V_{P2}



Propagation delay as a function of the supply voltages V_{P1} and V_{P2}

The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

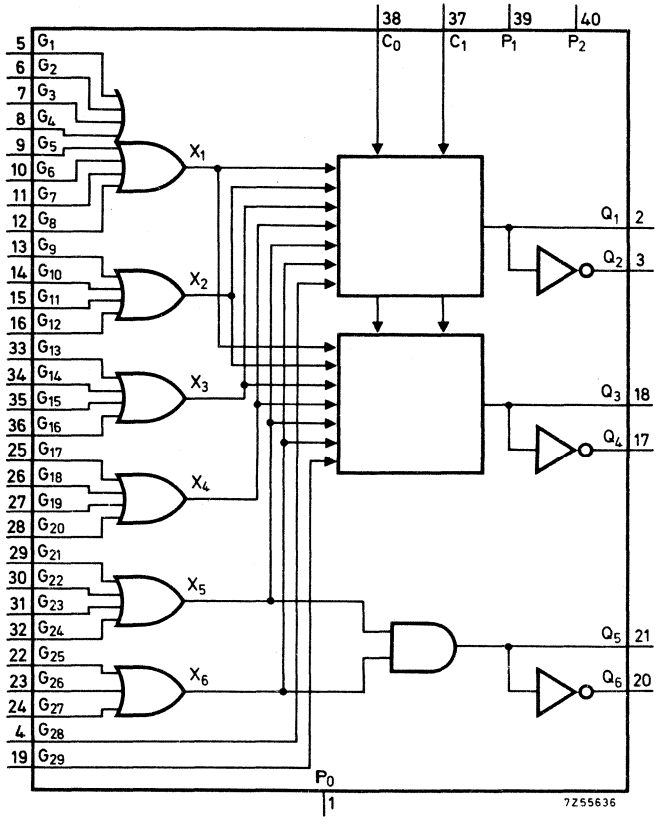
AND-OR GATING ARRAY



P_0 and metal lid on top of the package are connected.

QUICK REFERENCE DATA				
Supply voltage	V_{P1}	−24 to −28		V
Operating ambient temperature	T_{amb}	−55 to +85		°C
Average propagation delay C_L = 50 pF; T_{amb} = 25 °C	t_{pd}	typ.	180	ns
D.C. noise margin	M_H, M_L	>	1.0	V
Power consumption (f = 1 MHz)	P_{tot}	typ.	230	mW

PACKAGE OUTLINE 40 lead ceramic dual in-line (See General Section)


38 C0
37 C1
39 P1
40 P2
5 G1
6 G2
7 G3
8 G4
9 G5
10 G6
11 G7
12 G8
13 G9
14 G10
15 G11
16 G12
33 G13
34 G14
35 G15
36 G16
25 G17
26 G18
27 G19
28 G20
29 G21
30 G22
31 G23
32 G24
22 G25
23 G26
24 G27
4 G28
19 G29
X1
X2
X3
X4
X5
X6
Q1 2
Q2 3
Q3 18
Q4 17
Q5 21
Q6 20
P0 1
7Z55636

GENERAL DESCRIPTION

The FDH136 contains general purpose, expandable OR/AND/NAND gates.
Two control lines C_0 and C_1 provide four different logic configurations, as shown in the function table.
Complementary outputs are available.
All inputs are protected against over-voltages caused by static charges.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage on all inputs, outputs and supply terminals with reference to P_0			+0.5 to −30	V
Power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Junction temperature	T_j	max.	150	°C
Storage temperature	T_{stg}		−65 to +150	°C
Total current through terminal P_2	$-I_{P2}$	max.	40	mA
Output current (per output)	$\pm I_Q$	max.	20	mA

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$	=	125	°C/W

FUNCTION TABLE

C_0	C_1	logic equation	
		positive logic	negative logic
X	X	$X_1 = G_1 + G_2 + G_3 + G_4 + G_5 + G_6 + G_7 + G_8$	$X_1 = G_1 \cdot G_2 \cdot G_3 \cdot G_4 \cdot G_5 \cdot G_6 \cdot G_7 \cdot G_8$
		$X_2 = G_9 + G_{10} + G_{11} + G_{12}$	$X_2 = G_9 \cdot G_{10} \cdot G_{11} \cdot G_{12}$
		$X_3 = G_{13} + G_{14} + G_{15} + G_{16}$	$X_3 = G_{13} \cdot G_{14} \cdot G_{15} \cdot G_{16}$
		$X_4 = G_{17} + G_{18} + G_{19} + G_{20}$	$X_4 = G_{17} \cdot G_{18} \cdot G_{19} \cdot G_{20}$
		$X_5 = G_{21} + G_{22} + G_{23} + G_{24}$	$X_5 = G_{21} \cdot G_{22} \cdot G_{23} \cdot G_{24}$
		$X_6 = G_{25} + G_{26} + G_{27}$	$X_6 = G_{25} \cdot G_{26} \cdot G_{27}$
		$Q_5 = X_5 \cdot X_6$	$Q_5 = X_5 + X_6$
		$Q_6 = \overline{X_5} + \overline{X_6}$	$Q_6 = \overline{X_5} \cdot \overline{X_6}$
L	L	$Q_1 = X_1 \cdot X_2 \cdot X_3 \cdot G_{28}$	$Q_1 = X_1 + X_2 + X_3 + G_{28}$
		$Q_2 = \overline{X_1} + \overline{X_2} + \overline{X_3} + \overline{G_{28}}$	$Q_2 = \overline{X_1} \cdot \overline{X_2} \cdot \overline{X_3} \cdot \overline{G_{28}}$
		$Q_3 = X_4 \cdot X_5 \cdot X_6 \cdot G_{29}$	$Q_3 = X_4 + X_5 + X_6 + G_{29}$
		$Q_4 = \overline{X_4} + \overline{X_5} + \overline{X_6} + \overline{G_{29}}$	$Q_4 = \overline{X_4} \cdot \overline{X_5} \cdot \overline{X_6} \cdot \overline{G_{29}}$

FUNCTION TABLE (continued)

C_0	C_1	logic equation	
		positive logic	negative logic
L	H	$Q_1 = X_1 \cdot X_2 \cdot X_3 \cdot X_4 \cdot X_5 \cdot X_6 \cdot G_{28}$ $Q_2 = \overline{X_1} + \overline{X_2} + \overline{X_3} + \overline{X_4} + \overline{X_5} + \overline{X_6} + \overline{G_{28}}$ $Q_3 = X_1 \cdot X_2 \cdot G_{29}$ $Q_4 = \overline{X_1} + \overline{X_2} + \overline{G_{29}}$	$Q_1 = X_1 + X_2 + X_3 + X_4 + X_5 + X_6 + G_{28}$ $Q_2 = \overline{X_1} \cdot \overline{X_2} \cdot \overline{X_3} \cdot \overline{X_4} \cdot \overline{X_5} \cdot \overline{X_6} \cdot \overline{G_{28}}$ $Q_3 = X_1 + X_2 + G_{29}$ $Q_4 = \overline{X_1} \cdot \overline{X_2} \cdot \overline{G_{29}}$
H	L	$Q_1 = X_1 \cdot X_2 \cdot G_{28}$ $Q_2 = \overline{X_1} + \overline{X_2} + \overline{G_{28}}$ $Q_3 = X_3 \cdot X_4 \cdot G_{29}$ $Q_4 = \overline{X_3} + \overline{X_4} + \overline{G_{29}}$	$Q_1 = X_1 + X_2 + G_{28}$ $Q_2 = \overline{X_1} \cdot \overline{X_2} \cdot \overline{G_{28}}$ $Q_3 = X_3 + X_4 + G_{29}$ $Q_4 = \overline{X_3} \cdot \overline{X_4} \cdot \overline{G_{29}}$
H	H	$Q_1 = X_1 \cdot X_2 \cdot X_3 \cdot X_4 \cdot G_{28}$ $Q_2 = \overline{X_1} + \overline{X_2} + \overline{X_3} + \overline{X_4} + \overline{G_{28}}$ $Q_3 = X_5 \cdot X_6 \cdot G_{29}$ $Q_4 = \overline{X_5} + \overline{X_6} + \overline{G_{29}}$.	$Q_1 = X_1 + X_2 + X_3 + X_4 + G_{28}$ $Q_2 = \overline{X_1} \cdot \overline{X_2} \cdot \overline{X_3} \cdot \overline{X_4} \cdot \overline{G_{28}}$ $Q_3 = X_5 + X_6 + G_{29}$ $Q_4 = \overline{X_5} \cdot \overline{X_6} \cdot \overline{G_{29}}$

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

CHARACTERISTICS

Test conditions: V_{P1} = −24 to −28 V; V_{P2} = −12 to −14 V; T_{amb} = −55 to +85 °C; P_0 = grounded; standard load : 50 pF in parallel with 1 MΩ to P_0.

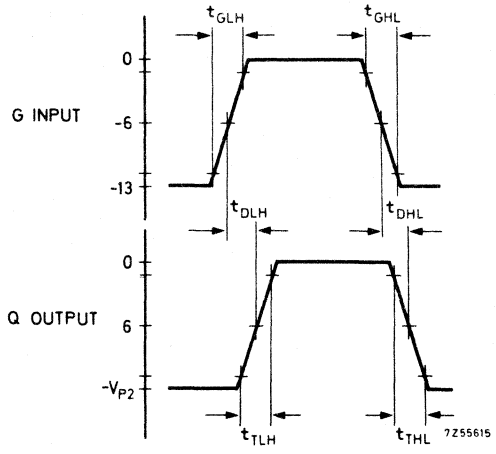
	Symbol	min.	typ.[1]	max.		Conditions and references
Input logic levels						
HIGH	V_{GH}, V_{CH}	−2	–	+0.3	V	
LOW	V_{GL}, V_{CL}	−28	–	−9	V	
Output levels						
HIGH	V_{QH}	−1.0	–	0	V	
LOW	V_{QL}	−14	–	−10	V	
Input capacitance	G_G, C_C	–	3	5.5	pF	bias: $V_G = V_C = 0$ V; f = 1 MHz
Leakage current	$-I_{GL}$, $-I_{CL}$	–	–	1	mA	$V_G = V_C = -15$ V; T_{amb} = 25 °C; all other terminals at V_{P0}
Output resistance						
HIGH	R_{QH}	–	0.4	–	kΩ	V_Q = −1V
LOW	R_{QL}	–	1	–	kΩ	V_Q = −10V
Supply currents	$-I_{P1}$	–	4.5	7.5	mA	f = 1 MHz; T_{amb} = 25 °C
	$-I_{P2}$	–	8	13	mA	
Output transition times:						
fall time	t_{THL}	–	150	–	ns	
rise time	t_{TLH}	–	150	–	ns	
Delay times: (any input to output)						
fall time	t_{DHL}	–	180	400	ns	
rise time	t_{DLH}	–	180	400	ns	
Control input sink current: G_1;G_2;G_4;G_5; G_7;G_8;G_{10};G_{12}, G_{13}; G_{15};G_{17};G_{19};G_{21};G_{23}; G_{26};C_0;C_1	$-I_G$, $-I_C$	–	25	–	µA	$V_G = V_C = -2$ V; see note

[1]) Typical values are measured at V_{P1} = −26 V; V_{P2} = −13 V; T_{amb} = 25 °C.

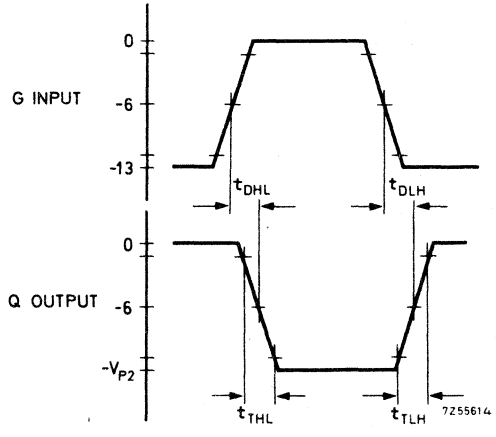
Note: Inputs mentioned are provided with a pull-down resistor to terminal P_2. These inputs, when not used, may be left floating; they will then be in the LOW state.

CHARACTERISTICS (continued)

TIMING DIAGRAMS



non-inverting function



inverting function

Measurements performed under the following conditions:

V_{P1} = −24 to −28 V; V_{P2} = −12 to −14 V; $t_{GLH} = t_{GHL}$ = 150 ns.

Note: The indicated points on the vertical axis are specified in the glossary of terms.

CHARACTERISTICS (continued)

GLOSSARY OF TERMS

1. Input signal rise time: t_{GLH}
   The time between the 90% and 10% voltage points as the input pulse goes from LOW to HIGH.

2. Input signal fall time: t_{GHL}
   The time between the 10% and 90% voltage points as the input pulse goes from HIGH to LOW.

3. Rise delay time: t_{DLH}
   The delay between the time the input arrives at its −6 V point and the time the output passes −6 V when going from LOW to HIGH.

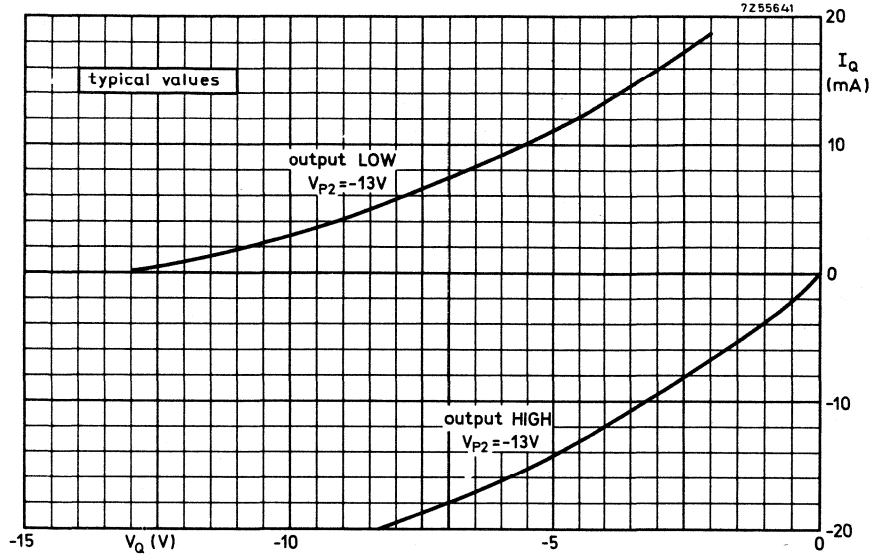
4. Fall delay time: t_{DHL}
   The delay between the time the input arrives at its −6 V point and the time the output passes −6 V when going from HIGH to LOW.

5. Output rise transition time: t_{TLH}
   The time between the 90% and 10% voltage points as the output goes from LOW to HIGH.

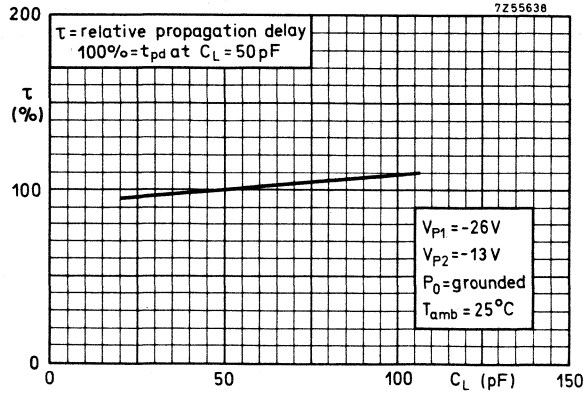
6. Output fall transition time: t_{THL}
   The time between the 10% and 90% voltage points as the output goes from HIGH to LOW.

OUTPUT BUFFER DESCRIPTION

The FDH136 utilizes push-pull output buffers which exhibit the V_Q versus I_Q output curves, for both HIGH and LOW output, shown below.

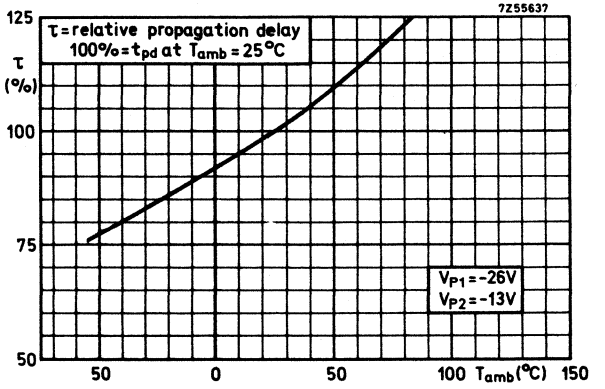


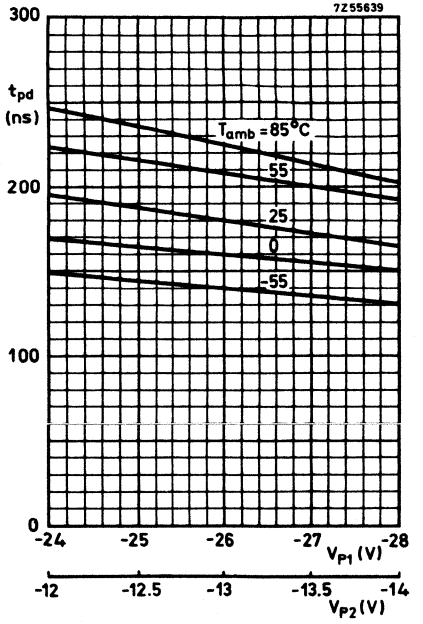
TYPICAL PERFORMANCE at load C_L in parallel with 1 MΩ to P_0.



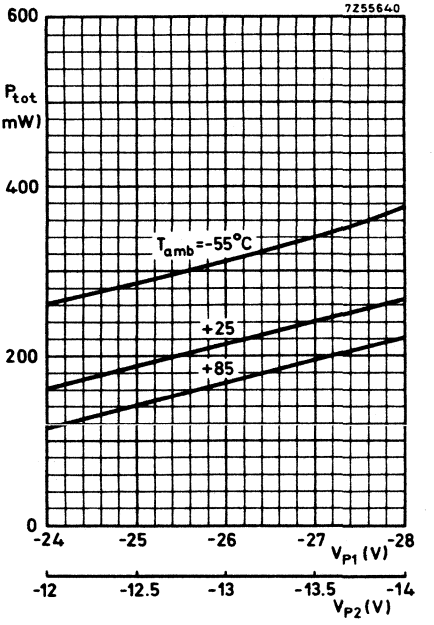
TYPICAL PERFORMANCE (continued)

Test conditions: P_0 = grounded; standard load of 50 pF in parallel with 1 MΩ to P_0.





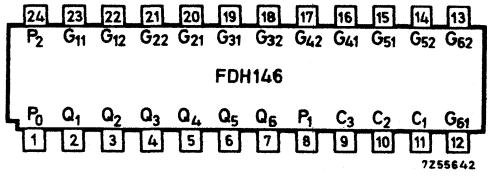
Power dissipation as a function of the supply voltages V_{P1} and V_{P2}



Propagation delay as a function of the supply voltages V_{P1} and V_{P2}

The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

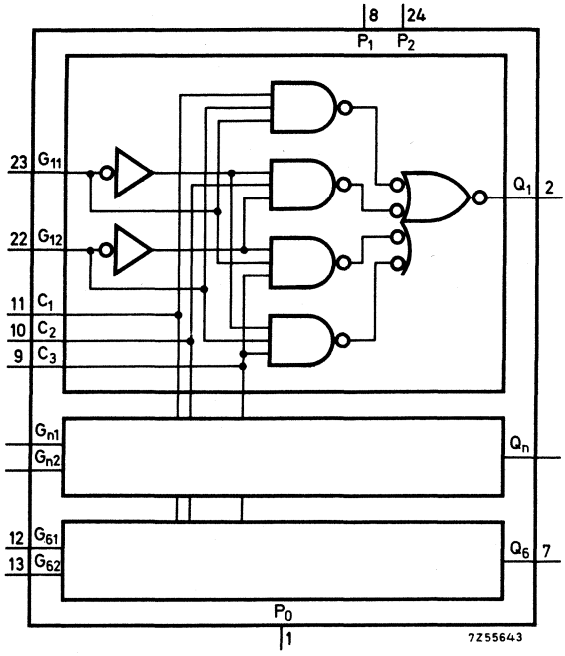
VARIABLE GATE ARRAY



P_0 and metal lid on bottom of the package are connected.

QUICK REFERENCE DATA				
Supply voltage	V_{P1}	−24 to −28		V
Operating ambient temperature	T_{amb}	−55 to +85		°C
Average propagation delay C_L = 50 pF; T_{amb} = 25 °C	t_{pd}	typ.	250	ns
D.C. noise margin	M_H, M_L	>	1.0	V
Average power consumption per function (f = 1 MHz)	P_{av}	typ.	35	mW

PACKAGE OUTLINE 24 lead ceramic dual in-line (See General Section)


8
24
P1
P2
23
G11
22
G12
11
C1
10
C2
9
C3
Q1
2
Gn1
Gn2
Qn
12
G61
13
G62
Q6
7
P0
1
7Z55643

GENERAL DESCRIPTION

The FDH146 consists of six, identical, 2-input gate networks. Three coded control lines determine the function of the six gate networks, so that eight different functions can be selected; the selected function is available six times.
The control inputs have pull-down resistors connected to P_2, so that they assume the LOW state, when left floating.
All inputs are protected against over-voltage caused by static charges.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage on all inputs, outputs and supply terminals with reference to P_0		+0.5 to −30	V
Power dissipation up to T_{amb} = 25 °C	P_{tot}	max. 1	W
Junction temperature	T_j	max. 150	°C
Storage temperature	T_{stg}	−65 to +150	°C
Total current through terminal P_2	$-I_{P2}$	max. 40	mA
Output current per output	$\pm I_Q$	max. 20	mA

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	= 125	°C/W

FUNCTION TABLE

C_3	C_2	C_1	logic equation (positive logic)	logic function	
				positive logic	negative logic
L	L	L	$Q_n = 1$	–	–
L	L	H	$Q_n = \overline{G_{n1} \cdot G_{n2}}$	NAND	NOR
L	H	L	$Q_n = G_{n1} + G_{n2}$	OR	AND
L	H	H	$Q_n = G_{n1} \cdot \overline{G_{n2}} + \overline{G_{n1}} \cdot G_{n2}$	exclusive-OR	comparator
H	L	L	$Q_n = G_{n1} \cdot G_{n2} + \overline{G_{n1}} \cdot \overline{G_{n2}}$	comparator	exclusive-OR
H	L	H	$Q_n = \overline{G_{n1} + G_{n2}}$	NOR	NAND
H	H	L	$Q_n = G_{n1} \cdot G_{n2}$	AND	OR
H	H	H	$Q_n = 0$	–	–

CHARACTERISTICS

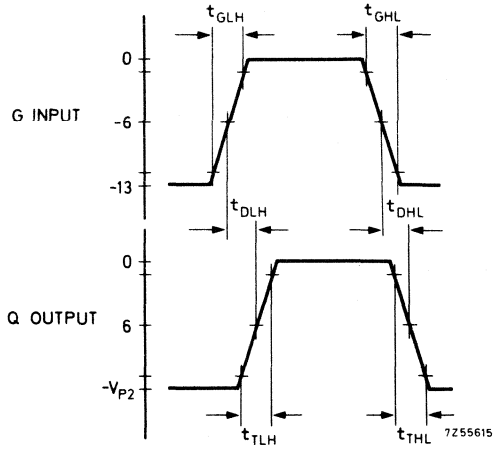
Test conditions: V_{P1} = −24 to −28 V; V_{P2} = −12 to −14 V; T_{amb} = −55 to +85 °C; P_0 = grounded; standard load : 50 pF in parallel with 1 MΩ to P_0.

	Symbol	min.	typ.[1]	max.		Conditions and references
Input logic levels						
HIGH	V_{GH}	−2	0	+0.3	V	
LOW	V_{GL}	−28	–	−9	V	
Output levels						
HIGH	V_{QH}	−1.0	–	0	V	
LOW	V_{QL}	−14	–	−10	V	
Input capacitance						
C_1; C_2	C_{C1}, C_{C2}	–	5.5	7	pF	bias: V_G = 0V; f = 1MHz
C_3	C_{C3}	–	9.5	11	pF	bias: V_G = 0V; f = 1MHz
G_{11} to G_{62}	C_{G11} to C_{G62}	–	3.5	5	pF	bias: V_G = 0V; f = 1MHz
Input leakage current	$-I_{GL}$	–	–	1	µA	V_G=−15V; T_{amb} = 25 °C; all other terminals at V_{P0}
Output resistance						
HIGH	R_{QH}	–	1.0	–	kΩ	V_Q = −1 V
LOW	R_{QL}	–	2.0	–	kΩ	V_Q = −10 V
Supply currents	$-I_{P1}$	–	4.6	7.0	mA	f = 1 MHz; T_{amb} = 25 °C
	$-I_{P2}$	–	6.2	8.5	mA	f = 1 MHz; T_{amb} = 25 °C
Output transition times:						
fall time	t_{THL}	–	150	–	ns	
rise time	t_{TLH}	–	150	–	ns	
Delay times (any input to output)						
fall time	t_{DHL}	–	250	400	ns	
rise time	t_{DLH}	–	250	400	ns	
Control input sink current: C_1, C_2	$-I_{C1}$; $-I_{C2}$	–	32	–	µA	V_G = −2 V
C_3	$-I_{C3}$	–	64	–	µA	V_G = −2 V

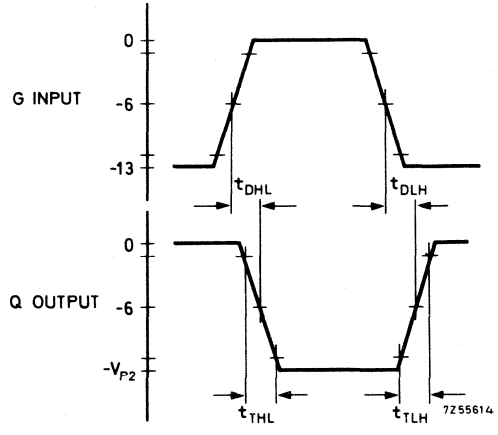
[1]) All typ. values are measured at: T_{amb} = 25 °C and V_{P1} = −26 V, V_{P2} = −13 V.

CHARACTERISTICS (continued)

TIMING DIAGRAMS



non-inverting function



inverting function

Measurements performed under the following conditions:

V_{P1} = −24 to −28 V; V_{P2} = −12 to −14 V; $t_{GLH} = t_{GHL}$ = 150 ns.

Note: The indicated points on the vertical axis are specified in the glossary of terms.

CHARACTERISTICS (continued)

GLOSSARY OF TERMS

1. Input pulse rise time: t_{GLH}
   The time between the 90 % and 10 % voltage points as the input pulse goes from LOW to HIGH.

2. Input pulse fall time: t_{GHL}
   The time between the 10 % and 90 % voltage points as the input pulse goes from HIGH to LOW.

3. Rise delay time: t_{DLH}
   The delay between the time the input arrives at its −6 V point and the time the output passes −6 V when going from LOW to HIGH.

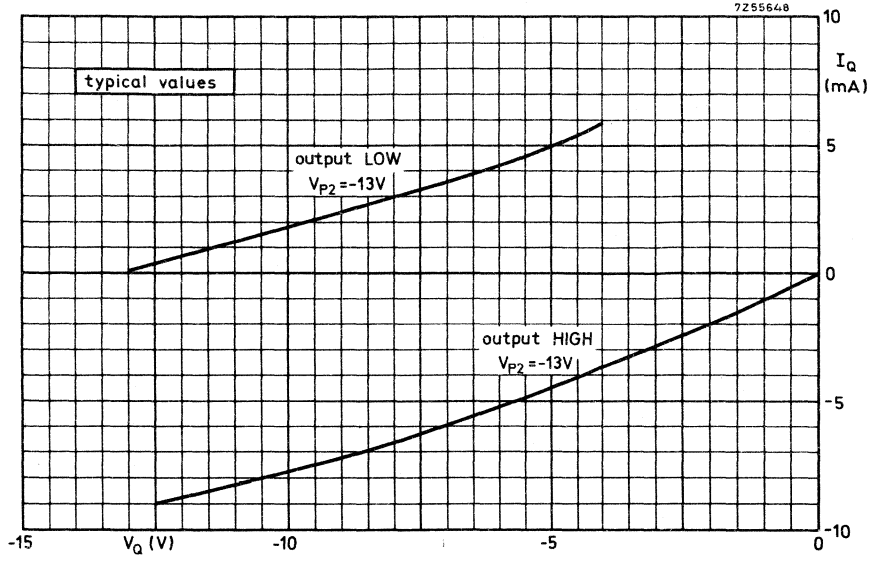
4. Fall delay time: t_{DHL}
   The delay between the time the input arrives at its −6 V point and the time the output passes −6 V when going from HIGH to LOW.

5. Output rise transition time: t_{TLH}
   The time between the 90 % and 10 % voltage points as the output goes from LOW to HIGH.

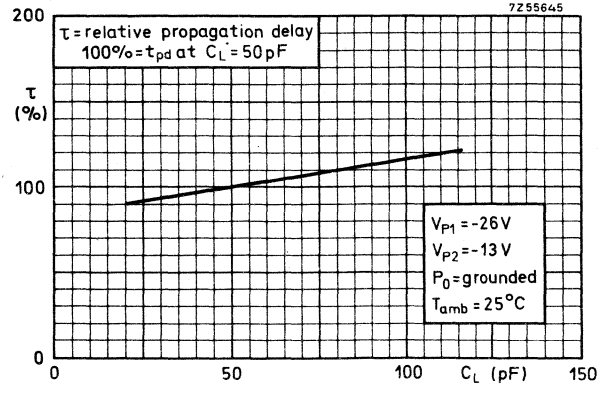
6. Output fall transition time: t_{THL}
   The time between the 10 % and 90 % voltage points as the output goes from HIGH to LOW.

OUTPUT BUFFER DESCRIPTION

The FDH146 utilizes push-pull output buffers which exhibit the V_Q versus I_Q output curves, for both HIGH and LOW output, shown below.

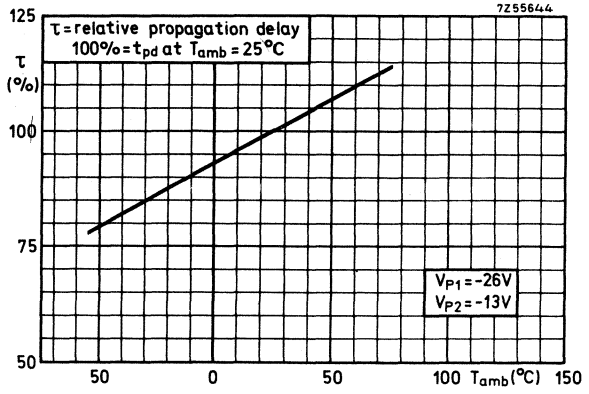


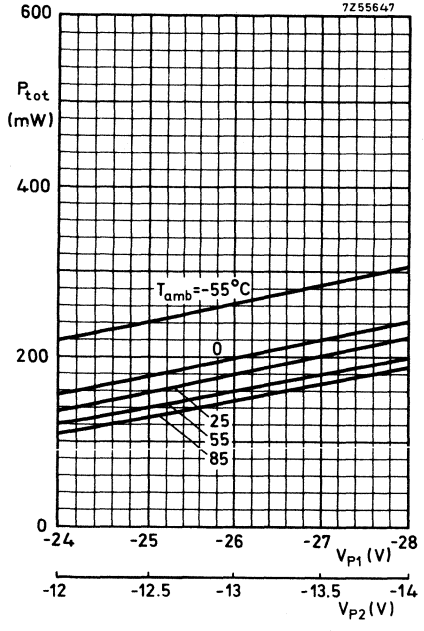
TYPICAL PERFORMANCE at load: C_L in parallel with 1 MΩ to P_0



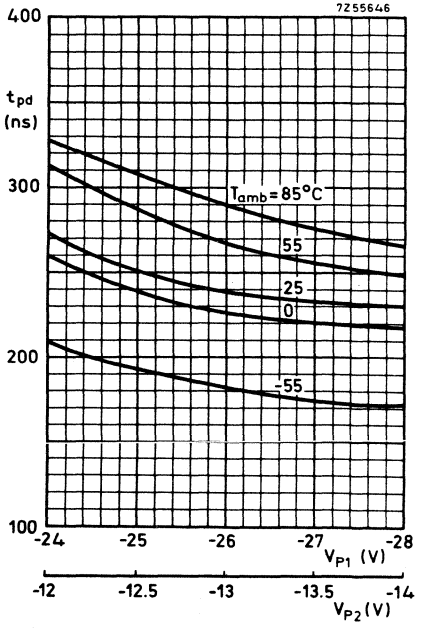
TYPICAL PERFORMANCE (continued)

Test conditions: P_0 = grounded; standard load: 50 pF in parallel with 1 MΩ to P_0.





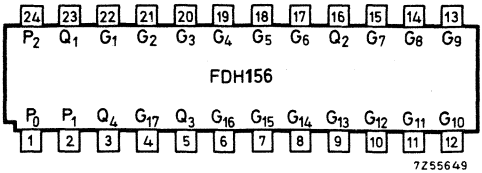
Power dissipation as a function of the supply voltages V_{P1} and V_{P2}



Propagation delay as a function of the supply voltages V_{P1} and V_{P2}

The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

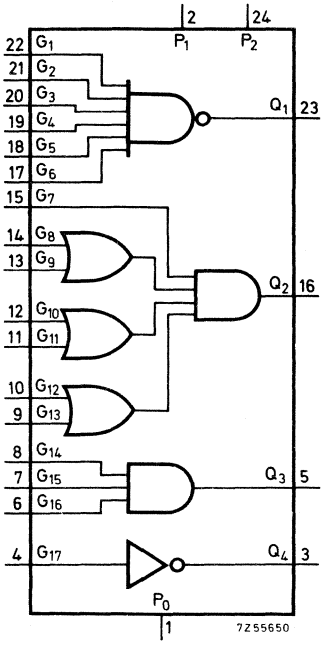
FIXED LOGIC ARRAY



P_0 and metal lid on bottom of the package connected

QUICK REFERENCE DATA				
Supply voltage	V_{P1}	−24 to −28		V
Operating ambient temperature	T_{amb}	−55 to +85		°C
Average propagation delay C_L = 50 pF	t_{pd}	typ.	150	ns
D.C. noise margin	M_H, M_L	>	1.0	V
Power dissipation f = 1 MHz; C_L = 50 pF	P_{tot}	typ.	160	mW

PACKAGE OUTLINE 24 lead ceramic dual in-line (See General Section)


2
24
22 G1
21 G2
20 G3
19 G4
18 G5
17 G6
15 G7
14 G8
13 G9
12 G10
11 G11
10 G12
9 G13
8 G14
7 G15
6 G16
4 G17
P1
P2
Q1 23
Q2 16
Q3 5
Q4 3
P0
1
7Z55650

GENERAL DESCRIPTION

The FDH156 contains all the logic functions shown in the diagram and described in the logic functions below. It is intended to perform logic functions in all MOS digital systems. The output voltage swing is determined by the output buffer supply voltage (V_{P2}).
All inputs are protected against over-voltage caused by static charges.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage on all inputs, outputs and supply terminals with reference to P_0			+0.5 to −30	V
Power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Junction temperature	T_j	max.	150	°C
Storage temperature	T_{stg}		−65 to +150	°C
Total current through terminal P_2	$-I_{P2}$	max.	40	mA
Output current (per output)	$\pm I_Q$	max.	20	mA

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$	=	125	°C/W

LOGIC FUNCTIONS

Positive logic

$Q_1 = \overline{G_1 \cdot G_2 \cdot G_3 \cdot G_4 \cdot G_5 \cdot G_6}$

$Q_2 = G_7 \cdot (G_8 + G_9) \cdot (G_{10} + G_{11}) \cdot (G_{12} + G_{13})$

$Q_3 = G_{14} \cdot G_{15} \cdot G_{16}$

$Q_4 = \overline{G_{17}}$

Negative logic

$Q_1 = \overline{G_1 + G_2 + G_3 + G_4 + G_5 + G_6}$

$Q_2 = G_7 + (G_8 \cdot G_9) + (G_{10} \cdot G_{11}) + (G_{12} \cdot G_{13})$

$Q_3 = G_{14} + G_{15} + G_{16}$

$Q_4 = \overline{G_{17}}$

CHARACTERISTICS

Test conditions: V_{P1} = −24 to −28 V; V_{P2} = −12 to −14 V (see note 1); T_{amb} = −55 to +85 °C; P_0 = grounded; standard load: 50 pF in parallel with 1 MΩ to P_0.

	Symbol	min.	typ.[1])	max.		Conditions and references
Input logic levels						
HIGH	V_{GH}	−2	0	+0.3	V	
LOW	V_{GL}	−28	–	−9	V	
Output levels						
HIGH	V_{QH}	−1.0	–	0	V	
LOW	V_{QL}	−14	–	−10	V	
Input capacitance	C_G	–	5	7	pF	bias: V_G=0; f = 1 MHz
Input leakage current	$-I_{GL}$	–	–	1	μA	V_G=−15V; T_{amb}=25°C all other terminals at V_{P0}
Output resistance						
HIGH	R_{QH}	–	1	–	kΩ	V_Q = −1 V
LOW	R_{QL}	–	2	–	kΩ	V_Q = −10 V
Supply currents	$-I_{P1}$	–	4.6	6.5	mA	f = 1 MHz; T_{amb} = 25°C see note 2
	$-I_{P2}$	–	2.3	3.0	mA	
Output transition times:						
fall time	t_{THL}	–	150	–	ns	
rise time	t_{TLH}	–	150	–	ns	
Delay times (fall and rise times)						
G → Q_1	t_{DHL}, t_{DLH}	–	175	300	ns	see note 3
G → Q_2; Q_3	t_{DHL}, t_{DLH}	–	150	250	ns	
G → Q_4	t_{DHL}, t_{DLH}	–	125	250	ns	

Note 1: V_{P2} is independent of circuit operation and is used for output LOW only.

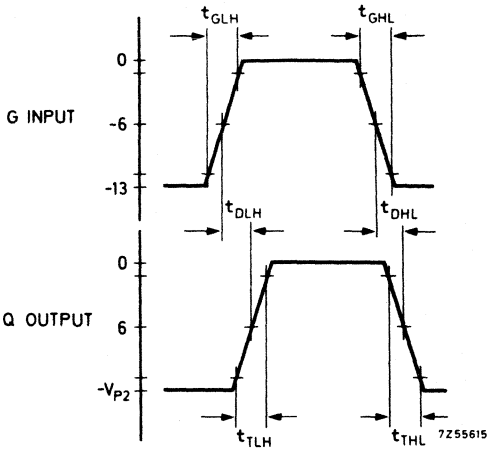
Note 2: Output buffer supply current is almost entirely dependent on the external load.
The value shown is for a load: 50 pF in parallel with 1 MΩ to P_0.

Note 3: Delays are measured at −6 V levels of input and output signals.
(see also timing diagram on page 5)

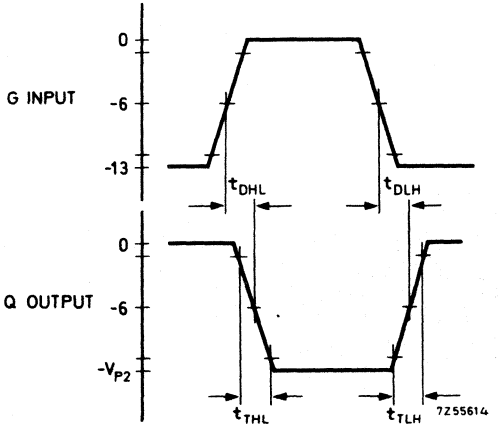
[1]) All typ. values are measured at: T_{amb} = 25 °C ; V_{P1} = −26 V; V_{P2} = −13 V.

CHARACTERISTICS (continued)

TIMING DIAGRAMS



non-inverting function



inverting function

Measurements performed under the following conditions:

$V_{P1} = -24$ to -28 V; $V_{P2} = -12$ to -14 V; $t_{GLH} = t_{GHL} = 150$ ns.

Note: The indicated points on the vertical axis are specified in the glossary of terms.

CHARACTERISTICS (continued)

GLOSSARY OF TERMS

1. Input signal rise time: t_{GLH}
   The time between the 90 % and 10 % voltage points as the input pulse goes from LOW to HIGH.

2. Input signal fall time: t_{GHL}
   The time between the 10 % and 90 % voltage points as the input pulse goes from HIGH to LOW.

3. Rise delay time: t_{DLH}
   The delay between the time the input arrives at −6 V point and the time the output passes −6 V when going from LOW to HIGH.

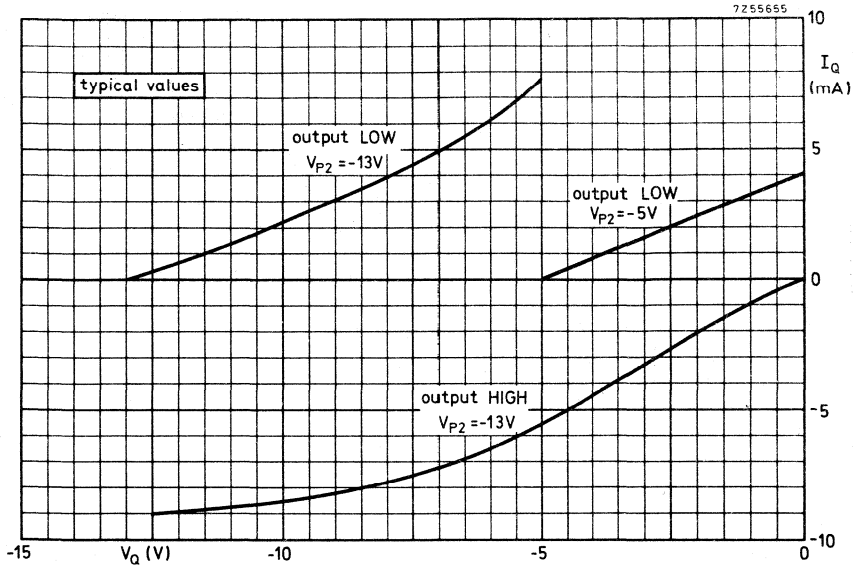
4. Fall delay time: t_{DHL}
   The delay between the time the input arrives at −6 V point and the time the output passes −6 V when going from HIGH to LOW.

5. Output rise transition time: t_{TLH}
   The time between the 90 % and 10 % voltage points as the output goes from LOW to HIGH.

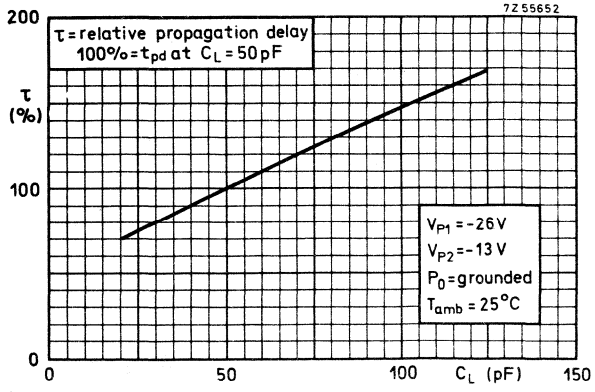
6. Output fall transition time: t_{THL}
   The time between the 10 % and 90 % voltage points as the output goes from HIGH to LOW.

OUTPUT BUFFER DESCRIPTION

The FDH156 utilizes push-pull output buffers which exhibit the V_Q versus I_Q output curves, for both HIGH and LOW output, shown below.

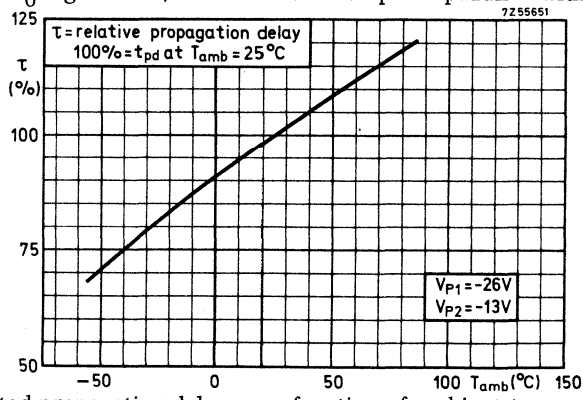


TYPICAL PERFORMANCE at load: C_L in parallel with 1 MΩ to P_0.

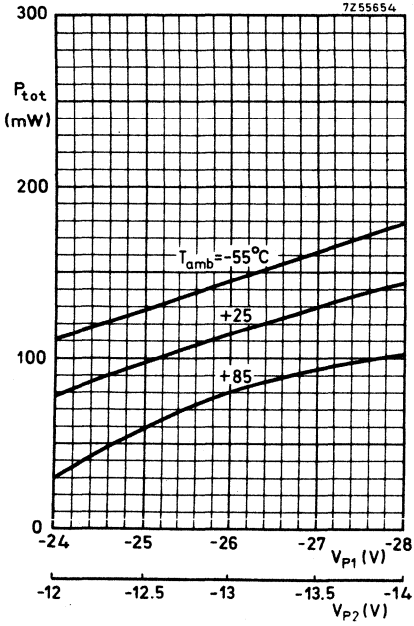


TYPICAL PERFORMANCE (continued)

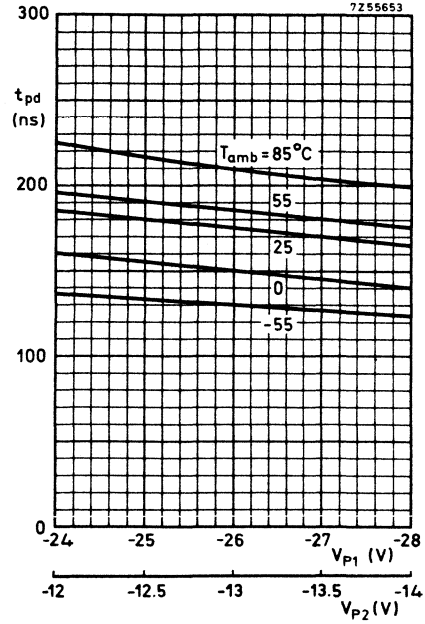
Test conditions: P_0 = grounded; standard load: 50 pF in parallel with 1 MΩ to P_0.



Rated propagation delay as a function of ambient temperature.



Power dissipation as a function of the supply voltages V_{P1} and V_{P2}

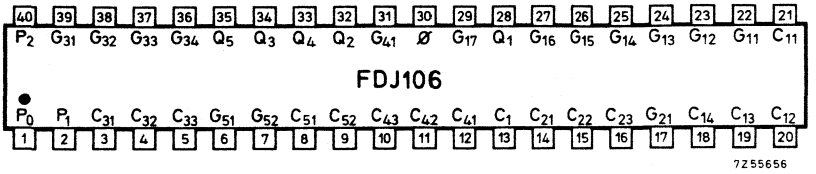


Propagation delay of Q_2 (slowest output) as a function of the supply voltages V_{P1} and V_{P2}.

Note: output buffer power dissipation not included, since it is entirely dependent of loading conditions

The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

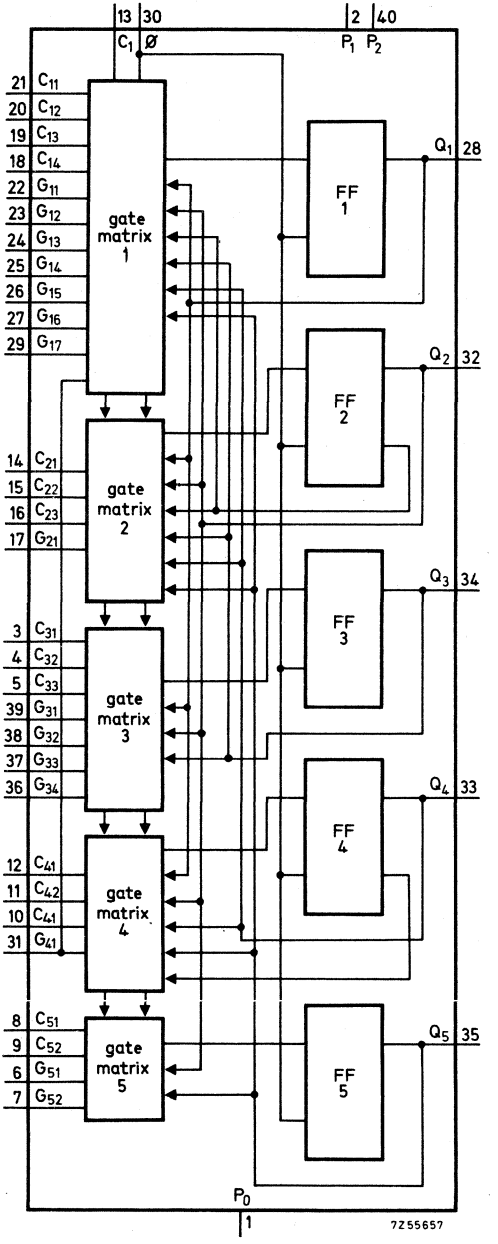
REGISTER ARRAY



P_0 and metal lid on top of the package are connected.

QUICK REFERENCE DATA				
Supply voltage	V_{P1}		−24 to −28	V
Operating ambient temperature	T_{amb}		−55 to +85	°C
Cycle time		typ.	400	ns
Propagation delay time at C_L = 50 pF	t_{pd}	typ.	150	ns
D.C. noise margin	M_H, M_L	>	1.0	V
Power dissipation $f\phi$ = 1 MHz; C_L = 50 pF	$P_{tot.}$	typ.	180	mW

PACKAGE OUTLINE : 40 lead ceramic dual in-line (See General Section)


13 30
C1 Ø
2 40
P1 P2
21 C11
20 C12
19 C13
18 C14
22 G11
23 G12
24 G13
25 G14
26 G15
27 G16
29 G17
gate matrix 1
FF 1
Q1 28
14 C21
15 C22
16 C23
17 G21
gate matrix 2
FF 2
Q2 32
3 C31
4 C32
5 C33
39 G31
38 G32
37 G33
36 G34
gate matrix 3
FF 3
Q3 34
12 C41
11 C42
10 C41
31 G41
gate matrix 4
FF 4
Q4 33
8 C51
9 C52
6 G51
7 G52
gate matrix 5
FF 5
Q5 35
P0
1
7Z55657

GENERAL DESCRIPTION

The FDJ106 is an array of 5 flip-flops, designed to act as a synchronous bit slice of a CPU.
Each of the 5 D-type flip-flops has at least one external input and output, as well as individually controlled transfer and input SELECT logic.
The input gating matrix can therefore enable transfers from external inputs or from other registers in the same array.
The register array contains one bit of each of the five main registers in most computers:

FF1 - accumulator
FF2 - memory data register
FF3 - multiplier/quotient register
FF4 - program counter
FF5 - instruction register

All inputs are protected against over-voltage caused by static charge.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage on all inputs, outputs and supply terminals with reference to P_0		+0.5	to	−30	V
Power dissipation up to T_{amb} = 25 °C	$P_{tot.}$	max.		1	W
Junction temperature	T_j	max.		150	°C
Storage temperature	T_{stg}	−65	to	+150	°C
Total current through terminal P_2	$-I_{P2}$	max.		40	mA
Current per output	$\pm I_Q$	max.		20	mA

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$	=	125	°C/W

LOGIC FUNCTION

REGISTER INPUT SELECTION TABLE

The FDJ106 outputs will conform to the following input transfer function table. With the given set of control inputs, including C_1, which is common to all gate matrices, each flip-flop will have at its D-input the signal shown in the table below.
With the control inputs established, the output of each register will assume the state of its input after the positive going edge of ϕ.

control input (for any gate matrix)				Flip-flop inputs									
				C_1 : HIGH					C_1 : LOW				
C_{n4}	C_{n3}	C_{n2}	C_{n1}	FF1	FF2	FF3	FF4	FF5	FF1	FF2	FF3	FF4	FF5
L	L	L	L	H					G_{41}				
L	L	L	H	G_{17}					G_{17}				
L	L	H	L	G_{16}					G_{16}				
L	L	H	H	G_{15}					G_{15}				
L	H	L	L	G_{14}					G_{14}				
L	H	L	H	G_{13}					G_{13}				
L	H	H	L	G_{12}					G_{12}				
L	H	H	H	G_{11}					G_{11}				
H	L	L	L	H	H	G_{34}	H		Q_1	$\overline{Q_2}$	G_{34}	$\overline{Q_4}$	
H	L	L	H	H	H	G_{33}	H		Q_1	H	G_{33}	H	
H	L	H	L	Q_5	Q_5	G_{32}	G_{41}		Q_1	G_{21}	G_{32}	L	
H	L	H	H	Q_4	Q_{21}	G_{31}	H		Q_1	Q_2	G_{31}	Q_4	
H	H	L	L	$\overline{Q_2}$	Q_4	H	Q_1	G_{52}	Q_1	Q_2	Q_3	Q_4	G_{52}
H	H	L	H	Q_2	Q_1	Q_2	Q_2	G_{51}	Q_1	Q_2	Q_3	Q_4	G_{51}
H	H	H	L	Q_3	Q_3	Q_1	Q_5	Q_2	Q_1	Q_2	Q_3	Q_4	Q_5
H	H	H	H	Q_1	Q_2	Q_3	Q_4	Q_5	Q_1	Q_2	Q_3	Q_4	Q_5

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

CHARACTERISTICS

Test conditions: V_{P1} = −24 to −28 V; V_{P2} = −12 to −14 V; T_{amb} = −55 to +85 °C; P_0 = grounded; standard load: 50 pF in parallel with 1 MΩ to P_0.

DRIVE REQUIREMENTS	Symbol	min.	typ.[1])	max.		Conditions and references
Data and control input logic levels (except C_1)						
HIGH	V_{GH}, V_{CH}	−2	–	+0.3	V	
LOW	V_{GL}, V_{CL}	−28	–	−9	V	
C_1 input levels						
HIGH	V_{C1H}	−2	–	0.3	V	
LOW	V_{C1L}	−28	–	−24	V	
Clock pulse width	$t_{\phi L}$	0.25	–	1.0	µs	see timing diagram on page 7
Clock pulse transition times	$t_{\phi LH}$, $t_{\phi HL}$	–	–	0.1	µs	see timing diagram on page 7
Clock pulse voltage levels: HIGH	$V_{\phi H}$	−2	–	+0.3	V	
LOW	$V_{\phi L}$	−28	−26	−24	V	

[1]) All typical values are measured at: V_{P1} = −26 V; V_{P2} = −13 V; T_{amb} = 25 °C.

CHARACTERISTICS (continued)

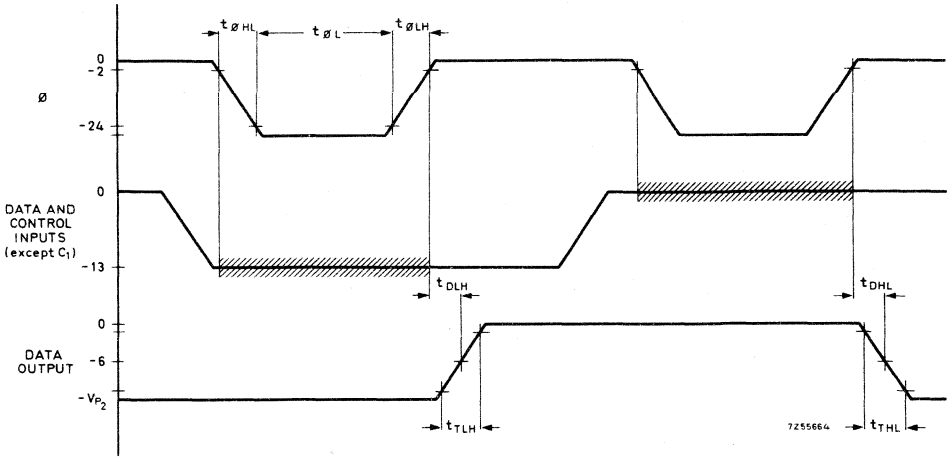
Test conditions: V_{P1} = −24 to −28 V; V_{P2} = −12 to −14 V; T_{amb} = −55 to +85 °C; P_0 = grounded; standard load: 50 pF in parallel with 1 MΩ to P_0.

	Symbol	min.	typ.[1])	max.		Conditions and references
Output logic levels						
HIGH	V_{QH}	−1.0	–	0	V	
LOW	V_{QL}	−14	–	−10	V	
Input capacitance data and control (except C_1)	C_G, C_C	–	4	7.5	pF	bias: $V_G = V_C$ = 0 V; f = 1 MHz
C_1	C_{C1}	–	7	10	pF	bias: V_{C1} = 0 V; f = 1 MHz
clock input	C_ϕ	–	20	25	pF	bias: V_ϕ = 0 V; f = 1 MHz
Input leakage current data and control (except C_1)	$-I_{GL}, -I_{CL}$	–	–	1	µA	bias: $V_G = V_C$ = −15 V; T_{amb} = 25 °C; all other terminals at V_{P0}
C_1	$-I_{C1L}$	–	–	100	µA	bias: V_{C1} = −28 V; T_{amb} = 25 °C; all other terminals at V_{P0}
clock input	$-I_{\phi L}$	–	–	100	µA	bias: V_ϕ = −28 V; T_{amb} = 25 °C; all other terminals at V_{P0}
Output resistance						
HIGH	R_{QH}	–	1.0	–	kΩ	V_Q = −1 V
LOW	R_{QL}	–	1.0	–	kΩ	V_Q = −10 V
Supply currents	$-I_{P1}$	–	6.0	10.0	mA	f = 1 MHz; T_{amb} = 25 °C
	$-I_{P2}$	–	1.6	2.5	mA	f = 1 MHz; T_{amb} = 25 °C
Output transition times: fall time	t_{THL}	–	150	–	ns	
rise time	t_{TLH}	–	150	–	ns	
Delay times:						
fall time	t_{DHL}	–	150	300	ns	
rise time	t_{DLH}	–	150	300	ns	

[1]) All typical values are measured at: V_{P1} = −26 V; V_{P2} = −13 V; T_{amb} = 25 °C.

CHARACTERISTICS (continued)

TIMING DIAGRAMS



Note:
The indicated points on the vertical axis are specified in the glossary of terms.

Timing diagram notes:

1. Data and control inputs must remain valid for the shaded interval to ensure proper entry.
2. C_1 may be switched in the same manner as all other inputs, providing it completes its switching transition before input G_{41} becomes LOW, for any given clock pulse.

CHARACTERISTICS (continued)

GLOSSARY OF TERMS

1. Clock pulse width: $t_{\phi L}$
   The time for which the clock pulse is LOW; $V_{\phi} \leq -24$ V.

2. Clock pulse rise time: $t_{\phi LH}$
   The time between the −24 V and −2 V voltage points as the clock pulse goes from LOW to HIGH.

3. Clock pulse fall time: $t_{\phi HL}$
   The time between the −2 V and −24 V voltage points as the clock pulse goes from HIGH to LOW.

4. Output rise transition time: t_{TLH}
   The time between the 90% and 10% voltage points as the output goes from LOW to HIGH.

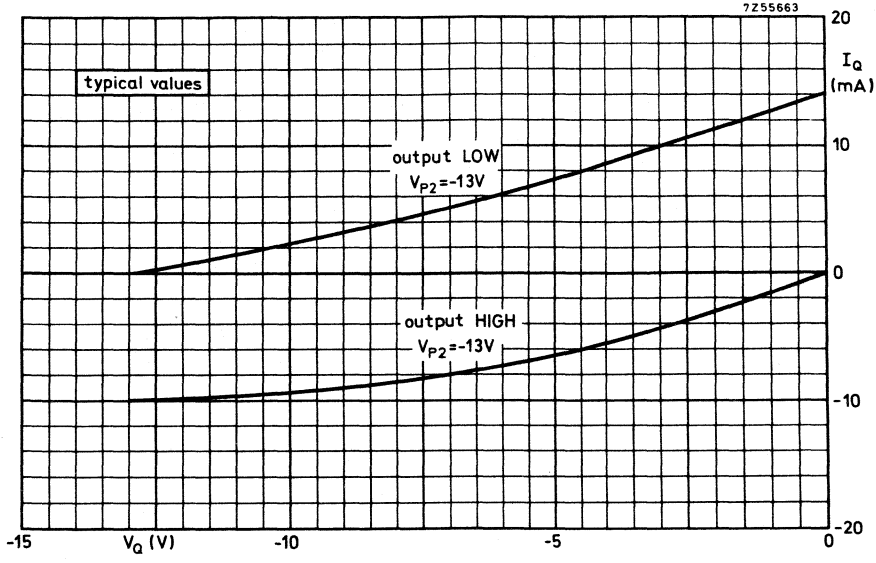
5. Output fall transition time: t_{THL}
   The time between the 10% and 90% voltage points as the output goes from HIGH to LOW.

6. Fall delay time: t_{DHL}
   The delay between the time the positive going edge of the clock pulse arrives at −2 V and the output −6 V voltage point as the output goes from HIGH to LOW.

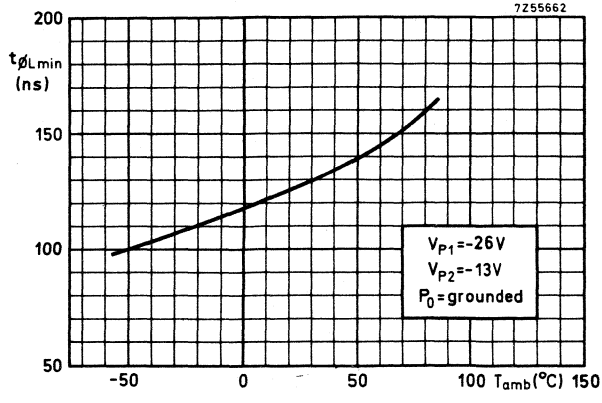
7. Rise delay time: t_{DLH}
   The delay between the time the positive going edge of the clock pulse arrives at −2 V and the output −6 V voltage point as the output goes from LOW to HIGH.

OUTPUT BUFFER DESCRIPTION

The FDJ106 utilizes push-pull output buffers which exhibit the V_Q versus I_Q output curves, for both HIGH and LOW output, shown below.

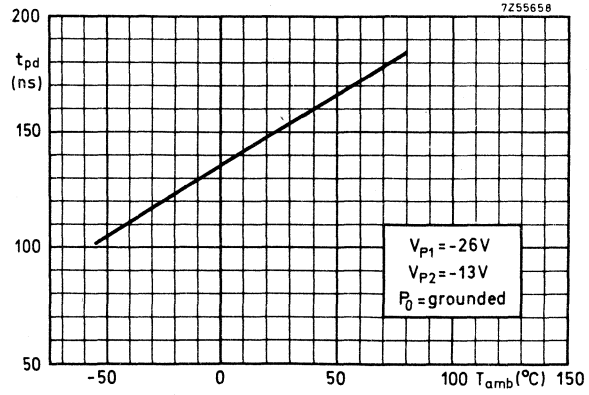


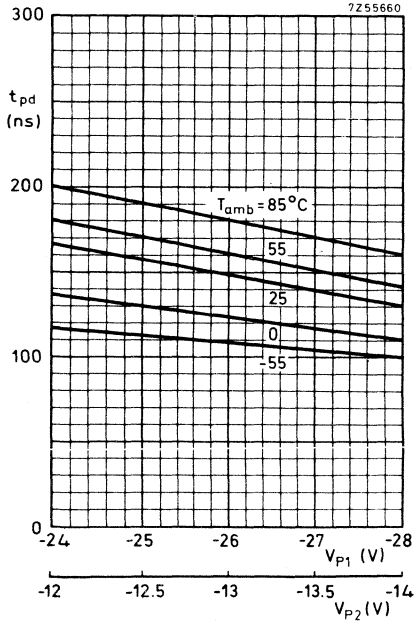
TYPICAL PERFORMANCE



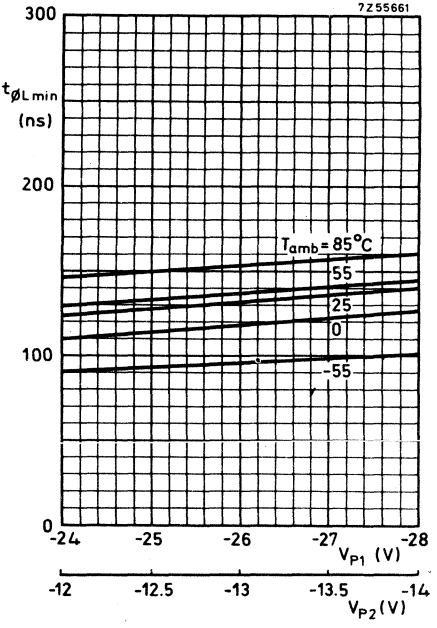
TYPICAL PERFORMANCE (continued)

Test conditions: P_0 = grounded; standard load: 50 pF in parallel with 1 MΩ to P_0.





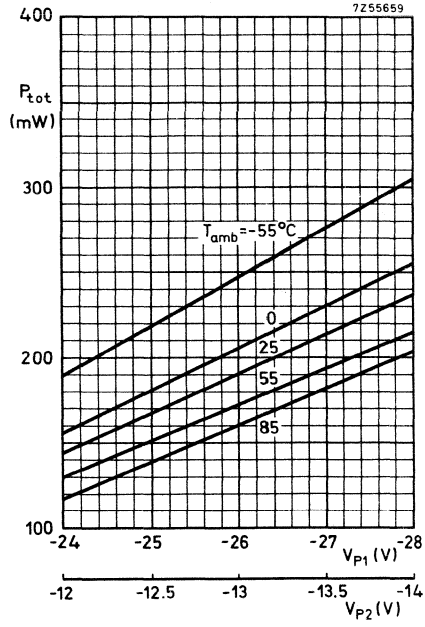
Propagation delay as a function of the supply voltages V_{P1} and V_{P2}



Minimum clock pulse width as a function of the supply voltages V_{P1} and V_{P2}

TYPICAL PERFORMANCE (continued)

Test conditions: P_0 = grounded; standard load: 50 pF in parallel with 1 MΩ to P_0.

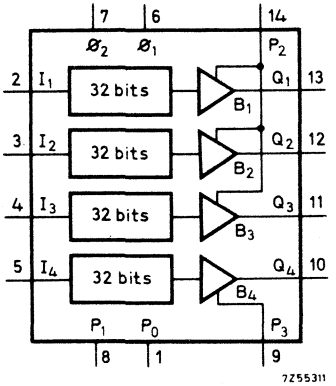


Power dissipation as a function of the supply voltages V_{P1} and V_{P2}

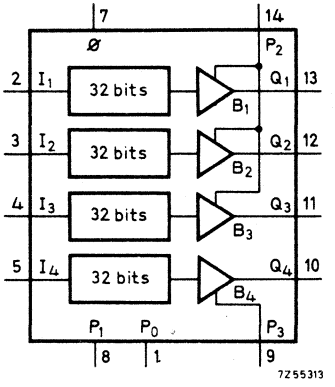
The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

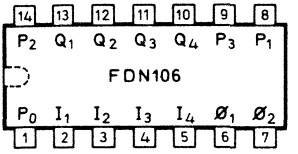
QUADRUPLE 32-BIT DYNAMIC SHIFT REGISTERS

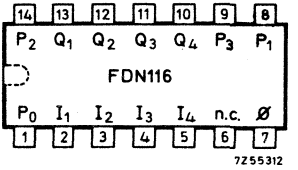
FDN106



FDN116







P_0 and metal package bottom are connected.

QUICK REFERENCE DATA			
Supply voltage	V_{P_1}	−24 to −28	V
D.C. noise margin	M_L; M_H	> 1	V
Clock rate: FDN106	f_ϕ	0.01 to 3	MHz
FDN116	f_ϕ	0.01 to 1	MHz
Power consumption per bit at 1 MHz: FDN106	P_{av}	typ. 0.6	mW
FDN116	P_{av}	typ. 1.0	mW
Power dissipation	P_{tot}	max. 300	mW
Operating ambient temperature	T_{amb}	−55 to +85	°C

PACKAGE OUTLINE: 14 lead metal-ceramic dual in-line (See General Section)

GENERAL DESCRIPTION

The FDN106 and FDN116 packages comprise 4 separate 32-bit shift registers that can be used independently or can be externally connected to make registers up to 128-bits long. Clock and power lines are common to all four registers. The output buffers are bi-directional, low impedance NRZ [1]), that by suitable biasing will directly drive MOS, DTL or TTL loads or, because they have separate supply voltages (V_{P_2}; V_{P_3}), a combination of MOS and bipolar. V_{P_2} and V_{P_3} are output buffer voltages only, and the output LOW signal is independent of the width and amplitude of the clock pulse.

The FDN106 uses a two-phase external clock, has low power dissipation and will operate at high speed.

The FDN116 uses a single phase external clock, and is for applications not calling for the low power economy and high speed of the FDN106.

With the FDN106; FDN116; the FDN126; FDN136 (variable length 1 to 64-bit dynamic shift registers) and the FDN146; FDN156 (256-bit dynamic shift registers) shift registers of any length can be built from off-the shelf parts.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages on all data inputs, clock inputs, outputs and supply terminals with reference to P_0			+0.5 to −30	V
Power disspation up to T_{amb} = 25 °C	P_{tot}	max.	800	mW
Junction temperature	T_j	max.	150	°C
Storage temperature	T_{stg}		−65 to +150	°C
Total current through terminals P_2 and P_3	$-I_{P2}$, $-I_{P3}$	max.	40	mA
Output current (per output)	$\pm I_Q$	max.	20	mA

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$	=	156	°C/W

[1]) Non return to zero.

CHARACTERISTICS at T_{amb} = −55 to +85 °C

	Symbol	Type number	min.	typ.	max.	Conditions and references
Clock rate	f_ϕ	FDN106	0.01	–	3 MHz	
	f_ϕ	FDN116	0.01	–	1 MHz	
Clock pulse width	$t_{\phi 1L}$	FDN106	0.125	–	25 µs	see timing diagram for parameter def.
	$t_{\phi 2L}$	FDN106	0.125	–	25 µs	
	$t_{\phi L}$	FDN116	0.50	–	50 µs	
Clock pulse fall time	$t_{\phi HL}$		–	–	0.10 µs	see note 1, 2
Clock pulse rise time	$t_{\phi LH}$		–	–	0.10 µs	see note 2
Clock delay time	$t_{\phi 1\phi 2}$	FDN106	0	–	25 µs	
Clock delay time	$t_{\phi 2\phi 1}$	FDN106	0	–	25 µs	
Clock pulse space	$t_{\phi H}$	FDN116	0.50	–	50 µs	
Clock pulse voltage level						
HIGH	$V_{\phi H}$		−2	0	+0.3 V	
LOW	$V_{\phi L}$	FDN106	−28	−26	−24 V	
	$V_{\phi L}$	FDN116	−28	−12	−9 V	
Data input logic levels						
HIGH	V_{IH}		−1.5	0	+0.3 V	
LOW	V_{IL}		−28	−12	−9 V	
Data lead time	$t_{\ell I}$	FDN106	10	–	– ns	
	$t_{\ell I}$	FDN116	20	–	– ns	
Data hold time	t_{hI}	FDN116	75	–	– ns	

Note 1

The fall time specified for the FDN116 is to ensure that output data will meet the input hold time requirements of other shift registers, when more shift registers operate in series from a common clock. If a register does not drive other registers the clock pulse fall time may be longer.

Note 2

For FDN106 above f_ϕ = 1.54 MHz $t_{\phi 1Lmin}$ and $t_{\phi 2Lmin}$ determine the maximum value of $t_{\phi HL}$ and $t_{\phi LH}$.

CHARACTERISTICS

Test conditions: V_{P_1} = −24 V to −28 V; V_{P_2} = −12 V to −14 V; T_{amb} = −55 to +85 °C; P_0 = grounded; standard load of 20 kΩ in parallel with 50 pF to P_0

	Symbol	Type number	min.	typ.	max.	Conditions and references
ELECTRICAL DATA						
Output levels						
HIGH	V_{QH}		−0.5	−	0 V	
LOW	V_{QL}		−14	−	−10 V	
Data input capacitance	C_I		−	2	3.5 pF	bias: V_I = 0 V; f = 1 MHz
Clock input capacitance	$C_{\phi 1}$, $C_{\phi 2}$	FDN106	−	38	50 pF	bias: V_ϕ = 0 V; f = 1 MHz
	C_ϕ	FDN116	−	6	8 pF	bias: V_ϕ = 0 V; f = 1 MHz
	$C_{\phi 1}$, $C_{\phi 2}$	FDN106	−	28	37 pF	bias: V_ϕ = −26 V; f = 1 MHz
Leakage currents:						
Data input currents	$-I_{IL}$		−	−	1 μA	V_I = −15 V; all other terminals at V_{P_0}; T_{amb} = 25 °C
Clock input current	$-I_{\phi L}$		−	−	100 μA	V_ϕ = −28 V; all other terminals at V_{P_0}; T_{amb} = 25 °C
Output resistance						
HIGH	R_{QH}		−	220	500 Ω	
LOW	R_{QL}		−	220	500 Ω	V_{P_2} = V_{P_3} = −5 V
Drive capability (see note 1)	V_{QL}		−	−10	−8 V	R_L = 4 kΩ reference to P_0
	V_{QL}		−	−4.7	−4.4 V	V_{P_2} = V_{P_3} = −5 V; R_L = 4 kΩ reference to P_0
Power supply current drain (see note 2)	$-I_{P_2}$, $-I_{P_3}$		−	3.0	3.5 mA	V_{P_2} = V_{P_3} = −13 V; fφ = 1 MHz; T_{amb} = 25 °C
	$-I_{P_1}$	FDN106	−	2.0	4.0 mA	V_{P_1} = −26 V; fφ = 1 MHz; T_{amb} = 25 °C
	$-I_{P_1}$	FDN116	−	5.0	7.0 mA	
Output transition times:						
fall time	t_{THL}		−	100	− ns	
rise time	t_{TLH}		−	100	− ns	
Delay times: fall time	t_{DHL}	FDN106	−	70	− ns	
	t_{DHL}	FDN116	−	300	− ns	
rise time	t_{DLH}	FDN106	−	70	− ns	
	t_{DLH}	FDN116	−	300	− ns	
D.C. noise margin	M_L, M_H		1	−	− V	

CHARACTERISTICS (continued)

Note 1 (see page 4)

The maximum capacitive load that can be driven depends only on the speed desired and the power dissipation allowable. See the output buffer description on page 8 for further information on output drive capability.

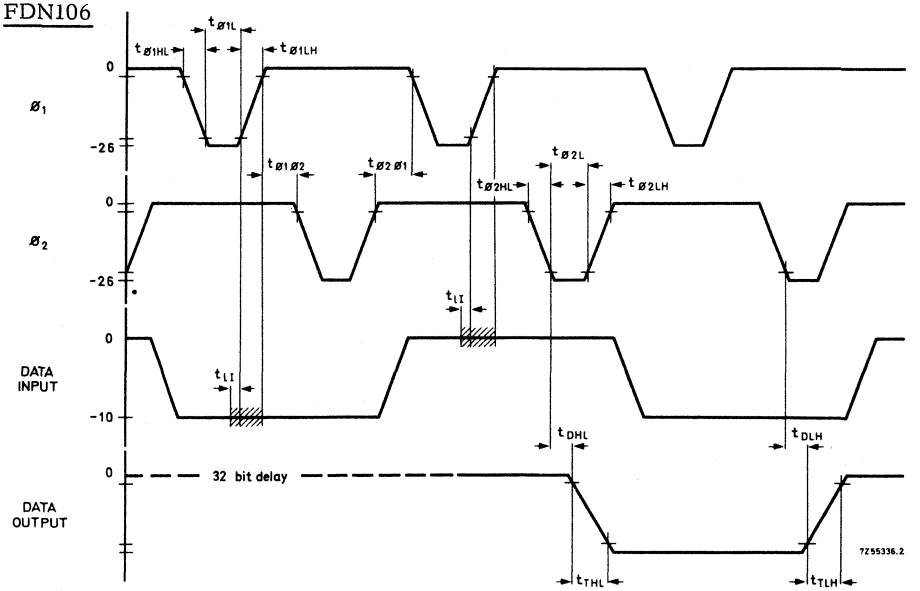
Note 2 (see page 4)

The output buffer power supply currents (I_{P_2}, I_{P_3}) are almost entirely dependent on the external load.

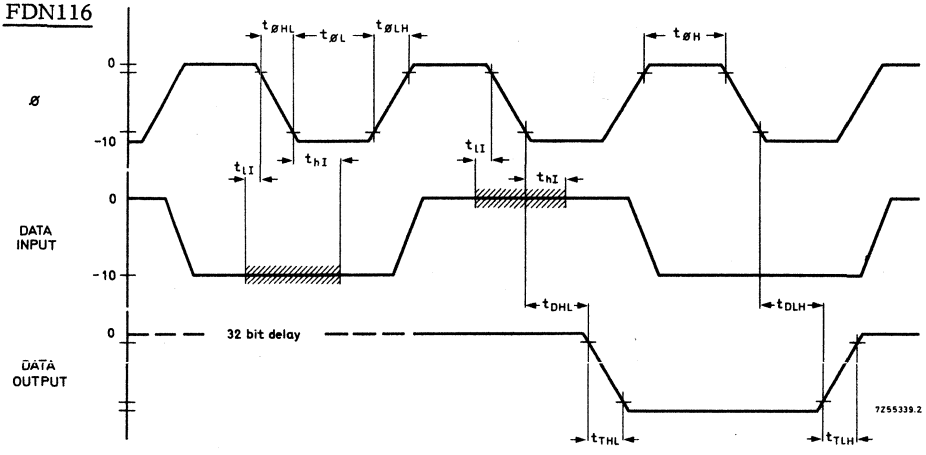
CHARACTERISTICS (continued)

TIMING DIAGRAMS

FDN106



FDN116



Notes

1. The indicated points on the vertical axes are specified in the glossary of terms.
2. Input data must remain valid during the shaded interval to ensure proper entry into the register.

CHARACTERISTICS (continued)

GLOSSARY OF TERMS

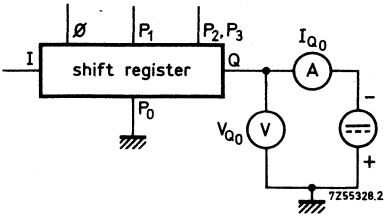
1. Clock pulse width: $t_{\phi L}$
   The time for which the clock pulse is LOW: FDN106; $V_{\phi L} \leq -24$ V
   FDN116; $V_{\phi L} \leq -9$ V
2. Clock pulse fall time: $t_{\phi HL}$
   The time between the 10% and 90% voltage points as the clock pulse goes from HIGH to LOW.
3. Clock pulse rise time: $t_{\phi LH}$
   The time between the 90% and 10% voltage points as the clock pulse goes from LOW to HIGH.
4. Clock delay time: $t_{\phi 1 \phi 2}$, $t_{\phi 2 \phi 1}$ (FDN106)
   The least allowable time between the end of the ϕ_1 (or ϕ_2) clock pulse and the start of the ϕ_2 (or ϕ_1) clock pulse, defined at −2 V.
5. Clock pulse space: $t_{\phi H}$ (FDN116)
   The minimum time between the end of a clock pulse (ϕ) and the start of the next, defined at −2 V.
6. Data lead time: $t_{\ell I}$
   FDN106: The time before the 90% point on the clock pulse ϕ_1 for which the voltage at the data input must be at its specified logic level in order to ensure that the data will be entered in the register.
   FDN116: The time before the 10% point on the clock pulse for which the voltage at the data input must be at its specified logic level in order to ensure that the data will be entered in the register.
7. Data hold time: t_{hI} (FDN116)
   The time after the clock pulse ϕ reaches LOW for which the input data must remain stable to guarantee that it will be entered into the register.
8. Output fall transition time: t_{THL}
   The time between the 10% and 90% voltage points as the output goes from HIGH to LOW.
9. Output rise transition time: t_{TLH}
   The time between the 90% and 10% voltage points as the output goes from LOW to HIGH.
10. Fall delay time: t_{DHL}
    FDN106: The delay between the clock pulse ϕ_2 reaching LOW and the output beginning to change from HIGH to LOW.
    FDN116: The delay between the clock pulse ϕ reaching LOW and the output beginning to change from HIGH to LOW.
11. Rise delay time: t_{DLH}
    FDN106: The delay between the clock pulse ϕ_2 reaching LOW and the output beginning to change from LOW to HIGH.
    FDN116: The delay between the clock pulse ϕ reaching LOW and the output beginning to change from LOW to HIGH.

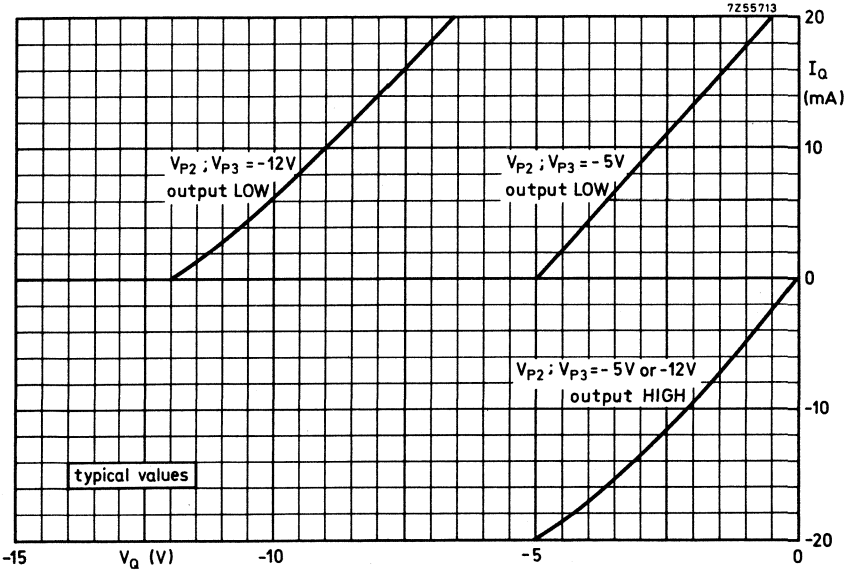
OUTPUT BUFFER DESCRIPTION

1. The curves below are typical output buffer voltage-current characteristics for the FDN106 and FDN116. They show V_Q versus I_Q for the bias V_{P_2} and V_{P_3} at **−5 V and −12 V, for both HIGH and LOW output.**

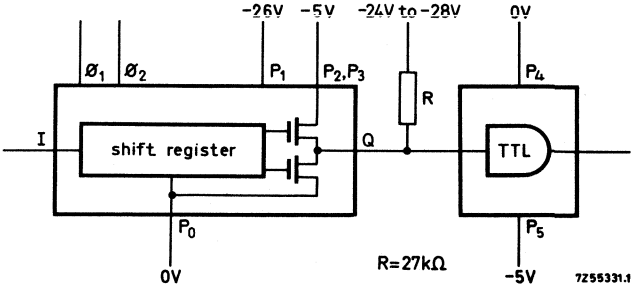
   Note: When operating with high output current levels, the maximum power rating must not be exceeded.

The circuit shown may be used to obtain output curves for other values of V_{P_2} and V_{P_3}.

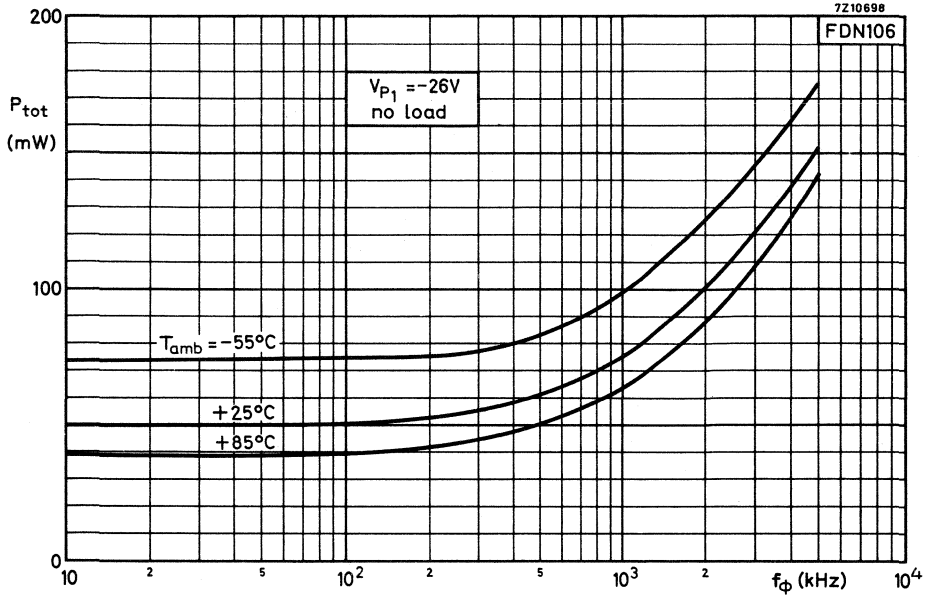


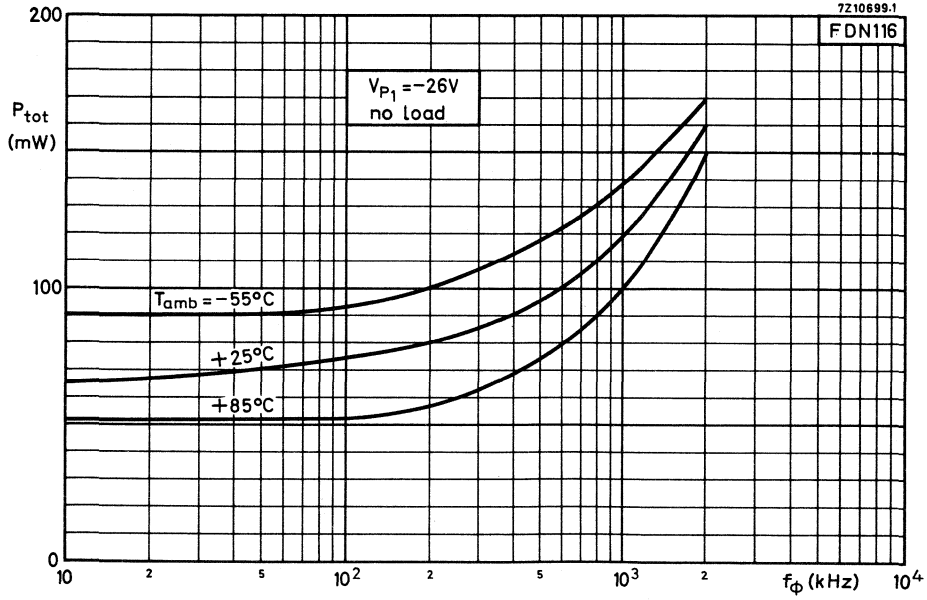


2. The bias arrangement shown is suitable for driving TTL or DTL loads direct.

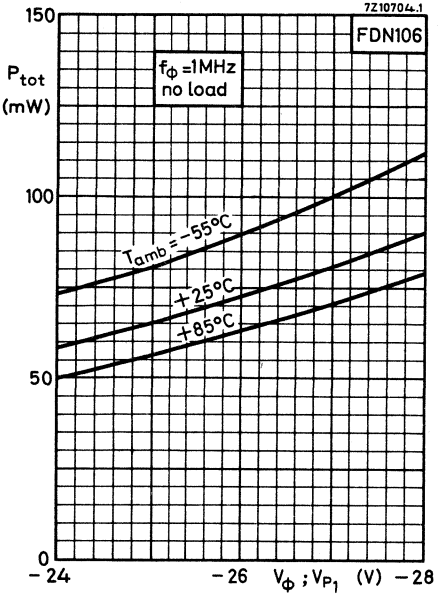


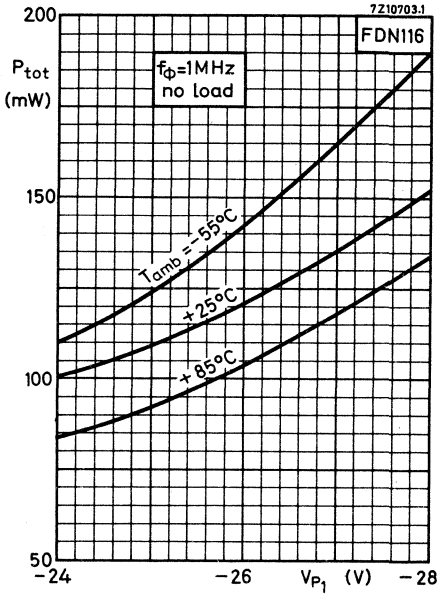
TYPICAL PERFORMANCE

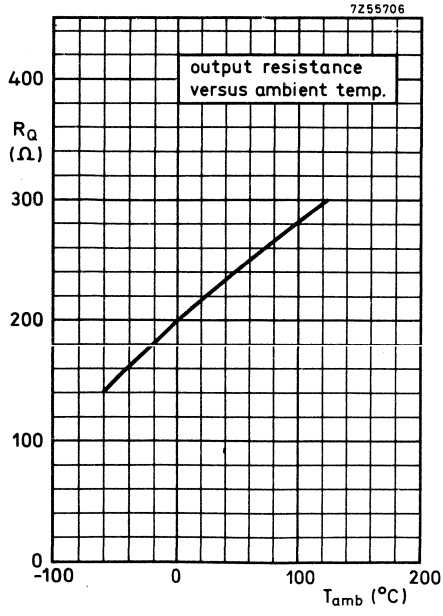


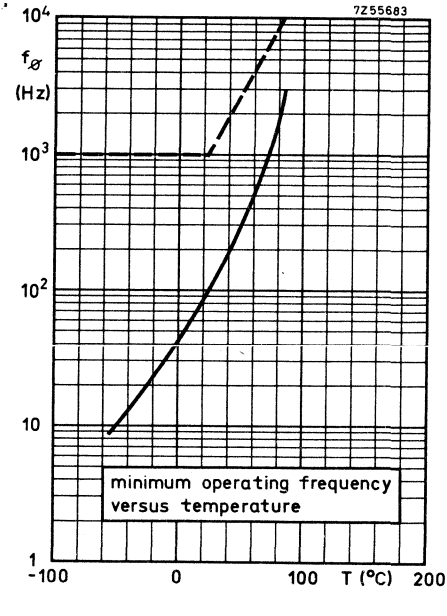


TYPICAL PERFORMANCE (continued)



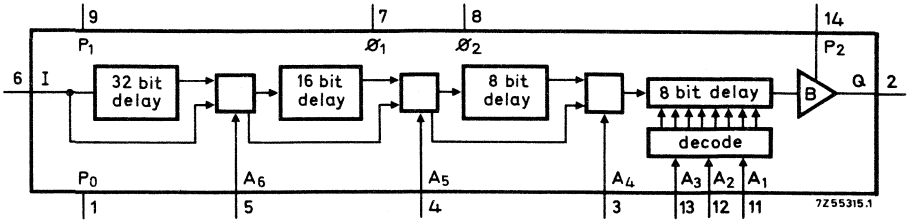


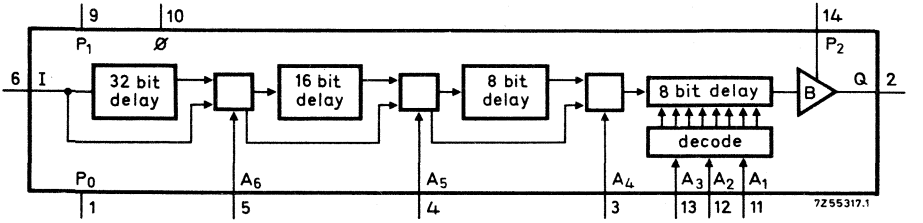


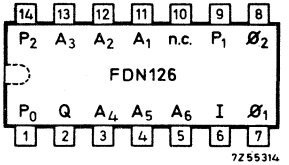


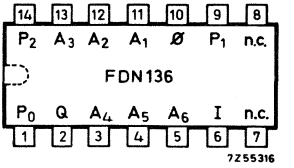
The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

VARIABLE LENGTH 1 TO 64-BIT DYNAMIC SHIFT REGISTERS









P_0 and metal package bottom are connected.

QUICK REFERENCE DATA			
Supply voltage	V_{P_1}	−24 to −28	V
D.C. noise margin	M_L; M_H	> 1	V
Clock rate: FDN126	f_ϕ	0.01 to 3	MHz
FDN136	f_ϕ	0.01 to 1	MHz
Operating ambient temperature	T_{amb}	−55 to +85	°C

PACKAGE OUTLINE : 14 lead metal-ceramic dual in-line (See General Section)

GENERAL DESCRIPTION

The FDN126 and FDN136 are unique in that the bit length of both registers can be set from 1 to 64 bits by appropriate choice of the logic state of 6 control inputs. The same input and output leads are used, the control inputs determine the number of register stages connected between them.

The FDN126 is essentially for high speed operation and needs a 2 phase external clock.

The FDN136 needs only a low level single phase external clock; it is suitable for applications that do not demand speeds in excess of 1 MHz.

Both circuits use a bi-directional low impedance output buffer which, when appropriately biased, is capable of driving MOS or DTL and TTL loads direct.

With the FDN126; FDN136, the FDN106; FDN116 (quadruple 32-bit dynamic shift registers) and FDN146; FDN156 (256 bit dynamic shift registers) shift registers of any length can be built from off-the-shelf parts.

REGISTER LENGTH CONTROL

The length of the register is controlled by applying binary signals to lines A_1 to A_6. The actual length is one more than the binary sum (see table). The length control bits are gated in at ϕ_1. The length of the register is set up approximately 2 µs +2 clock cycles after application of the control signals. (one clock cycle is one ϕ_1 pulse + one ϕ_2 pulse for the FDN126 and one ϕ pulse for the FDN136)

Table (examples)

weight: 32	16	8	4	2	1	
A_6	A_5	A_4	A_3	A_2	A_1	register length
H	H	H	H	H	H	1-bit
H	H	H	H	H	L	2-bits
H	H	H	L	H	L	6-bits
L	H	H	H	H	H	33-bits
L	L	L	L	L	L	64-bits

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages on all data inputs, clock inputs, outputs, control inputs and supply terminals with reference to P_0			+0.5 to −30	V
Power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	800	mW
Junction temperature	T_j	max.	150	°C
Storage temperature	T_{stg}		−65 to +150	°C
Total current through terminal P_2	$-I_{P2}$	max.	20	mA
Output current (per output)	$\pm I_Q$	max.	20	mA

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	156	°C/W

DRIVE REQUIREMENTS

	Symbol	Type number	min.	typ.	max.	Conditions and references
Clock rate	f_ϕ	FDN126	0.01	–	3 MHz	
	f_ϕ	FDN136	0.01	–	1 MHz	
Clock pulse width	$t_{\phi 1L}$	FDN126	0.1	–	1.0 µs	see timing diagram for parameter def.
	$t_{\phi 2L}$	FDN126	0.125	–	1.0 µs	
	$t_{\phi L}$	FDN136	0.50	–	50 µs	
Clock pulse fall time	$t_{\phi HL}$		–	–	0.10 µs	see note 1, 2
Clock pulse rise time	$t_{\phi LH}$		–	–	0.10 µs	see note 2
Clock delay time	$t_{\phi 1\phi 2}$	FDN126	0	–	49 µs	
Clock delay time	$t_{\phi 2\phi 1}$	FDN126	0	–	49 µs	
Clock pulse space	$t_{\phi H}$	FDN136	0.50	–	50 µs	
Clock pulse voltage level						
HIGH	$V_{\phi H}$		−2	0	+0.3 V	
LOW	$V_{\phi L}$	FDN126	−28	−26	−24 V	
	$V_{\phi L}$	FDN136	−28	−12	−9 V	
Data and control input logic level HIGH	V_{IH};V_{AH}		−1.5	0	+0.3 V	
LOW	V_{IL};V_{AL}		−28	−12	−9 V	
Data lead time	$t_{\ell I}$	FDN126	20	–	– ns	
	$t_{\ell I}$	FDN136	75	–	– ns	
Data hold time	t_{hI}	FDN136	75	–	– ns	

Note

The clock pulse fall time specified for the FDN136 is to ensure that output data will meet the input hold time requirements of other shift registers, when more shift registers operate in series from a common clock. If a register does not drive other registers, the clock pulse rise and fall times may be longer.

Note 2

For FDN126 above f_ϕ = 1.6 MHz $t_{\phi 1Lmin}$ and $t_{\phi 2Lmin}$ determine the maximum value of $t_{\phi HL}$ and $t_{\phi LH}$.

CHARACTERISTICS

Test conditions: V_{P_1} = −24 V to −28 V; V_{P_2} = −12 to −14 V; T_{amb} = −55 to +85 °C; P_0 = grounded; standard load of 20 kΩ in parallel with 50 pF to P_0

	Symbol	Type number	min.	typ.	max.	Conditions and references
ELECTRICAL DATA						
Output levels						
HIGH	V_{QH}		−0.5	−	0 V	
LOW	V_{QL}		−14	−	−10 V	
Data input capacitance	C_I		−	2	3.5 pF	bias: V_I = 0 V; f_ϕ = 1 MHz
Clock input capacitance	$C_{\phi 1}$, $C_{\phi 2}$	FDN126	−	22	30 pF	bias: V_ϕ = 0 V; f_ϕ = 1 MHz
	C_ϕ	FDN136	−	6	8 pF	
	$C_{\phi 1}$, $C_{\phi 2}$	FDN126	−	14	20 pF	bias: V_ϕ = −26 V; f_ϕ = 1 MHz
Leakage currents:						
Data input current	$-I_{IL}$		−	−	1 μA	V_I = −15 V; all other terminals at V_{P_0}; T_{amb} = 25 °C
Clock input current	$-I_{\phi L}$	FDN126	−	−	100 μA	V_ϕ = −28 V; all other terminals at V_{P_0}; T_{amb} = 25 °C
	$-I_{\phi L}$	FDN136	−	−	1 μA	V_ϕ = −15 V; all other terminals at V_{P_0}; T_{amb} = 25 °C
Output resistance:						
HIGH	R_{QH}		−	220	500 Ω	
LOW	R_{QL}		−	220	500 Ω	V_{P_2} = −5 V
Drive capability (see note 1)	V_{QL}		−	−10	−8 V	R_L = 4 kΩ reference to P_0
	V_{QL}		−	−4.7	−4.4 V	V_{P_2} = −5 V; R_L = 4 kΩ reference to P_0
Power supply current drain (see note 2)	$-I_{P_2}$		−	0.8	1.0 mA	V_{P_2} = −13 V; f_ϕ = 1 MHz; T_{amb} = 25 °C
	$-I_{P_1}$	FDN126	−	2.5	5.0 mA	V_{P_1} = −26 V; f_ϕ = 1 MHz; T_{amb} = 25 °C
	$-I_{P_1}$	FDN136	−	3.0	6.0 mA	
Output transition times:						
fall time	t_{THL}		−	80	− ns	
rise time	t_{TLH}		−	80	− ns	
Delay times: fall time	t_{DHL}	FDN126	−	70	− ns	
	t_{DHL}	FDN136	−	300	− ns	
rise time	t_{DLH}	FDN126	−	70	− ns	
	t_{DLH}	FDN136	−	300	− ns	
D.C. noise margin	M_L, M_H		1	−	− V	

CHARACTERISTICS (continued)

Note 1 (see page 4)

The maximum capacitive load that can be driven depends only on the speed desired and the power dissipation allowable. See the output buffer description on page 8 for further information on output drive capability.

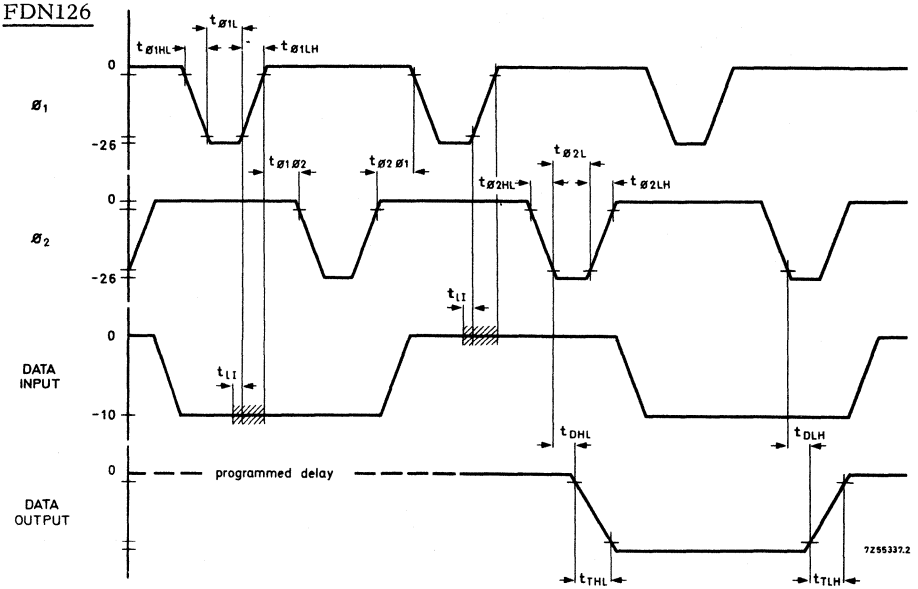
Note 2 (see page 4)

The output buffer power supply current I_{P2} is almost entirely dependent on the external load.

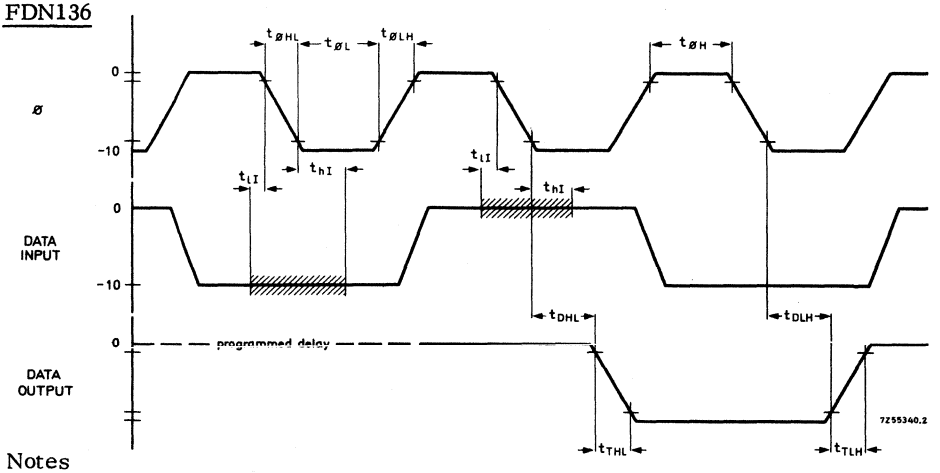
CHARACTERISTICS (continued)

TIMING DIAGRAMS

FDN126



FDN136



Notes

1. The indicated points on the vertical axes are specified in the glossary of terms.
2. During a continuous series of LOW signals the data output may return momentarily to zero once every clock cycle, i. e. when the register output normally changes signal. The data output should be not sampled during this period.
3. Input data must remain valid during the shaded interval to ensure proper entry into the register.

CHARACTERISTICS (continued)

GLOSSARY OF TERMS

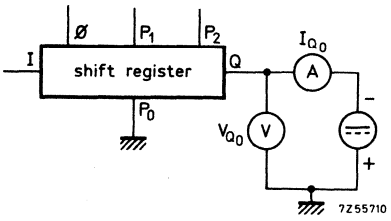
1. Clock pulse width: $t_{\phi L}$
   The time for which the clock pulse is LOW: FDN126; $V_{\phi L} \leq -24$ V
   FDN136; $V_{\phi L} \leq -9$ V
2. Clock pulse fall time: $t_{\phi HL}$
   The time between the 10% and 90% voltage points as the clock pulse goes from HIGH to LOW.
3. Clock pulse rise time: $t_{\phi LH}$
   The time between the 90% and 10% voltage points as the clock pulse goes from LOW to HIGH.
4. Clock delay time: $t_{\phi 1 \phi 2}$; $t_{\phi 2 \phi 1}$ (FDN126)
   The least allowable time between the end of the ϕ_1 (or ϕ_2) clock pulse and the start of the ϕ_2 (or ϕ_1) clock pulse, defined at −2 V.
5. Clock pulse space: $t_{\phi H}$ (FDN136)
   The minimum time between the end of a clock pulse (ϕ) and the start of the next, defined at −2 V.
6. Data lead time: $t_{\ell I}$
   FDN126: The time before the 90% point on the clock pulse ϕ_1 for which the voltage at the data input must be at its specified logic level in order to ensure that the data will be entered in the register.
   FDN136: The time before the 10% point on the clock pulse for which the voltage at the data input must be at its specified logic level in order to ensure that the data will be entered in the register.
7. Data hold time: t_{hI} (FDN136)
   The time after the clock pulse ϕ reaches LOW for which the input data must remain stable to guarantee that it will be entered into the register.
8. Output fall transition time: t_{THL}
   The time between the 10% and 90% voltage points as the output goes from HIGH to LOW.
9. Output rise transition time: t_{TLH}
   The time between the 90% and 10% voltage points as the output goes from LOW to HIGH.
10. Fall delay time: t_{DHL}
    FDN126: The delay between the clock pulse ϕ_2 reaching LOW and the output beginning to change from HIGH to LOW.
    FDN136: The delay between the clock pulse ϕ reaching LOW and the output beginning to change from HIGH to LOW.
11. Rise delay time: t_{DLH}
    FDN126: The delay between the clock pulse ϕ_2 reaching LOW and the output beginning to change from LOW to HIGH.
    FDN136: The delay between the clock pulse ϕ reaching LOW and the output beginning to change from LOW to HIGH.

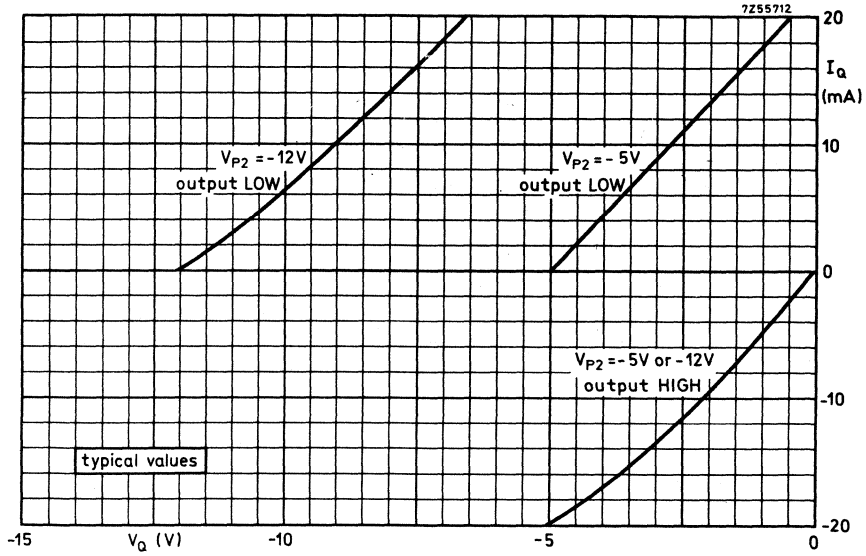
OUTPUT BUFFER DESCRIPTION

1. The curves below are typical output buffer voltage-current characteristics for the FDN126 and FDN136. They show V_Q versus I_Q for the bias V_{P2} at − 5 V and − 12 V, for both HIGH and LOW output.

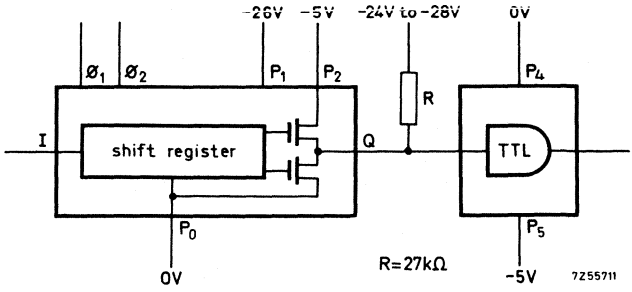
   Note: When operating with high output current levels, the maximum power rating must not be exceeded.

   The circuit shown may be used to obtain output curves for other values of V_{P2}.

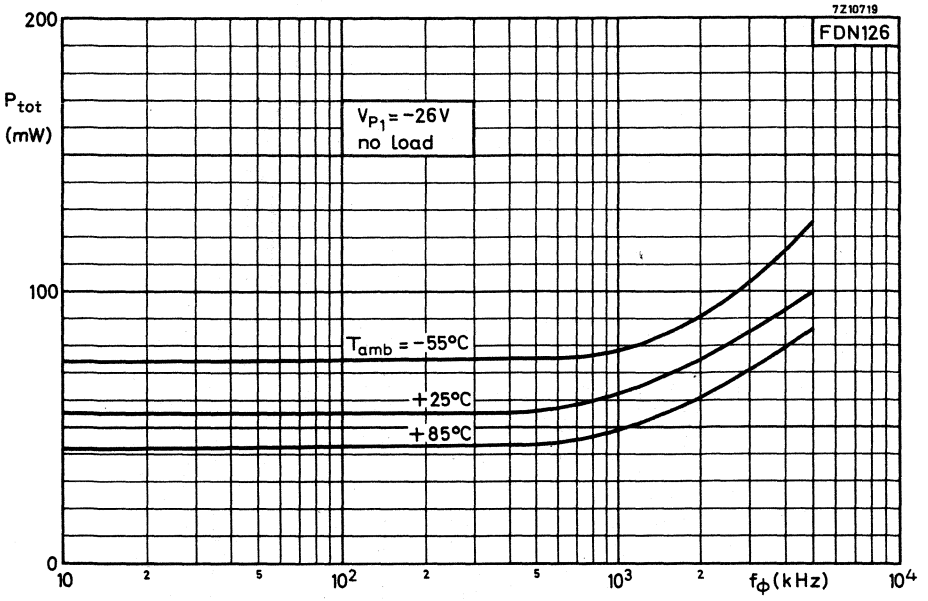


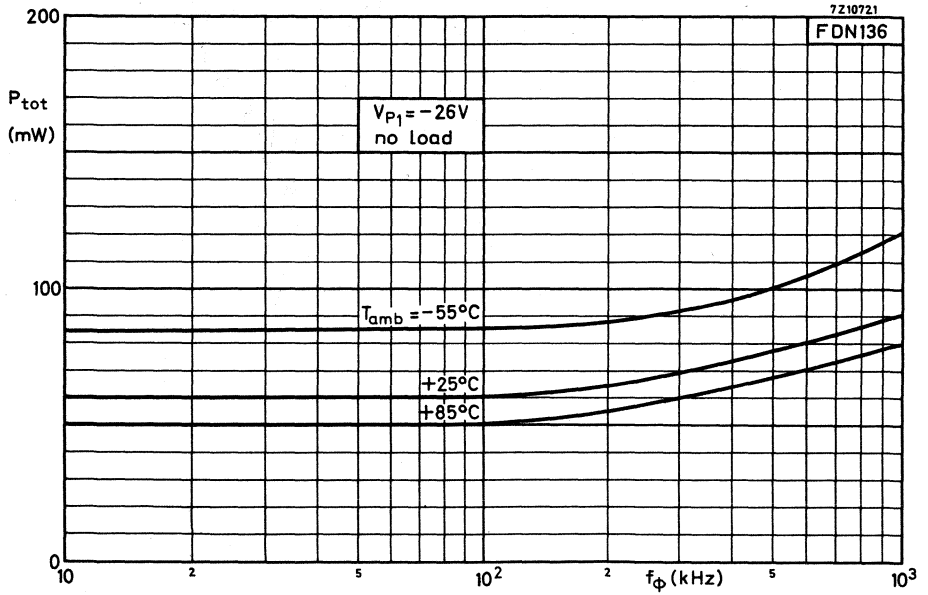


2. The bias arrangement shown is suitable for driving TTL or DTL loads direct.

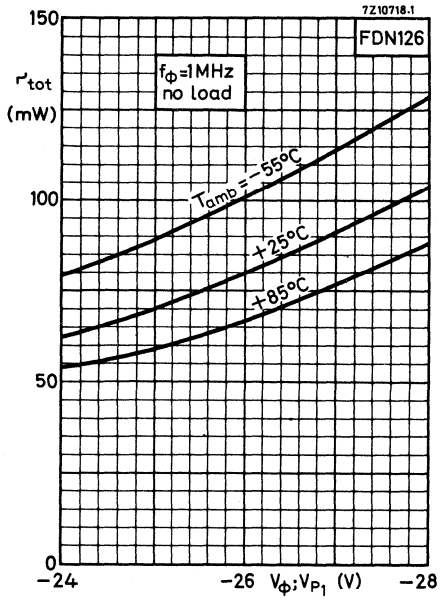


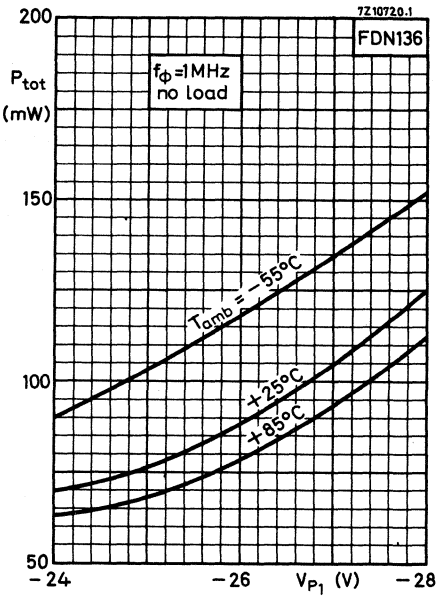
TYPICAL PERFORMANCE

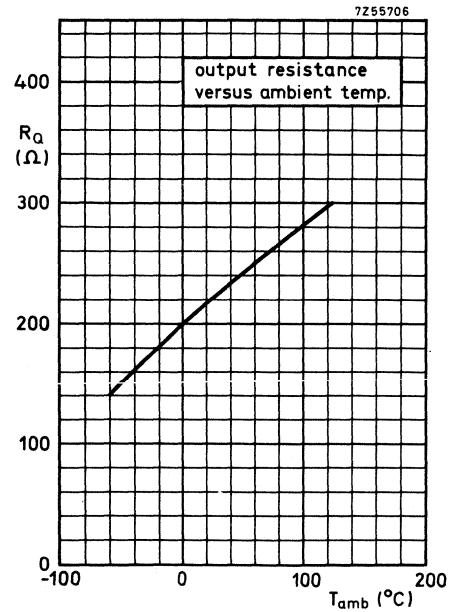


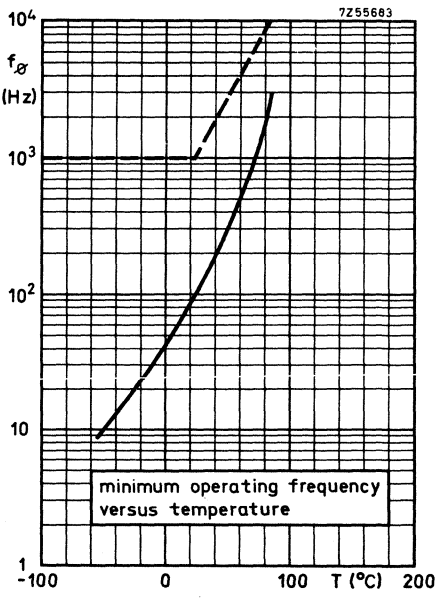


TYPICAL PERFORMANCE (continued)



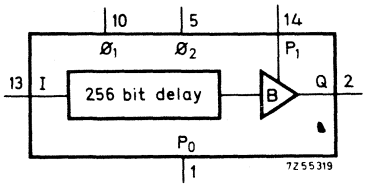


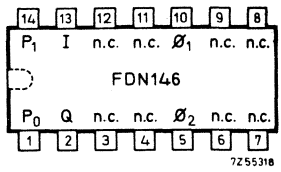


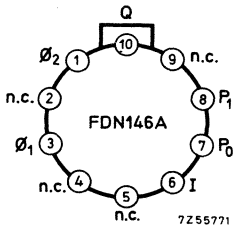


The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

256-BIT DYNAMIC SHIFT REGISTER







Pin numbers refer to FDN146 only

FDN146 : P_0 connected to metal bottom
FDN146A: P_0 connected to metal case

QUICK REFERENCE DATA			
D.C. noise margin	M_L	> 1	V
Clock rate	f_ϕ	0.01 to 3	MHz
Power consumption per bit at 10 kHz	P_{av}	< 0.002	mW
1 MHz	P_{av}	< 0.2	mW
3 MHz	P_{av}	< 0.6	mW
Power dissipation	P_{tot}	max. 300	mW
Operating ambient temperature	T_{amb}	−55 to +85	°C

GENERAL DESCRIPTION

The FDN146(A) contains one continuous 256-bit shift register with one serial input and one serial output. It dissipates very little power and uses a two-phase external clock. The device has a low impedance push-pull output buffer which, when appropriately biased is capable of interfacing direct with MOS, DTL, TTL and other loads. The buffer supply terminal P_1 is a separate supply which determines the output LOW signal only. This provides an output level that is independent of both the amplitude and width of the clock pulse. With the FDN146(A), the FDN106 (a quadruple 32-bit shift register) and FDN126 (a variable length 1 to 64 bit shift register) shift registers of any length can be built from off-the-shelf parts.

PACKAGE OUTLINE: FDN146: 14 lead metal-ceramic dual in-line (See General Section)
FDN146A: TO-100 (See General Section)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages on all data inputs, clock inputs, outputs and supply terminals with reference to P_0			+0.5 to −30	V
Power dissipation up to T_{amb} = 25 °C	FDN146 : P_{tot}	max.	800	mW
	FDN146A: P_{tot}	max.	625	mW
Junction temperature	T_j	max.	150	°C
Storage temperature	T_{stg}		−65 to +156	°C

THERMAL RESISTANCE

From junction to ambient	FDN146 : $R_{th\ j\text{-}a}$	=	156	°C/W
	FDN146A: $R_{th\ j\text{-}a}$	=	200	°C/W

CHARACTERISTICS at T_{amb} = −55 to +85 °C

	Symbol	min.	typ.	max.	Conditions and references
Clock rate	f_ϕ	0.01	–	3 MHz	
Clock pulse width	$t_{\phi 1L}$	0.125	–	1.0 μs	see timing diagram for parameter definitions
	$t_{\phi 2L}$	0.125	–	1.0 μs	
Clock pulse fall time	$t_{\phi HL}$	–	–	0.10 μs	see note 2
Clock pulse rise time	$t_{\phi LH}$	–	–	0.10 μs	
Clock delay time	$t_{\phi 1\phi 2}$	0	–	49 μs	
Clock delay time	$t_{\phi 2\phi 1}$	0	–	49 μs	
Clock pulse voltage level					
HIGH	$V_{\phi H}$	−2	0	+0.3 V	
LOW	$V_{\phi L}$	−28	−27	−26 V	see note 1
Data input logic levels					
HIGH	V_{IH}	−1.5	0	+0.3 V	
LOW	V_{IL}	−28	−12	−9 V	
Data lead time	$t_{\ell I}$	10	–	– ns	

Note 1

The FDN146(A) can be supplied in versions that will operate with −24 V to −28 V clock pulse LOW signal range.

Note 2

Above f_ϕ = 1.54 MHz $t_{\phi 1Lmin}$ and $t_{\phi 2Lmin}$ determine the maximum value of $t_{\phi HL}$ and $t_{\phi LH}$.

CHARACTERISTICS (continued)

Test conditions: V_{P_1} = −12 V to −14 V; T_{amb} = −55 to +85 °C; P_0 = grounded; standard load: 50 pF in parallel with 20 kΩ to P_0

	Symbol	min.	typ.	max.		Conditions and references
ELECTRICAL DATA						
Output levels						
HIGH	V_{QH}	−0.5	–	0	V	
LOW	V_{QL}	−14	–	−10	V	
Data input capacitance	C_I	–	2	3.5	pF	bias: V_I = 0 V; $f\phi$ = 1 MHz
Clock input capacitance	$C_{\phi 1}$, $C_{\phi 2}$	–	70	80	pF	bias: $V\phi$ = 0 V; $f\phi$ = 1 MHz
	$C_{\phi 1}$, $C_{\phi 2}$	–	45	55	pF	bias: $V\phi$ = −26 V; $f\phi$ = 1 MHz
Leakage currents:						
Data input current	$-I_{IL}$	–	–	1	μA	V_I = −15 V; all other terminals at V_{P_0}; T_{amb} = 25 °C
Clock input current	$-I_{\phi L}$	–	–	100	μA	$V\phi$ = −28 V; all other terminals at V_{P_0}; T_{amb} = 25 °C
Output resistance						
HIGH	R_{QH}	–	250	500	Ω	
LOW	R_{QL}	–	120	300	Ω	V_{P_1} = −5 V
Drive capability see note 1	V_{QL}	–	−4.8	−4.6	V	V_{P_1} = −5 V; R_L = 4 kΩ reference to P_0
Power supply current drain (see note 2)	$-I_{P_1}$	–	1.0	1.5	mA	V_{P_1} = −13 V; $f\phi$ = 1 MHz; T_{amb} = 25 °C
Output transition times:						
fall time	t_{THL}	–	70	–	ns	
rise time	t_{TLH}	–	70	–	ns	
Delay times: fall time	t_{DHL}	–	70	–	ns	
rise time	t_{DLH}	–	70	–	ns	
D.C. noise margin	M_L; M_H	1	–	–	V	

Note 1

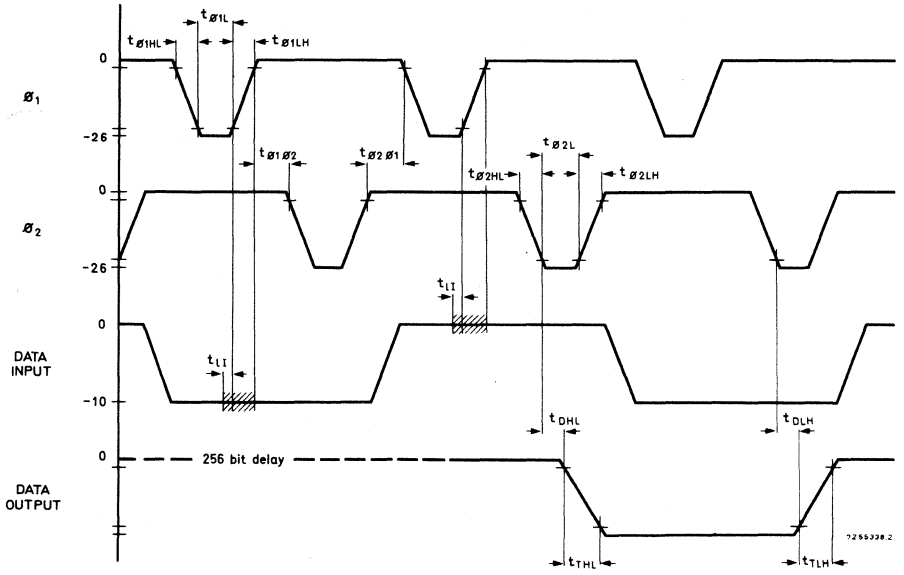
The maximum capacitive load that can be driven depends only on the speed desired and the power dissipation allowable. See the output buffer description on pages 6 and 7 for further information on output drive capability.

Note 2

The output buffer power supply current I_{P_1} is almost entirely dependent on the external load. The value shown is for a standard load of 1 MΩ, 50 pF load.

CHARACTERISTICS (continued)

TIMING DIAGRAM



Notes

1. The indicated points on the vertical axis are specified in the glossary of terms.
2. Input data must remain valid during the shaded interval to ensure proper entry into the register.

CHARACTERISTICS (continued)

GLOSSARY OF TERMS

1. Clock pulse width: $t_{\phi L}$
   The time for which the clock pulse is LOW: $V_{\phi L} \leq -26$ V

2. Clock pulse fall time: $t_{\phi HL}$
   The time between the 10% and 90% voltage points as the clock pulse goes from HIGH to LOW.

3. Clock pulse rise time: $t_{\phi LH}$
   The time between the 90% and 10% voltage points as the clock pulse goes from LOW to HIGH.

4. Clock delay time: $t_{\phi 1 \phi 2}$, $t_{\phi 2 \phi 1}$
   The least allowable time between the end of the ϕ_1 (or ϕ_2) clock pulse and the start of the ϕ_2 (or ϕ_1) clock pulse, defined at -2 V.

5. Data lead time: $t_{\ell I}$
   The time before the 90% point on the clock pulse ϕ_1 for which the voltage at the data input must be at its specified logic level in order to ensure that the data will be entered in the register.

6. Output fall transition time: t_{THL}
   The time between the 10% and 90% voltage points as the output goes from HIGH to LOW.

7. Output rise transition time: t_{TLH}
   The time between the 90% and 10% voltage points as the output goes from LOW to HIGH.

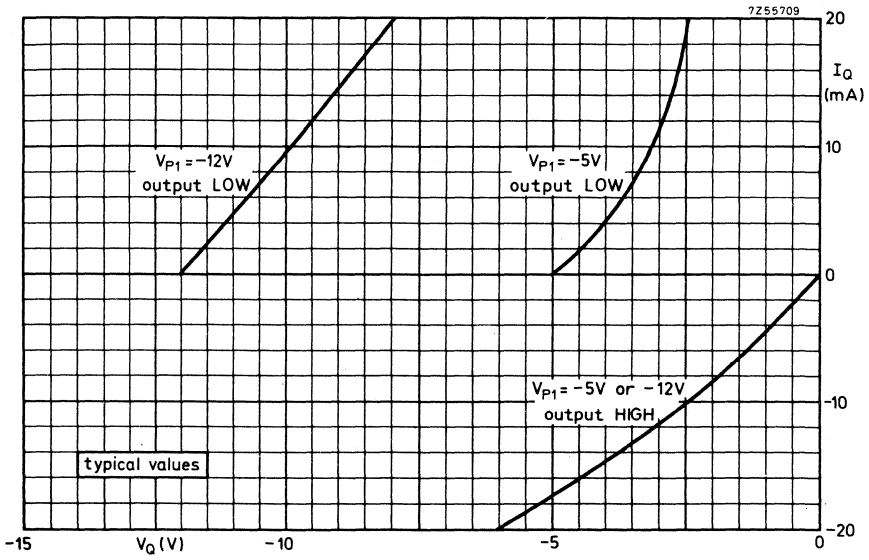
8. Fall delay time: t_{DHL}
   The delay between the clock pulse ϕ_2 reaching LOW and the output beginning to change from HIGH to LOW.

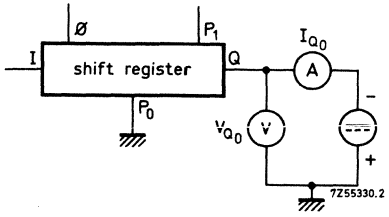
9. Rise delay time: t_{DLH}
   The delay between the clock pulse ϕ_2 reaching LOW and the output beginning to change from LOW to HIGH.

OUTPUT BUFFER DESCRIPTION

1. The curves below are typical output buffer voltage-current characteristics for the FDN146(A). They show V_Q versus I_Q for the bias V_{P_1} at −5 V and −12 V, for both HIGH and LOW output. The circuit shown may be used to obtain output curves for other values of V_{P_1}.

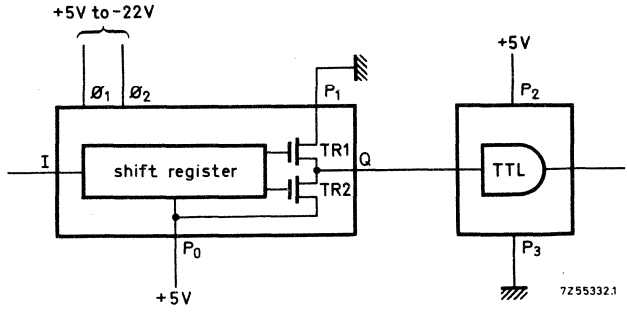
   Note: When operating with high output current levels, the maximum power rating must not be exceeded.





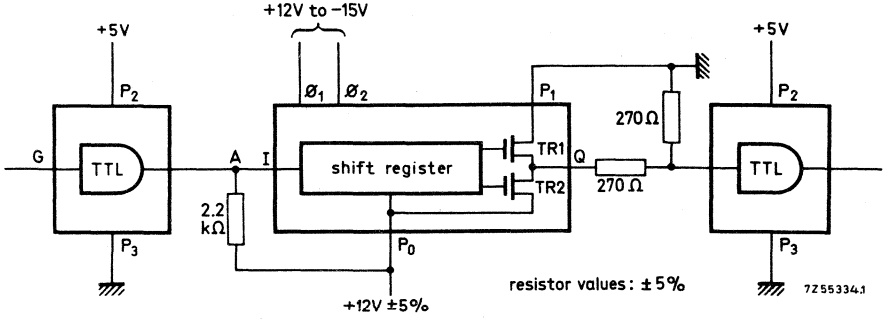
OUTPUT BUFFER DESCRIPTION (continued)

2. Biasing circuit A may be used to drive TTL or DTL loads direct. The MOS input logic levels must be referenced to V_{P_0}. TR1 and TR2 are the push-pull output driver transistors of the FDN146.



Biasing circuit A

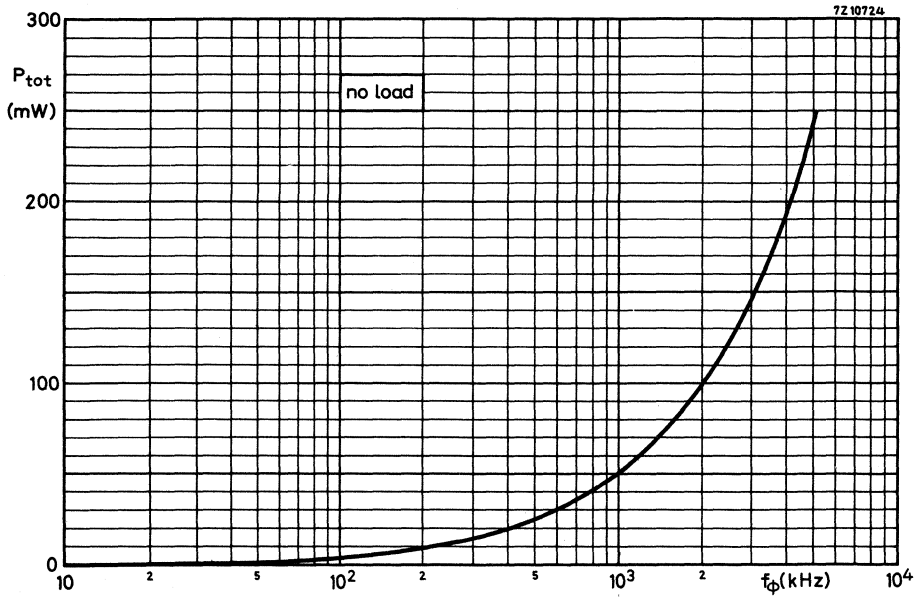
3. Biasing circuit B allows the MOS device to be interfaced with TTL or DTL at both the input and output using only passive interface components.
Note that the TTL or DTL integrated circuit must be able to withstand +12 V applied to the output lead (point A), most non-R_C type gates of our FC series and most FJ gates satisfy this requirement. Special open collector FJ gates (FJH301, 311, 321) have a minimum ouput breakdown voltage guarantee of 15 V.

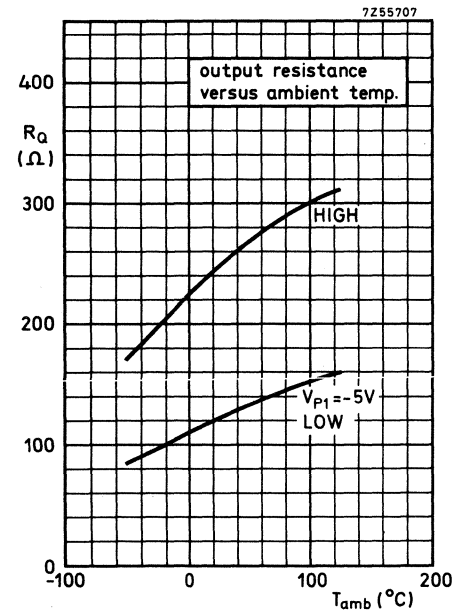


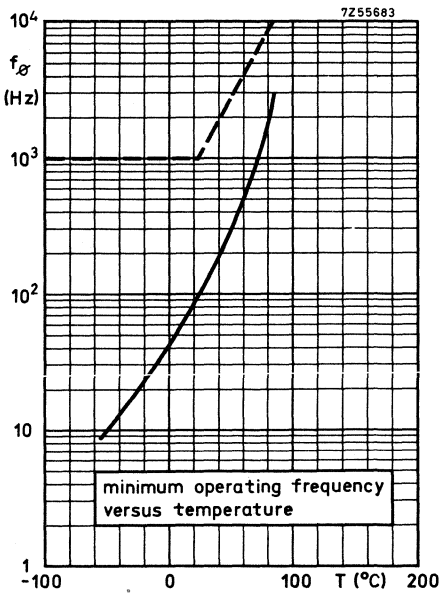
Biasing circuit B

4. To drive MOS loads direct, the bias V_{P_1} should be between −12 and −14 V to P_0.

TYPICAL PERFORMANCE

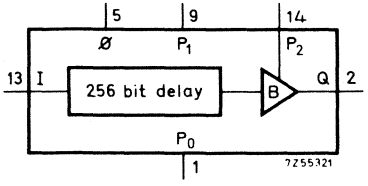


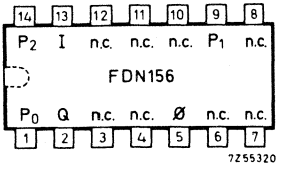


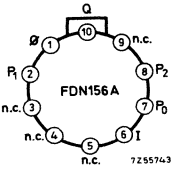


The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

256-BIT DYNAMIC SHIFT REGISTER







Pin numbers refer to FDN156 only

FDN156 : P_0 connected to the metal bottom
FDN156A: P_0 connected to the metal case

QUICK REFERENCE DATA				
Supply voltage	V_{P_1}	−26 to −28		V
D.C. noise margin	M_L	>	1	V
	M_H	>	1.5	V
Clock rate	f_ϕ	0.01 to	1	MHz
Power consumption per bit at f = 10 kHz	P_{av}	<	0.2	mW
f = 1 MHz	P_{av}	<	0.6	mW
Operating ambient temperature	T_{amb}	−55 to +85		°C

GENERAL DESCRIPTION

The FDN156A contains one 256-bit shift register with one serial input and one serial output. It dissipates very little power and uses a one-phase external clock. The device has a low impedance push-pull output buffer which, when appropriately biased is capable of interfacing direct with MOS, DTL, TTL and other loads.
The buffer supply terminal P_2 is a separate supply which determines the output LOW signal only. This provides an output level that is independent of both the amplitude and width of the clock pulse.
With the FDN156A, the FDN116 (a quadruple 32-bit shift register) and FDN136 (a variable length 1 to 64-bit shift register) shift registers of any length can be built from off-the-shelf parts.

PACKAGE OUTLINE: FDN156: 14 lead metal-ceramic dual in-line (See General Section)
FDN156A: TO-100 (See General Section)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages on all data inputs, clock inputs, outputs and supply terminals with reference to P_0			+0.5 to −30	V
Power dissipation up to T_{amb} = 25 °C	FDN156 : P_{tot}	max.	800	mW
	FDN156A: P_{tot}	max.	625	mW
Junction temperature	T_j	max.	150	°C
Storage temperature	T_{stg}		−65 to +150	°C
Total current through terminal P_2	$-I_{P2}$	max.	20	mA
Output current (per output)	$\pm I_Q$	max.	20	mA

THERMAL RESISTANCE

From junction to ambient	FDN156 : $R_{th\ j\text{-}a}$	=	156	°C/W
	FDN156A: $R_{th\ j\text{-}a}$	=	200	°C/W

CHARACTERISTICS at T_{amb} = −55 to +85 °C

	Symbol	min.	typ.	max.	Conditions and references
Clock rate	f_ϕ	0.01	–	1 MHz	
Clock pulse width	$t_{\phi L}$	0.5	–	50 μs	See timing diagram for parameter definitions
Clock pulse fall time	$t_{\phi HL}$	–	–	0.10 μs	See note 1
Clock pulse rise time	$t_{\phi LH}$	–	–	0.10 μs	
Clock pulse space	$t_{\phi H}$	0.5	–	50 μs	
Clock pulse voltage level					
HIGH	$V_{\phi H}$	−2	0	+0.3 V	
LOW	$V_{\phi L}$	−28	−12	−9 V	
Data input logic levels					
HIGH	V_{IH}	−2	0	+0.3 V	
LOW	V_{IL}	−28	−12	−9 V	
Data lead time	$t_{\ell I}$	20	–	– ns	
Data hold time	t_{iI}	75	–	– ns	
Supply voltages	V_{P_1}	−28	−26	−24 V	$f\phi \leq$ 750 kHz
	V_{P_1}	−28	−27	−26 V	$f\phi \leq$ 750 kHz
	V_{P_2}	−28	–	+0.3 V	

Note 1

The fall time specified for the FDN156(A) is to ensure that output data will meet the input hold time requirements of other shift registers, when more shift registers operate in series from a common clock. If a register does not drive other registers the clock pulse fall time may be longer.

CHARACTERISTICS (continued)

Test conditions: V_{P_1} = −26 V to −28 V; V_{P_2} = −12 V to −14 V; T_{amb} = −55 to +85 °C; P_0 = grounded; standard load: 50 pF in parallel with 20 kΩ to P_0.

	Symbol	min.	typ.	max.	Conditions and references
ELECTRICAL DATA					
Output levels					
HIGH	V_{QH}	−0.5	−	0 V	
LOW	V_{QL}	−14	−	−10 V	
Data input capacitance	C_I	−	2	3.5 pF	bias: V_I = 0 V; f_ϕ = 1 MHz
Clock input capacitance	C_ϕ	−	6	10 pF	bias: V_ϕ = 0 V; f_ϕ = 1 MHz
Leakage currents					
Data input currents	$-I_{IL}$	−	−	1 μA	V_I = −15 V; all other terminals at V_{P_0}; T_{amb} = 25 °C
Clock input current	$-I_{\phi L}$	−	−	100 μA	V_ϕ = −28 V; all other terminals at V_{P_0}; T_{amb} = 25 °C
Output resistance					
HIGH	R_{QH}	−	250	500 Ω	
LOW	R_{QL}	−	250	500 Ω	V_{P_2} = −5 V
Drive capability (see note 1)	V_{QL}	−	−4.8	−4.6 V	V_{P_2} = −5 V; R_L = 4 kΩ to reference P_0
Power supply current drain (see note 2)	$-I_{P_2}$	−	1.0	1.5 mA	V_{P_2} = −13 V; f_ϕ = 1 MHz; T_{amb} = 25 °C
	$-I_{P_1}$	−	5.0	8.0 mA	V_{P_1} = −27 V; f_ϕ = 1 MHz; T_{amb} = 25 °C
Output transition times:					
fall time	t_{THL}	−	100	− ns	
rise time	t_{TLH}	−	100	− ns	
Delay times: fall time	t_{DHL}	−	300	− ns	
rise time	t_{DLH}	−	300	− ns	
D.C. noise margin	M_L	1	−	− V	
	M_H	1.5	−	− V	

Note 1

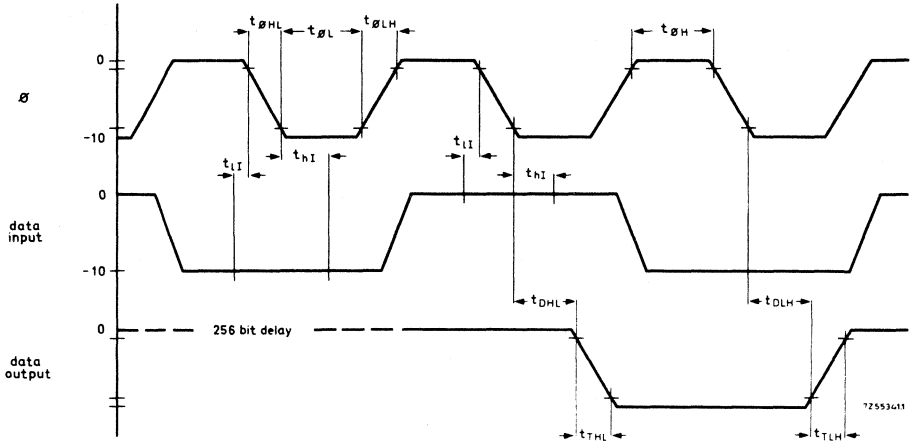
The maximum capacitive load that can be driven depends only on the speed desired and the power dissipation allowable. See the output buffer description on pages 5 and 6 for further information on output drive capability.

Note 2

The output buffer power supply current I_{P_2} is almost entirely dependent on the external load.

CHARACTERISTICS (continued)

TIMING DIAGRAM



Notes

1. The indicated points on the vertical axis are specified in the glossary of terms.

CHARACTERISTICS (continued)

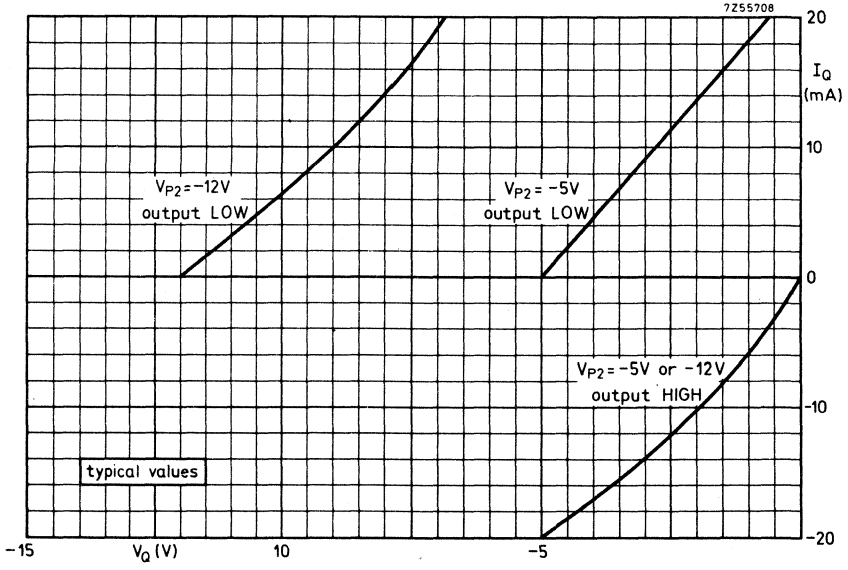
GLOSSERY OF TERMS

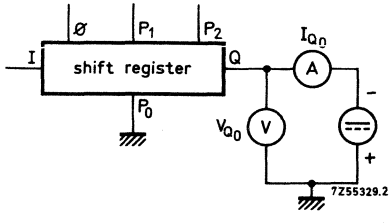
1. Clock pulse width: $t_{\phi L}$
   The time for which the clock pulse is LOW: $V_{\phi L} \leq -9$ V.
2. Clock pulse fall time: $t_{\phi HL}$
   The time between the 10% and 90% voltage points as the clock pulse goes from HIGH to LOW.
3. Clock pulse rise time: $t_{\phi LH}$
   The time between the 90% and 10% voltage points as the clock pulse goes from LOW to HIGH.
4. Clock pulse space: $t_{\phi H}$
   The least allowable time between the end of a clock pulse (ϕ) and the start of the next.
5. Data lead time: $t_{\ell l}$
   The time before the 10% point on the clock pulse for which the voltage at the data input must be at its specified logic level in order to ensure that the data will be entered in the register.
6. Data hold time: t_{hl}
   The time after the clock pulse ϕ reaches LOW for which the input data must remain stable in order to ensure that the data will be entered in the register.
7. Output fall transition time: t_{THL}
   The time between the 10% and 90% voltage points as the output goes from HIGH to LOW.
8. Output rise transition time: t_{TLH}
   The time between the 90% and 10% voltage points as the output goes from LOW to HIGH.
9. Fall delay time: t_{DHL}
   The delay between the clock pulse ϕ reaching LOW and the output beginning to change from HIGH to LOW.
10. Rise delay time: t_{DLH}
    The delay between the clock pulse ϕ reaching LOW and the output beginning to change from LOW to HIGH.

OUTPUT BUFFER DESCRIPTION

1. The curves below are typical output buffer voltage-current characteristics for the FDN156. They show V_Q versus I_Q for the bias V_{P_1} at −5 V and −12 V, for both HIGH and LOW output. The circuit shown may be used to obtain output curves for other values of V_{P_2}.

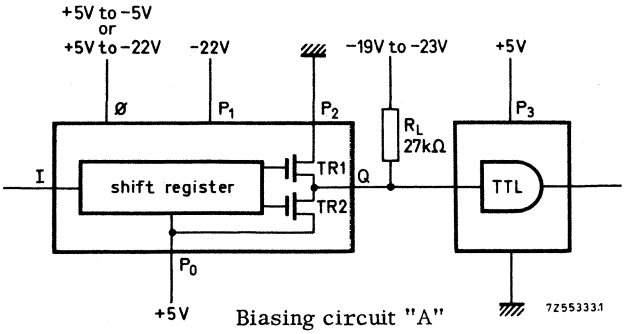
   Note: When operating with high output current levels, the maximum power rating must not be exceeded.





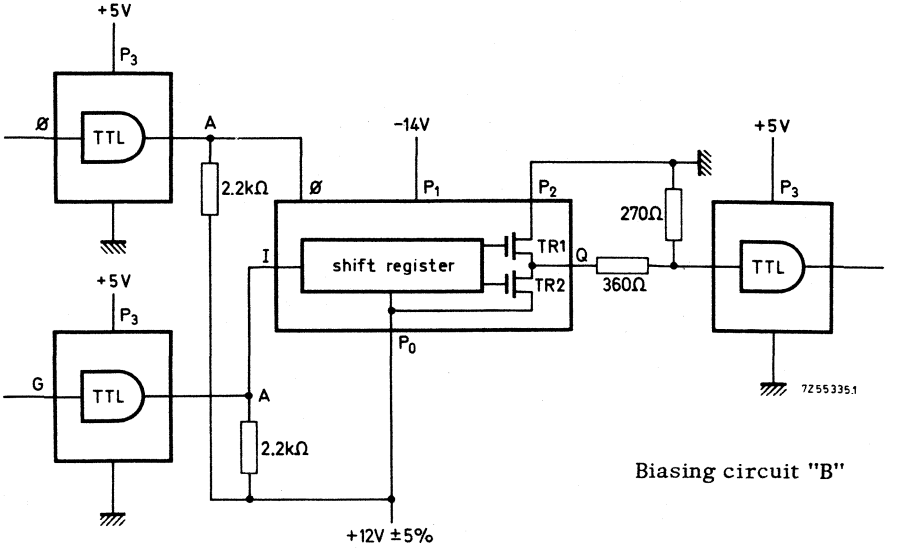
OUTPUT BUFFER DESCRIPTION

2. Biasing circuit "A" may be used to drive TTL or DTL loads direct. The MOS input logic levels must be referenced to V_{P_0}. TR1 and TR2 are the push-pull output driver transistor of the FDN156.



Biasing circuit "A"

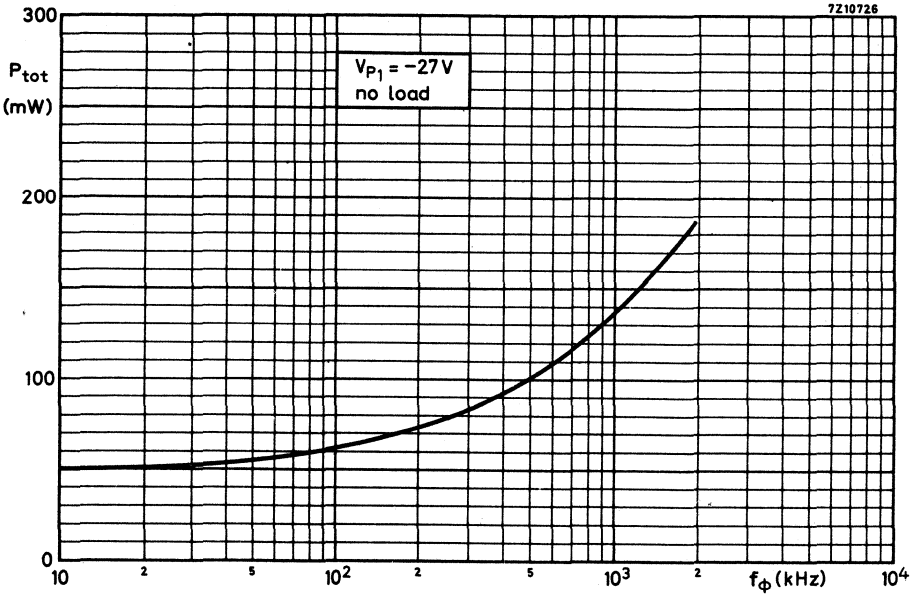
3. Biasing circuit "B" allows the MOS device to be interfaced with TTL or DTL at both input and output using only passive interface components. Note that the TTL or DTL integrated circuit must be able to withstand +10 V applied to the output lead (point A), most non-R_C type gates of our FC series and most FJ gates satisfy this requirement. Special open collector FJ gates (FJH301; 311; 321) have a minimum output breakdown voltage guarantee of 15 V.

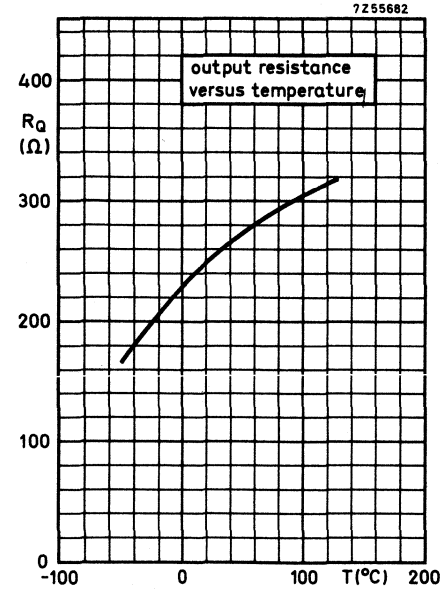


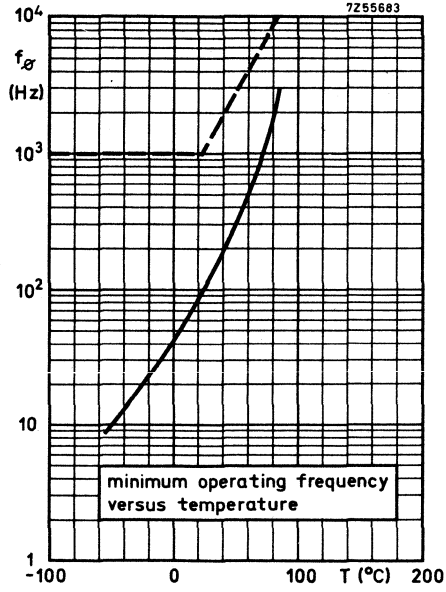
Biasing circuit "B"

4. To drive MOS loads direct, the bias V_{P_1} should be between −12 and −14 V to P_0.

TYPICAL PERFORMANCE

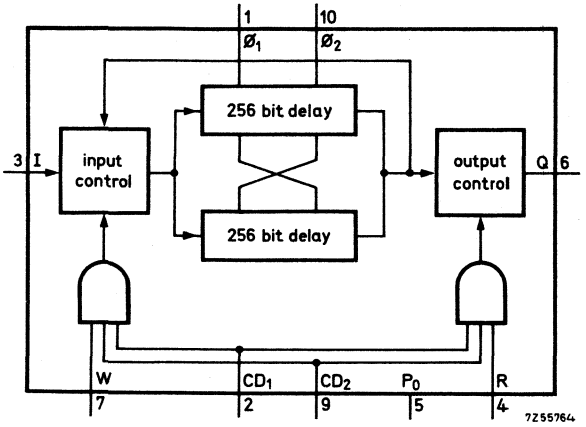


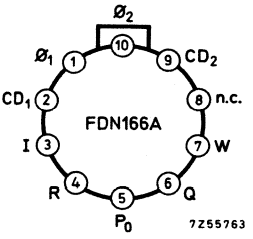




The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

512-BIT RECIRCULATING DYNAMIC SERIAL MEMORY





P_0 connected to the metal case

QUICK REFERENCE DATA			
Clock rate	f_ϕ	0.005 to 5	MHz
Data rate	f_D	0.01 to 5	MHz
Power consumption per bit			
at 1 MHz data rate	P_{av}	0.07	mW
at 5 MHz data rate	P_{av}	0.35	mW
Operating ambient temperature	T_{amb}	−55 to +85	°C

PACKAGE OUTLINE : TO-100 (See General Section)

GENERAL DESCRIPTION

The FDN166A consists of two 256-bit 2-phase dynamic shift registers, with internal multiplexing and recirculation circuitry. [1])

Data is written into and read from the device at both ϕ_1 and ϕ_2, so that the data rate is twice the clock rate. The chip disable (CD) inputs allow selection of one-out-of--many circuits in larger memories. Both CD inputs have to be in the HIGH state to activate the device. Data will be written in when W, CD_1, and CD_2 are in the HIGH state; at all other times the device is in the recirculation mode. The output is active only when R, CD_1 and CD_2 are in the HIGH state; so that the outputs of more devices can be wired-OR.

With the FDN166A large serial memories with a drum-like organisation can be made.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage on all data inputs, clock inputs, outputs and supply terminals with reference to P_0			+0.5 to −30	V
Power dissipation	P_{tot}	max.	625	mW
Junction temperature up to T_{amb} = 25 °C	T_j	max.	150	°C
Storage temperature	T_{stg}		−65 to +150	°C
Output current (per output)	$\pm I_Q$	max.	20	mA

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$	=	200	°C/W

Note

All terminals are protected against over-voltage due to static charges.

[1]) External behaviour: 512-bit shift register.

DRIVE REQUIREMENTS at T_{amb} = −55 to +85 °C; P_0 is grounded

	Symbol	min.	typ.	max.		Conditions and references
Clock rate	f_ϕ	0.05	–	1.5	MHz	$V_{\phi L}$ = −23 V
		0.05	–	2.5	MHz	$V_{\phi L}$ = −26 V
Clock pulse width	$t_{\phi L}$	0.28	–	10	µs	$V_{\phi L}$ = −23 V
		0.16	–	10	µs	$V_{\phi L}$ = −26 V
Clock pulse rise time	$t_{\phi LH}$	–	–	100	ns	
Clock pulse fall time	$t_{\phi HL}$	–	–	100	ns	
Clock delay	$t_{\phi 1\phi 2}$, $t_{\phi 2\phi 1}$	0	–	100	µs	
Clock pulse voltage levels						
HIGH	$V_{\phi H}$	−2	–	+0.3	V	
LOW	$V_{\phi L}$	−28	–	−23	V	
Data input logic levels						
HIGH	V_{IH}, V_{CDH}, V_{RH}, V_{WH}	−1	–	+0.3	V	
LOW	V_{IL}, V_{CDL}, V_{RL}, V_{WL}	−28	–	−9	V	
Data lead time for I, W, R and CD inputs	t_ℓ	50	–	–	ns	

CHARACTERISTICS at T_{amb} = −55 to +85 °C; P_0 grounded

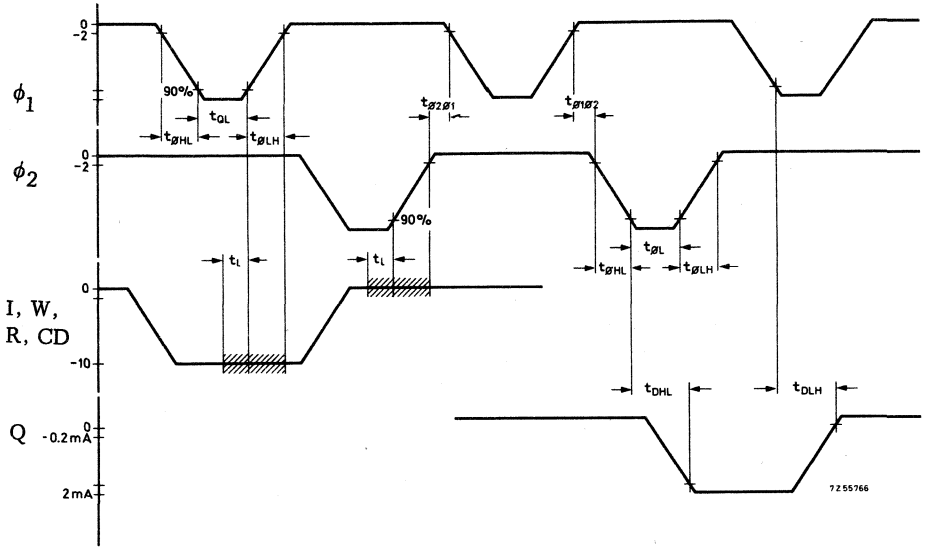
	Symbol	min.	typ.	max.	Conditions and references
Data rate	f_D	0.01	–	3 MHz	$V_{\phi L}$ = −23 V
	f_D	0.01	–	5 MHz	$V_{\phi L}$ = −26 V
Output current					
HIGH	$-I_{QH}$	2	–	– mA	V_Q = −5 V; see note
LOW	$-I_{QL}$	–	–	10 µA	V_Q = −15 V
Capacitances					
I, R, W and CD inputs	C_I	–	2.3	3.5 pF	V_I = 0 V; f = 1 MHz
Clock input capacitance	C_ϕ	–	95	110 pF	V_ϕ = 0 V; f = 1 MHz
Output capacitance	C_Q	–	2.0	2.5 pF	V_Q = 0 V; f = 1 MHz
Leakage currents					
I, R, W and CD inputs	$-I_I$	–	–	1 µA	V_I = −15 V; T_{amb} = 25 °C all other terminals at V_{P0}
Clock inputs	$-I_\phi$	–	–	100 µA	V_ϕ = −28 V; T_{amb} = 25 °C all other terminals at V_{P0}
Output resistance HIGH	R_{QH}	–	–	1 kΩ	V_Q = −5 V; See note
Delay times					
Clock input to data output	t_{DHL}, t_{DLH}	–	–	110 ns	

Note

The specified output current is measured immediately after the delay time t_{DLH}. In a steady HIGH state the output resistance decreases to less then 1 kΩ.

CHARACTERISTICS (continued)

TIMING DIAGRAM



Note

Data inputs (I, W, R, CD_1 and CD_2) must remain valid for the shaded interval to ensure proper entry.
When CD_1, CD_2 and R are HIGH during this time, the output circuit will be active during the succeeding clock pulse.

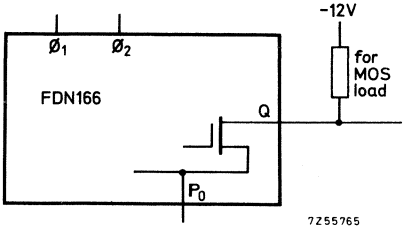
CHARACTERISTICS

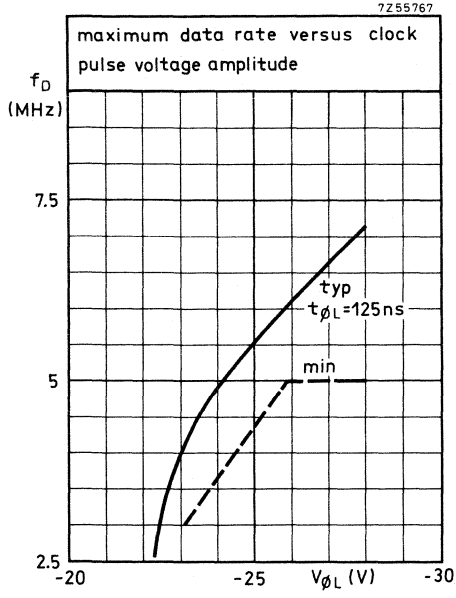
GLOSSARY OF TERMS

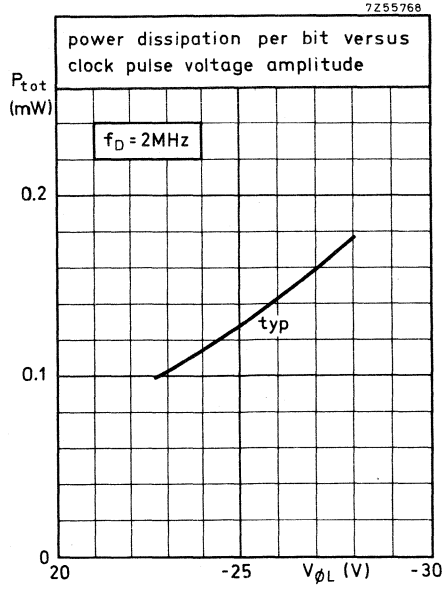
1. Clock pulse width: $t_{\phi L}$
   The time for which the clock pulse is LOW.
2. Clock pulse fall time: $t_{\phi HL}$
   The time between the 10 % and 90 % voltage points as the clock pulse goes from HIGH to LOW.
3. Clock pulse rise time: $t_{\phi LH}$
   The time between the 90 % and 10 % voltage points as the clock pulse goes from LOW to HIGH.
4. Clock delay time: $t_{\phi 1 \phi 2}$, $t_{\phi 2 \phi 1}$
   The time for which the clock pulses are simultaneously HIGH.
5. Data lead time: t_{ℓ}
   The time before the indicated point on the clock pulse for which I, R, W, CD_1 and CD_2 must be present at the inputs to ensure correct entry into the memory.
6. Delay time: t_D
   The delay between the clock pulse reaching LOW and the output beginning to change from LOW to HIGH.

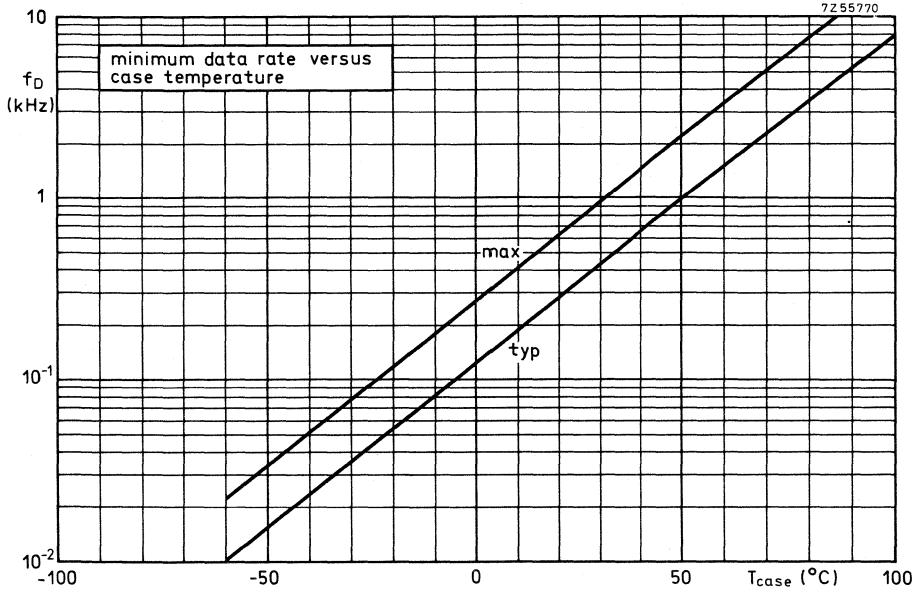
OUTPUT BUFFER DESCRIPTION

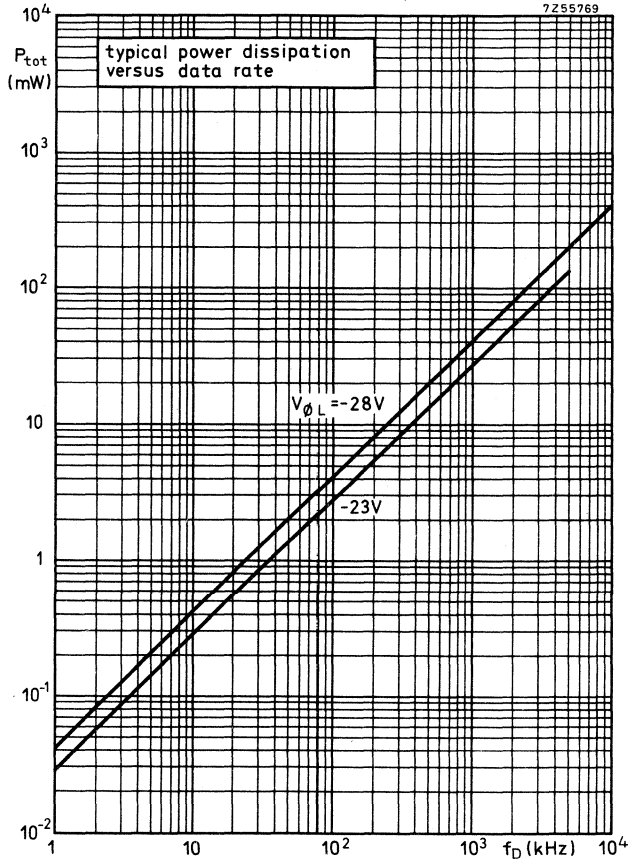
The output buffer of the FDN166A consists of an open drain MOS transistor. The source is connected to P_0, the drain to the output terminal Q. The use of this type of output allows wired-OR-ing of the outputs in expanded memories. The buffer can simply be interfaced with TTL or with other MOS circuits. In the latter case only one resistor is required; which value depends on the load capacitance and the speed desired.




7Z55767
maximum data rate versus clock pulse voltage amplitude
f_D (MHz)
7.5
5
2.5
typ
$t_{\phi L}$=125ns
min
-20
-25
$V_{\phi L}$ (V)
-30

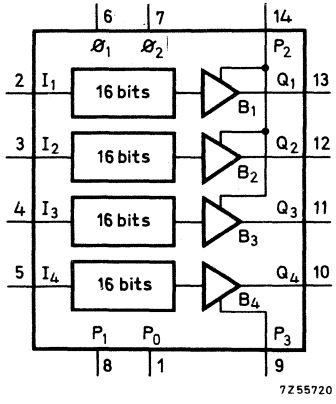

7Z55768
power dissipation per bit versus clock pulse voltage amplitude
P_{tot} (mW)
f_D = 2MHz
0.2
0.1
0
typ
20
-25
$V_{\phi L}$ (V)
-30

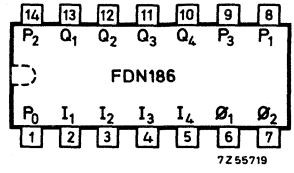

7Z55770
minimum data rate versus case temperature
f_D (kHz)
10
1
10^{-1}
10^{-2}
max
typ
-100
-50
0
50
T_{case} (°C)
100


7Z55769
typical power dissipation
versus data rate
P_{tot} (mW)
10^4
10^3
10^2
10
1
10^{-1}
10^{-2}
$V_{\phi L}$ =-28V
-23V
1
10
10^2
10^3
f_D (kHz)
10^4

The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

QUADRUPLE 16-BIT DYNAMIC SHIFT REGISTER





P0 and metal package bottom are connected.

QUICK REFERENCE DATA			
Supply voltage	V_{P_1}	−24 to −28	V
D.C. noise margin	$M_L; M_H$	> 1	V
Clock rate	f_ϕ	0.01 to 3	MHz
Power consumption per bit at 1 MHz	P_{av}	typ. 1.2	mW
Operating ambient temperature	T_{amb}	−55 to +85	°C

PACKAGE OUTLINE : 14 lead metal-ceramic dual in-line (See General Section)

GENERAL DESCRIPTION

The FDN186 package comprises 4 separate 16-bit shift registers that can be used independently or can be externally connected to make registers up to 64-bits long. Clock and power lines are common to all four registers. The output buffers are bi-directional, low impedance NRZ [1]), that by suitable biasing will directly drive MOS, DTL or TTL loads or, because they have separate output voltages (V_{P2}; V_{P3}), a combination of MOS and bipolar. V_{P2} and V_{P3} are output buffer voltages only, and the output signal is independent of the width and amplitude of the clock pulse.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage on all data inputs, clock inputs, outputs and supply terminals with reference to P_0			+0.5 to −30	V
Power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	800	mW
Junction temperature	T_j	max.	150	°C
Storage temperature	T_{stg}		−65 to +150	°C
Total current through terminals P_2 and P_3	$-I_{p2}, -I_{p3}$	max.	40	mA
Output current (per output)	$\pm I_Q$	max.	20	mA

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	156	°C/W

Note
The device is protected against over-voltage caused by static charges.

[1]) Non return to zero.

CHARACTERISTICS at T_{amb} = −55 to +85 °C

	Symbol	min.	typ.	max.		Conditions and references
Clock rate	f_ϕ	0.01	–	3	MHz	
Clock pulse width	$t_{\phi 1L}$	0.125	–	1	µs	see timing diagram for parameter def.
	$t_{\phi 2L}$	0.125	–	1	µs	
Clock pulse fall time	$t_{\phi HL}$	–	–	0.10	µs	see note 1
Clock pulse rise time	$t_{\phi LH}$	–	–	0.10	µs	see note 1
Clock delay times	$t_{\phi 1\phi 2}$	0	–	49	µs	
	$t_{\phi 2\phi 1}$	0	–	49	µs	
Clock pulse voltage level						
HIGH	$V_{\phi H}$	−2	0	+0.3	V	
LOW	$V_{\phi L}$	−28	−26	−24	V	
Data input logic level						
HIGH	V_{IH}	−1.5	0	+0.3	V	
LOW	V_{IL}	−28	−12	−9	V	
Data lead time	$t_{\ell I}$	10	–	–	ns	

1) Above f_ϕ = 1.54MHz $t_{\phi 1Lmin}$ and $t_{\phi 2Lmin}$ determine the maximum value of $t_{\phi HL}$ and $t_{\phi LH}$.

CHARACTERISTICS (continued)

Test conditions: V_{P_1} = −24 V to −28 V; $V_{P_2} = V_{P_3}$ = −12 V to −14 V; T_{amb} = −55 to +85 °C; P_0 = grounded; standard load: 50 pF in parallel with 20 kΩ to P_0

	Symbol	min.	typ.	max.		Conditions and references
ELECTRICAL DATA						
Output levels						
HIGH	V_{QH}	−0.5	–	0	V	
LOW	V_{QL}	−14	–	−10	V	
Data input capacitance	C_I	–	2	3.5	pF	bias: V_I = 0 V; f = 1 MHz
Clock input capacitance	$C_{\phi 1}, C_{\phi 2}$	–	19	25	pF	bias: V_ϕ = 0 V; f = 1 MHz
	$C_{\phi 1}, C_{\phi 2}$	–	14	18	pF	bias: V_ϕ = −26 V; f = 1 MHz
Leakage currents:						
Data input currents	$-I_{IL}$	–	–	1	μA	V_I = −15 V; all other terminals at V_{P0}; T_{amb} = 25 °C
Clock input current	$-I_{\phi L}$	–	–	100	μA	V_ϕ = −28 V; all other terminals at V_{P0}; T_{amb} = 25 °C
Output resistance						
HIGH	R_{QH}	–	300	600	Ω	
LOW	R_{QL}	–	250	500	Ω	$V_{P_2} = V_{P_3}$ = −5 V
Drive capability (see note 1 on page 5)	V_{QL}	–	−10	−8	V	R_L = 4 kΩ reference to P_0
	V_{QL}	–	−4.7	−4.4	V	$V_{P_2} = V_{P_3}$ = −5 V; R_L = 4 kΩ reference to P_0
Power supply current drain (see note 2 on page 5)	$-I_{P_1}$	–	2.0	3.0	mA	V_{P_1} = −26 V; f = 1 MHz T_{amb} = 25 °C
	$-I_{P_2}, -I_{P_3}$	–	2.4	3.0	mA	$V_{P_2} = V_{P_3}$ = −13 V; f = 1 MHz T_{amb} = 25 °C
Output transition times:						
fall time	t_{THL}	–	100	–	ns	
rise time	t_{TLH}	–	100	–	ns	
Delay times: fall time	t_{DHL}	–	80	–	ns	
rise time	t_{DLH}	–	80	–	ns	
D.C. noise margin	M_L, M_H	1	–	–	V	

CHARACTERISTICS (continued)

Note 1 (see page 4)

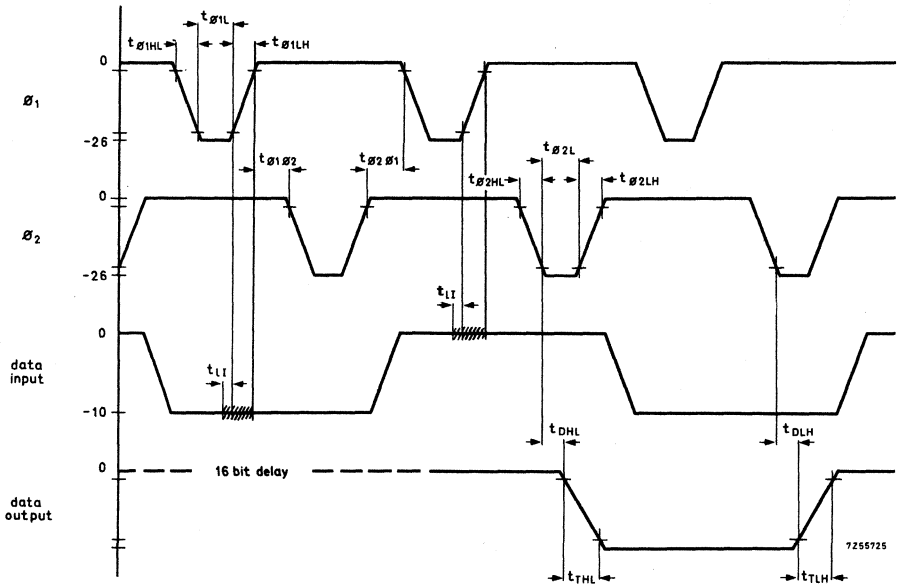
The maximum capacitive load that can be driven depends only on the speed deisred and the power dissipation allowable. See the output buffer description on page 8 for further information on output drive capability.

Note 2 (see page 4)

The output buffer power supply currents (I_{P_2}, I_{P_3}) are almost entirely dependent on the external load.

CHARACTERISTICS (continued)

TIMING DIAGRAM



Timing diagram note:

Input data must remain valid for the shaded interval to ensure proper entry into the register.

Note

The indicated points on the vertical axes are specified in the glossary of terms.

CHARACTERISTICS (continued)

GLOSSARY OF TERMS

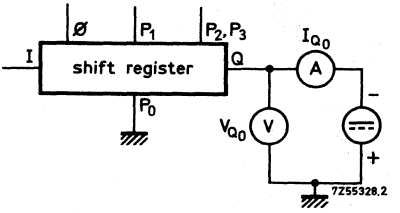
1. Clock pulse width: $t_{\phi L}$
   The time for which the clock pulse is LOW: $V_{\phi L} \leq -24$ V
2. Clock pulse fall time: $t_{\phi HL}$
   The time between the 10% and 90% voltage points as the clock pulse goes from HIGH to LOW.
3. Clock pulse rise time: $t_{\phi LH}$
   The time between the 90% and 10% voltage points as the clock pulse goes from LOW to HIGH.
4. Clock delay time: $t_{\phi 1\phi 2}$, $t_{\phi 2\phi 1}$
   The time between the end of the $\phi 1$ (or $\phi 2$) clock pulse and the start of the $\phi 2$ (or $\phi 1$) clock pulse, defined at -2 V.
5. Data lead time: $t_{\ell I}$
   The time before the 90% point on the clock pulse $\phi 1$ for which the voltage at the input must be at its specified logic level in order to ensure that the data will be entered in the register.
6. Output fall transition time: t_{THL}
   The time between the 10% and 90% voltage points as the output goes from HIGH to LOW.
7. Output rise transition time: t_{TLH}
   The time between the 90% and 10% voltage points as the output goes from LOW to HIGH.
8. Fall delay time: t_{DHL}
   The delay between the clock pulse $\phi 2$ reaching LOW and the output beginning to change from HIGH to LOW.
9. Rise delay time: t_{DLH}
   The delay between the clock pulse $\phi 2$ reaching LOW and the output beginning to change from LOW to HIGH.

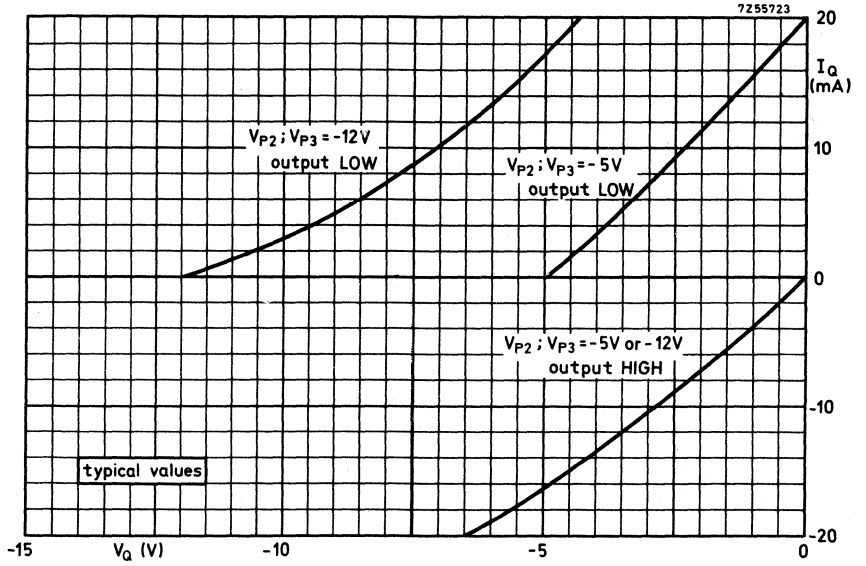
OUTPUT BUFFER DESCRIPTION

1. The curves below are typical output buffer voltage-current characteristics for the FDN186. They show V_Q versus I_Q for the V_{P2} and V_{P3} at −5 V and −12 V, for both HIGH and LOW output.

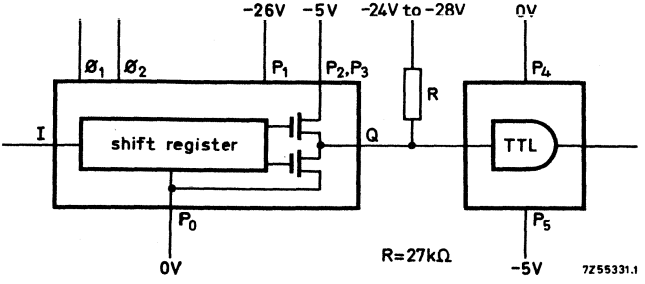
   Note: When operating with high output current levels, the maximum power rating must not be exceeded.

The circuit shown may be used to obtain output curves for other values of V_{P2} and V_{P3}.

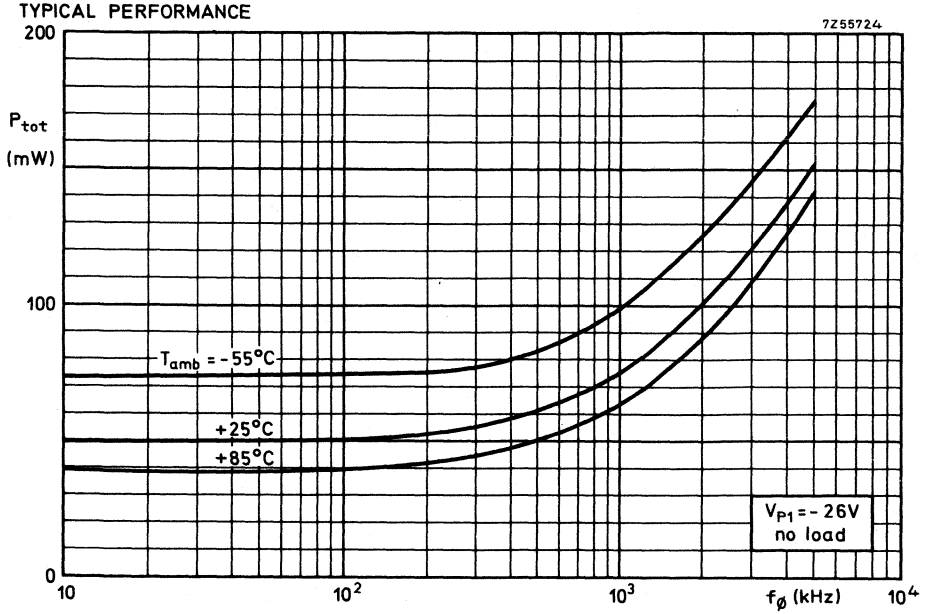


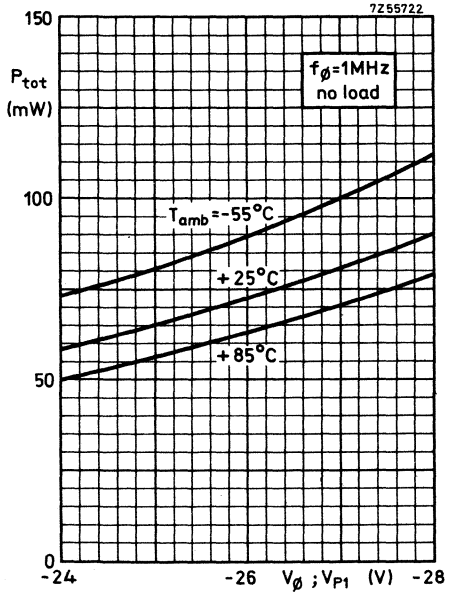


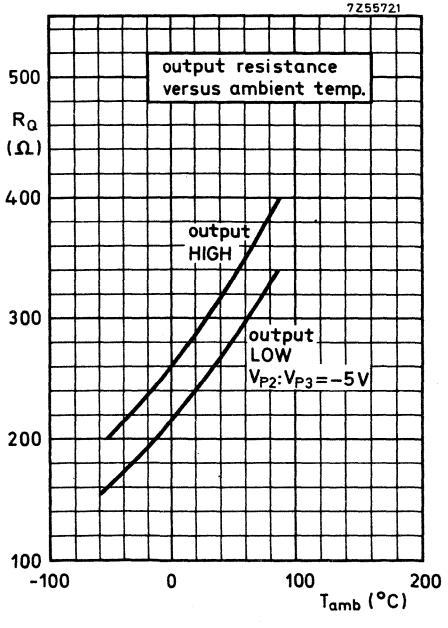
2. The bias arrangement shown is suitable for driving TTL or DTL loads direct.



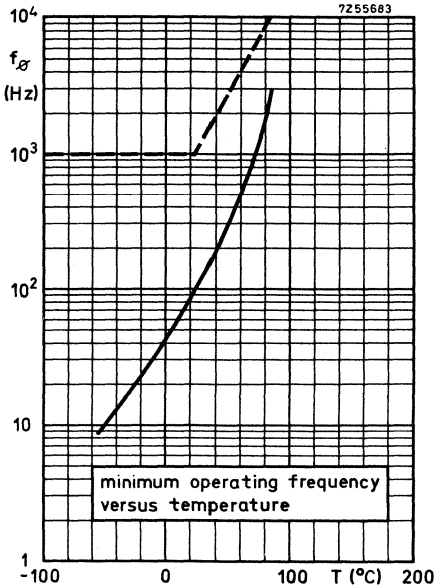
TYPICAL PERFORMANCE





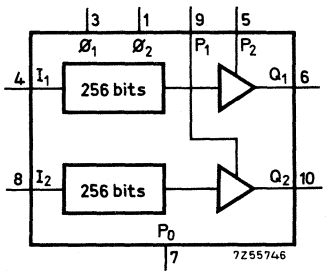


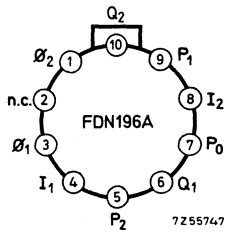
TYPICAL PERFORMANCE (continued)



The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enchancement mode technology.

DUAL 256-BIT DYNAMIC SHIFT REGISTER





P_0 connected to metal case

QUICK REFERENCE DATA			
Clock rate	f_ϕ	0.01 to 3	MHz
Power consumption per bit at f_ϕ = 3 MHz	P_{av}	typ. 0.36	mW
Operating ambient temperature	T_{amb}	−55 to +85	°C
D.C. noise margin	M_H; M_L	> 1	V

PACKAGE OUTLINE: TO-100 (See General Section)

GENERAL DESCRIPTION

The FDN196A consists of two 256-bit 2-phase dynamic shift registers, with common clock lines.
The device has two low impedance push-pull output buffers, with separate supply voltages. Thus the two outputs may be independently biased to drive a bipolar load or other MOS circuits.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage on all data inputs, clock inputs, outputs and supply terminals with reference to P_0		+0.5	−30	V
Power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	625	mW
Junction temperature	T_j	max.	150	°C
Storage temperature	T_{stg}	−65 to	+150	°C
Total current through terminals P_1, P_2	$-I_{P_1}$, $-I_{P_2}$	max.	20	mA
Output current (per output)	$\pm I_Q$	max.	20	mA

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$	=	200	°C/W

Note
All terminals are protected against over-voltage due to static charges.

DRIVE REQUIREMENTS at T_{amb} = −55 to +85 °C; P_0 is grounded

	Symbol	min.	typ.	max.		Conditions and references
Clock rate	f_ϕ	0.01	–	3	MHz	
Clock pulse width	$t_{\phi 1L}$	0.125	–	5.0	µs	
	$t_{\phi 2L}$	0.125		5.0	µs	
Clock pulse rise time	$t_{\phi LH}$	–	–	0.5	µs	
Clock pulse fall time	$t_{\phi HL}$	–	–	0.5	µs	
Clock delay	$t_{\phi 1\phi 2}, t_{\phi 2\phi 1}$	0	–	45	µs	
Clock pulse voltage levels						
HIGH	$V_{\phi H}$	−2	0	+0.3	V	
LOW	$V_{\phi L}$	−28	−26	−24	V	
Data input logic levels						
HIGH	V_{IH}	−2	0	+0.3	V	
LOW	V_{IL}	−28	−12	−9	V	
Data lead time	$t_{\ell I}$	10	–	–	ns	
Buffer supply voltages	$-V_{P1}, -V_{P2}$	0	–	14	V	

CHARACTERISTICS

Test conditions: $V_{P1} = V_{P2} = -12$ to -14 V; $T_{amb} = -55$ to $+85\,^{o}C$; P_0 = grounded
standard load: 50 pF in parallel with 20 kΩ to P_0.

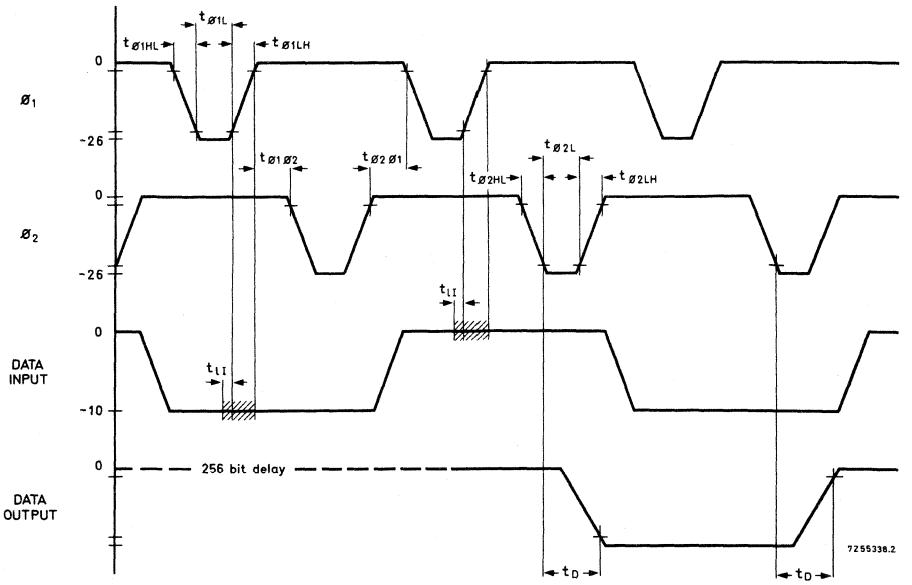
ELECTRICAL DATA	Symbol	min.	typ.	max.		Conditions and references
Output levels						
HIGH	V_{QH}	−0.5	–	0	V	
LOW	V_{QL}	−14	–	−10	V	
Data input capacitance	C_I	–	2	3.5	pF	V_I = 0 V; f = 1 MHz
Clock input capacitances	$C_{\phi 1}, C_{\phi 2}$	–	90	110	pF	V_ϕ = 0 V; f = 1 MHz
	$C_{\phi 1}, C_{\phi 2}$	–	60	80	pF	V_ϕ = −26 V; f = 1 MHz
Leakage currents						
Data input current	$-I_{IL}$	–	–	1	μA	V_I = −15 V; all other terminals at P_0; T_{amb} = 25 °C
Clock input current	$-I_{\phi L}$	–	–	100	μA	V_ϕ = −28 V; all other terminals at P_0; T_{amb} = 25 °C
Output resistance						
HIGH	R_{QH}	–	250	500	Ω	
LOW	R_{QL}	–	150	300	Ω	V_{P1}, V_{P2} = −5 V
Supply currents	$-I_{P1}, -I_{P2}$	–	−0.68	−1.0	mA	V_{P1}, V_{P2} = −13 V; f = 1 MHz; T_{amb} = 25 °C; See note
Delay time						
Clock to output	t_D	–	135	275	ns	

Note

The output buffer power supply current is almost entirely dependent on the external load. The value shown is for a load of 50 pF is parallel with 1 MΩ to P_0.

CHARACTERISTICS (continued)

TIMING DIAGRAM



Notes

1. The indicated points on the vertical axis are specified in the glossary of terms.
2. With the FDN196A the data inputs must also remain valid for the $t_{\phi}LH$.
3. Data inputs must remain valid for the shaded interval to ensure proper entry into the register.

CHARACTERISTICS (continued)

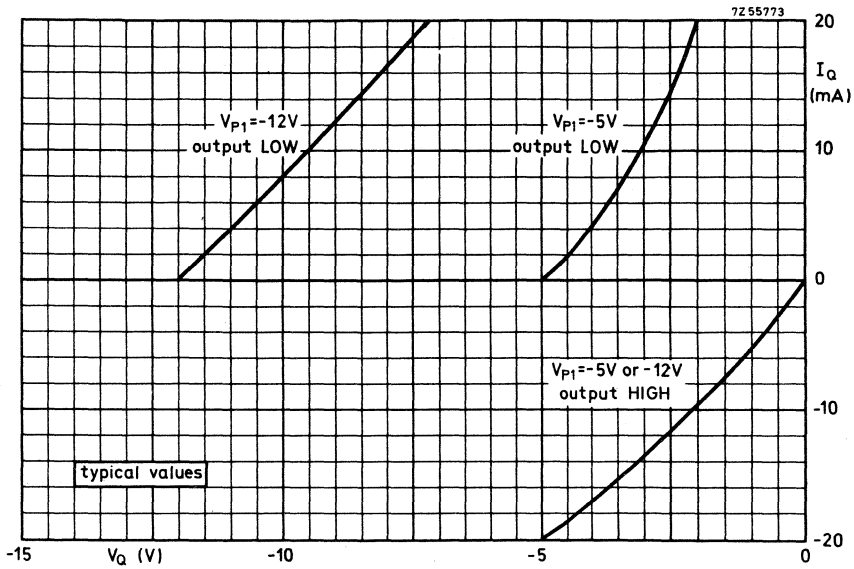
GLOSSARY OF TERMS

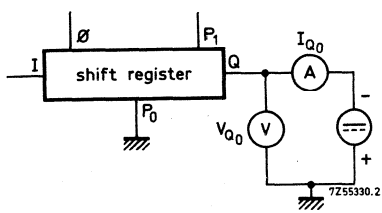
1. Clock pulse width: $t_{\phi L}$
   The time for which the clock pulse is LOW: $V_{\phi L} \leq -26$ V
2. Clock pulse fall time: $t_{\phi HL}$
   The time between the 10% and 90% voltage points as the clock pulse goes from HIGH to LOW.
3. Clock pulse rise time: $t_{\phi LH}$
   The time between the 90% and 10% voltage points as the clock pulse goes from LOW to HIGH.
4. Clock delay time: $t_{\phi 1\phi 2}$, $t_{\phi 2\phi 1}$
   The last allowable time between the end of the ϕ_1 (or ϕ_2) clock pulse and the start of the ϕ_2 (or ϕ_1) clock pulse, defined at -2 V.
5. Data lead time: $t_{\ell I}$
   The time before the 90% point on the clock pulse ϕ_1 for which the voltage at the data input must be at its specified logic level in order to ensure that the data will be entered in the register.
6. Delay time: t_D
   The delay between the clock pulse ϕ_2 reaching LOW and the output reaching its logic level.

OUTPUT BUFFER DESCRIPTION

1. The curves below are typical output buffer voltage-current characteristics for the FDN196A. They show V_Q versus I_Q for the bias V_{P_1} at −5 V and −12 V, for both HIGH and LOW output. The circuit shown may be used to obtain LOW output curves for other values of V_{P_1}.

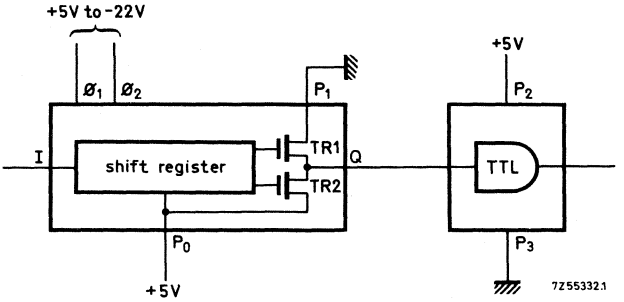
   Note: When operating with high output current levels, the maximum power rating must not be exceeded.





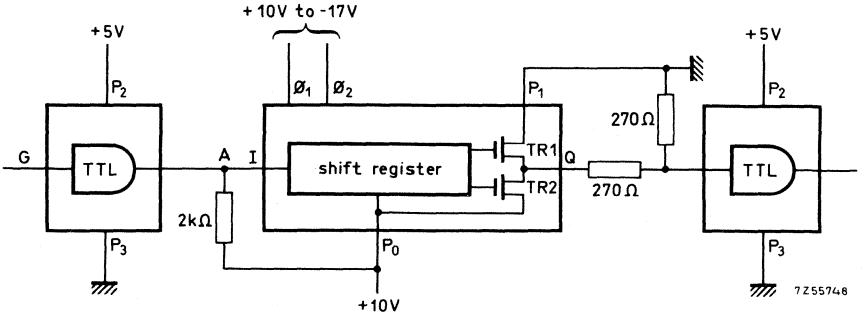
OUTPUT BUFFER DESCRIPTION (continued)

2. Biasing circuit A may be used to drive TTL or DTL loads direct. The MOS input logic levels must be referenced to V_{P0}. TR1 and TR2 are the push-pull output driver transistors of the FDN146.



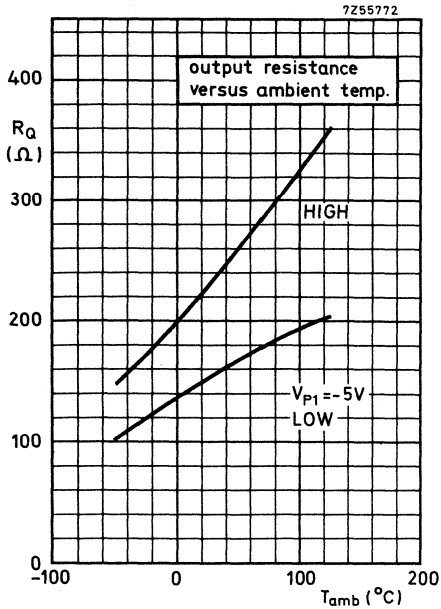
Biasing circuit A

3. Biasing circuit B allows the MOS device to be interfaced with TTL or DTL at and output using only passive interface components.
Note that the TTL or DTL integrated circuit must be able to withstand +10 V applied to the output lead (point A), most circuits of our FC series and most FJ gates satisfy this requirement. Some open collector FJ gates have a minimum output breakdown voltage guarantee of 15 V.



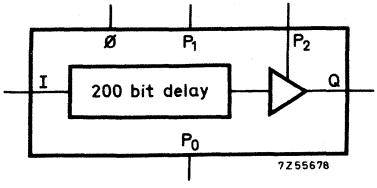
Biasing circuit B

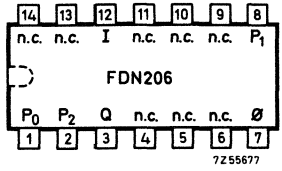
4. To drive MOS loads direct, the bias V_{P1} should be between −12 and −14 V to P_0.

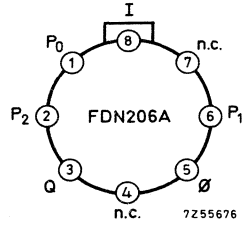

7Z55772
output resistance
versus ambient temp.
400
R_Q
(Ω)
300
200
100
0
HIGH
V_{P1} = -5V
LOW
−100
0
100
200
T_{amb} (°C)

The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

200-BIT DYNAMIC SHIFT REGISTER







FDN206 : P_0 connected to the metal bottom
FDN206A: P_0 connected to the metal case

QUICK REFERENCE DATA			
Supply voltage	V_{P1}	−26 to −28	V
D. C. noise margin	M_L; M_H	> 1	V
Clock rate	f_ϕ	0.01 to 1	MHz
Power consumption per bit at $f\phi$ = 10 kHz	P_{av}	< 0.2	mW
$f\phi$ = 1 MHz	P_{av}	< 0.6	mW
Operating ambient temperature	T_{amb}	−55 to +85	°C

PACKAGE OUTLINES: FDN206 ; 14 lead dual in-line (See General Section)
FDN206A; TO-99 (See General Section)

GENERAL DESCRIPTION

The FDN206 contains one 200-bit shift register with one serial input and one serial output. It dissipates little power and uses a one-phase external clock. The device has a low impedance push-pull output buffer which, when appropriately biased is capable of interfacing direct with MOS, DTL, TTL and other loads.
The buffer supply terminal P_2 is a separate supply which determines the output LOW signal only. This provides an output level that is independent of both the amplitude and width of the clock pulse.
With the FDN206, the FDN116 (a quadruple 32-bit shift register) and FDN136 (a variable length 1 to 64-bit shift register) shift registers of any required length can be built from off-the-shelf parts.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages on all data inputs, clock inputs, outputs and supply terminals with reference to P_0				+0.5 to −30	V
Power dissipation up to T_{amb} = 25 °C	FDN206 :	P_{tot}	max.	800	mW
	FDN206A:	P_{tot}	max.	625	mW
Junction temperature		T_j	max.	150	°C
Storage temperature		T_{stg}		−65 to +150	°C
Total current through terminal P_2		$-I_{P_2}$	max.	40	mA
Output current (per output)		$\pm I_Q$	max.	20	mA

THERMAL RESISTANCE

From junction to ambient	FDN206 :	$R_{th\ j-a}$	=	156	°C/W
	FDN206A:	$R_{th\ j-a}$	=	200	°C/W

CHARACTERISTICS at $T_{amb} = -55$ to $+85$ °C

	Symbol	min.	typ.	max.		Conditions and references
Clock rate	f_ϕ	0.01	–	1	MHz	
Clock pulse width	$t_{\phi L}$	0.45	–	50	µs	See timing diagram for parameter definitions
Clock pulse fall time	$t_{\phi HL}$	–	–	0.10	µs	See note
Clock pulse rise time	$t_{\phi LH}$	–	–	0.10	µs	
Clock pulse space	$t_{\phi H}$	0.45	–	50	µs	
Clock pulse voltage level						
HIGH	$V_{\phi H}$	−2	0	+0.3	V	
LOW	$V_{\phi L}$	−28	−12	−9	V	
Data input logic levels						
HIGH	V_{IH}	−2	0	+0.3	V	
LOW	V_{IL}	−28	−12	−9	V	
Data lead time	$t_{\ell I}$	20	–	–	ns	
Data hold time	t_{hI}	75	–	–	ns	
Supply voltages	V_{P1}	−28	−26	−24	V	$f_\phi \leq 750$ kHz
	V_{P1}	−28	−27	−26	V	$f_\phi \geq 750$ kHz
	V_{P2}	−28	–	+0.3	V	

Note

The fall time specified for the FDN206 is to ensure that output data will meet the input hold time requirements of other shift registers, when more shift registers are operating in series from a common clock. If a register does not drive other registers the clock fall time may be longer.

CHARACTERISTICS (continued)

Test conditions: V_{P_1} = −26 V to −28 V; V_{P_2} = −12 V to −14 V; T_{amb} = −55 to +85 °C; P_0 = grounded; standard load; 50 pF in parallel with 20 kΩ to P_0.

	Symbol	min.	typ.	max.		Conditions and references
ELECTRICAL DATA						
Output levels						
HIGH	V_{QH}	−0.5	−	0	V	
LOW	V_{QL}	−14	−	−10	V	
Data input capacitance	C_I	−	2	3.5	pF	bias: V_I = 0 V; f_ϕ = 1 MHz
Clock input capacitance	C_ϕ	−	6	10	pF	bias: V_ϕ = 0 V; f_ϕ = 1 MHz
Leakage currents						
Data input currents	$-I_{IL}$	−	−	1	μA	V_I = −15 V; all other terminals at V_{P_0}; T_{amb} = 25 °C
Clock input current	$-I_{\phi L}$	−	−	100	μA	V_ϕ = −28 V; all other terminals at V_{P_0}; T_{amb} = 25 °C
Output resistance:						
HIGH	R_{QH}	−	250	500	Ω	
LOW	R_{QL}	−	250	500	Ω	V_{P_2} = −5 V
Drive capability (see note 1)	V_{QL}	−	−4.8	−4.6	V	V_{P_2} = −5 V; R_L = 4 kΩ to reference P_0
Supply current (see note 2)	$-I_{P_2}$	−	1.0	1.5	mA	V_{P_2} = −13 V; f_ϕ = 1 MHz; T_{amb} = 25 °C
	$-I_{P_1}$	−	5.0	8.0	mA	V_{P_1} = −27 V; f_ϕ = 1 MHz; T_{amb} = 25 °C
Output transition times:						
fall time	t_{THL}	−	100	−	ns	
rise time	t_{TLH}	−	100	−	ns	
Delay times: fall time	t_{DHL}	−	300	−	ns	
rise time	t_{DLH}	−	300	−	ns	
D.C. noise margin	M_L	1	−	−	V	
	M_H	1.5	−	−	V	

Note 1

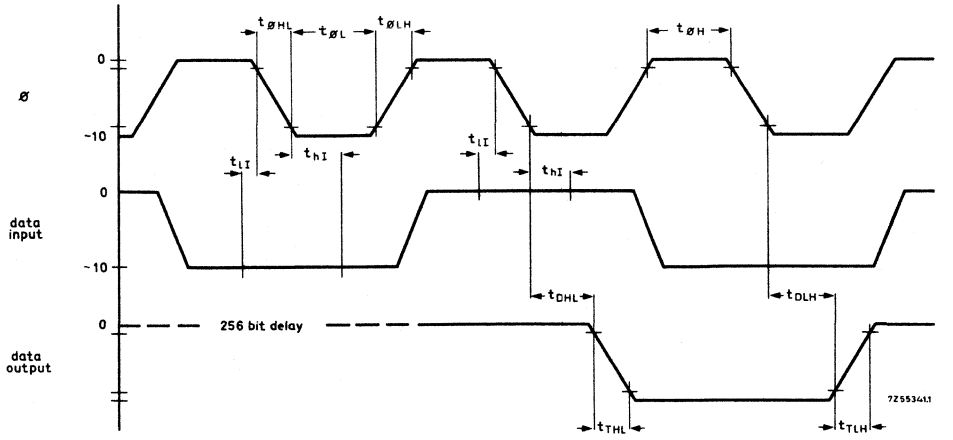
The maximum capacitive load that can be driven depends only on the speed desired and the power dissipation allowable. See the output buffer description on pages 7 and 8 for further information on output drive capability.

Note 2

The output buffer supply current I_{P_2} is almost entirely dependent on the external load.

CHARACTERISTICS (continued)

TIMING DIAGRAM



Note

The indicated points on the vertical axis are specified in the glossary of terms.

CHARACTERISTICS (continued)

GLOSSARY OF TERMS

1. Clock pulse width: $t_{\phi L}$
   The time for which the clock pulse is LOW: $V_{\phi L} \leq -9$ V.

2. Clock pulse fall time: $t_{\phi HL}$
   The time between the 10% and 90% voltage points as the clock pulse goes from HIGH to LOW.

3. Clock pulse rise time: $t_{\phi LH}$
   The time between the 90% and 10% voltage points as the clock pulse goes from LOW to HIGH.

4. Clock pulse space: $t_{\phi H}$
   The least allowable time between the end of one clock pulse (ϕ) and the start of the next.

5. Data lead time: $t_{\ell I}$
   The time before the 10% point on the clock pulse for which the voltage at the data input must be at its specified logic level in order to ensure that the data will be entered in the register.

6. Data hold time: t_{hI}
   The time after the clock pulse ϕ reaches LOW for which the input data must remain stable to guarantee that it will be entered in the register.

7. Output fall transition time: t_{THL}
   The time between the 10% and 90% voltage points as the output goes from HIGH to LOW.

8. Output rise transition time: t_{TLH}
   The time between the 90% and 10% voltage points as the output goes from LOW to HIGH.

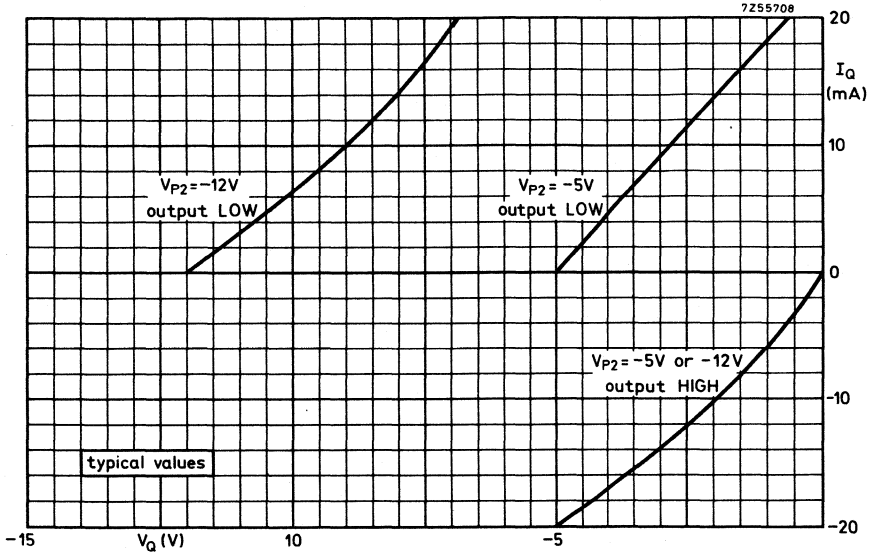
9. Fall delay time: t_{DHL}
   The delay between the clock pulse ϕ reaching LOW and the output beginning to change from HIGH to LOW.

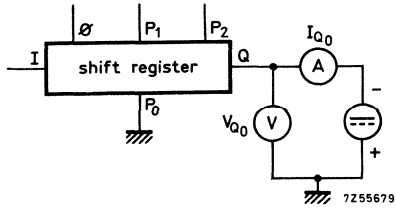
10. Rise delay time: t_{DLH}
    The delay between the clock pulse ϕ reaching LOW and the output beginning to change from LOW to HIGH.

OUTPUT BUFFER DESCRIPTION

1. The curves below are typical output buffer voltage-current characteristics for the FDN206. They show V_Q versus I_Q for the bias V_{P1} at −5 V and −12 V, for both HIGH and LOW output. The circuit shown may be used to obtain LOW output curves for other values of V_{P2}.

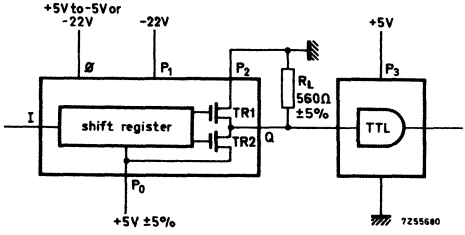
   Note: When operating with high output current levels, the maximum power rating *must not be exceeded.*





OUTPUT BUFFER DESCRIPTION (continued)

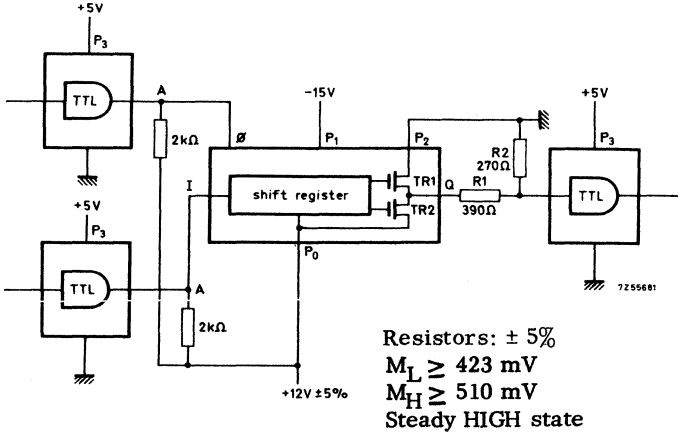
2 Biasing circuit A may be used to drive TTL or DTL loads direct. The MOS input logic levels must be referenced to V_{P_0}. TR1 and TR2 are the push-pull output driver transistors of the FDN206.



$M_L \geq 368$ mV
$M_H \geq 458$ mV
Steady HIGH state dissipation ≤ 13 mW

Biasing circuit A

3. Biasing circuit B allows the MOS device to be interfaced with TTL or DTL at both input and output using only passive interface components. Note that the TTL or DTL integrated circuit must be able to withstand +10 V applied to the output lead (point A); most non-R_C type circuits of our FC series and most FJ gates satisfy this requirement. Some open collector FJ gates have a minimum output breakdown voltage guarantee of 15 V (FJH301; FJH311; FJH321).

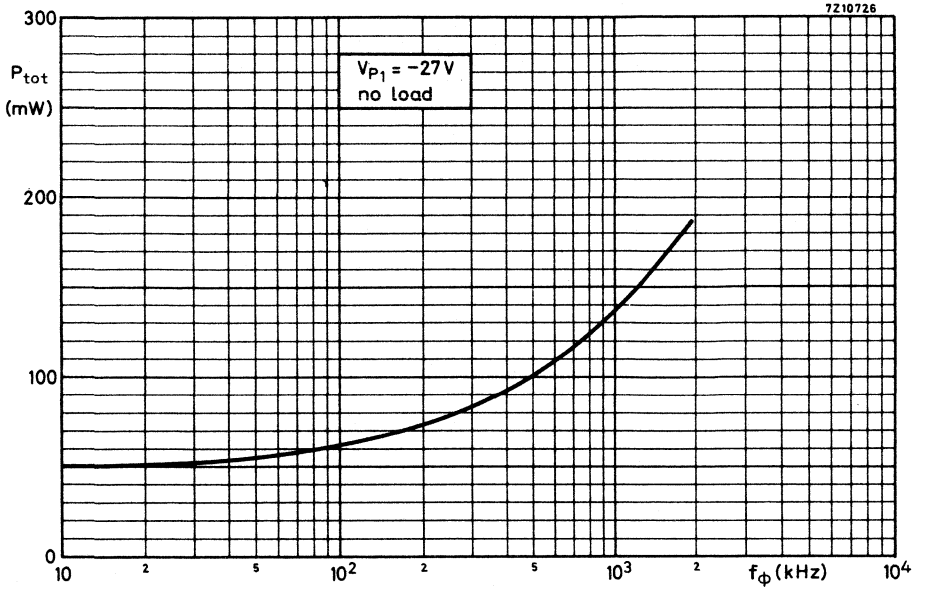


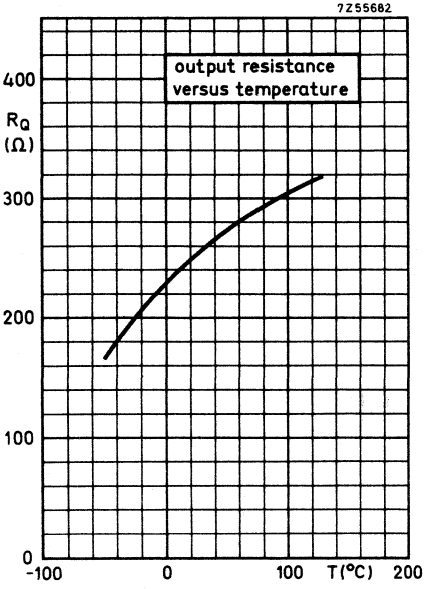
Resistors: ± 5%
$M_L \geq 423$ mV
$M_H \geq 510$ mV
Steady HIGH state dissipation ≤ 55 mW

Biasing circuit B

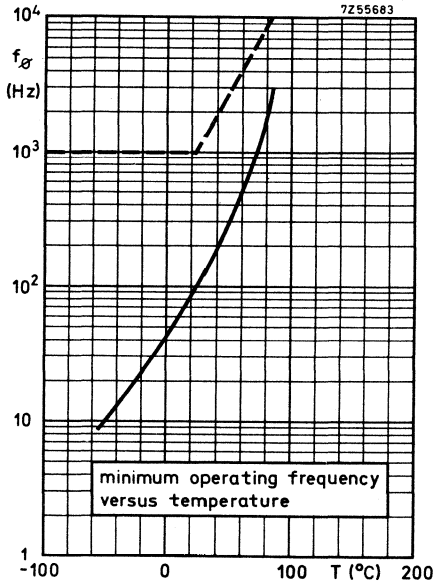
4. To drive MOS loads direct, the bias V_{P_0} should be between −12 and −14 V to P_0.

TYPICAL PERFORMANCE



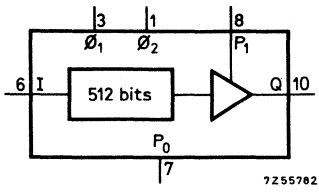


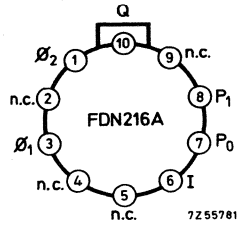
TYPICAL PERFORMANCE (continued)



The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

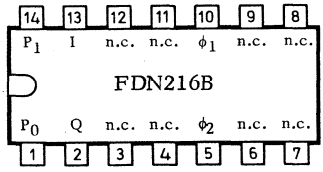
512-BIT DYNAMIC SHIFT REGISTER





top view

P_0 connected to the metal case



P_0 connected to the metal bottom

QUICK REFERENCE DATA			
Clock rate	f_ϕ	0.01 to 3	MHz
Power consumption per bit at $f\phi$ = 3 MHz	P_{av}	typ. 0.36	mW
Operating ambient temperature	T_{amb}	−55 to +85	°C
D.C. noise margin	M_H; M_L	> 1	V

PACKAGE OUTLINE:

FDN216A: TO-100 (See General Section).
FDN216B: 14 lead plastic dual in-line (Type A)(See General Section).

GENERAL DESCRIPTION

The FDN216A is a 512-bit 2-phase dynamic shift register.
The device has a low impedance push-pull output buffer.
The device offers a direct compatible pin configuration for users who have already designed their system using the FDN146A (a single 256-bit dynamic serial shift register).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage on all data inputs, clock inputs, outputs and supply terminals with reference to P_0			+0.5 to −30	V
Power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	625	mW
Junction temperature	T_j	max.	150	°C
Storage temperature	T_{stg}		−65 to +150	°C
Total current through terminal P_1	$-I_{P_1}$	max.	20	mA
Output current (per output)	$\pm I_Q$	max.	20	mA

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	200	°C/W

Note
All terminals are protected against over-voltage due to static charges.

DRIVE REQUIREMENTS at T_{amb} = −55 to +85 °C; P_0 is grounded.

	Symbol	min.	typ.	max.		Conditions and references
Clock rate	f_ϕ	0.01	–	3	MHz	
Clock pulse width	$t_{\phi 1L}$	0.125	–	5.0	µs	
	$t_{\phi 2L}$	0.125	–	5.0	µs	
Clock pulse rise time	$t_{\phi LH}$	–	–	0.5	µs	
Clock pulse fall time	$t_{\phi HL}$	–	–	0.5	µs	
Clock delay	$t_{\phi 1\phi 2}, t_{\phi 2\phi 1}$	0	–	45	µs	
Clock pulse voltage levels						
HIGH	$V_{\phi H}$	−2	0	+0.3	V	
LOW	$V_{\phi L}$	−28	−26	−24	V	
Data input logic levels						
HIGH	V_{IH}	−2	0	+0.3	V	
LOW	V_{IL}	−28	−12	−9	V	
Data lead time	$t_{\ell I}$	10	–	–	ns	
Buffer supply voltage	$-V_{P1}$	0	–	14	V	

CHARACTERISTICS

Test conditions: V_{P_1} = −12 to −14 V; T_{amb} = −55 to +85 °C; P_0 = grounded; standard load: 50 pF in parallel with 20 kΩ to P_0.

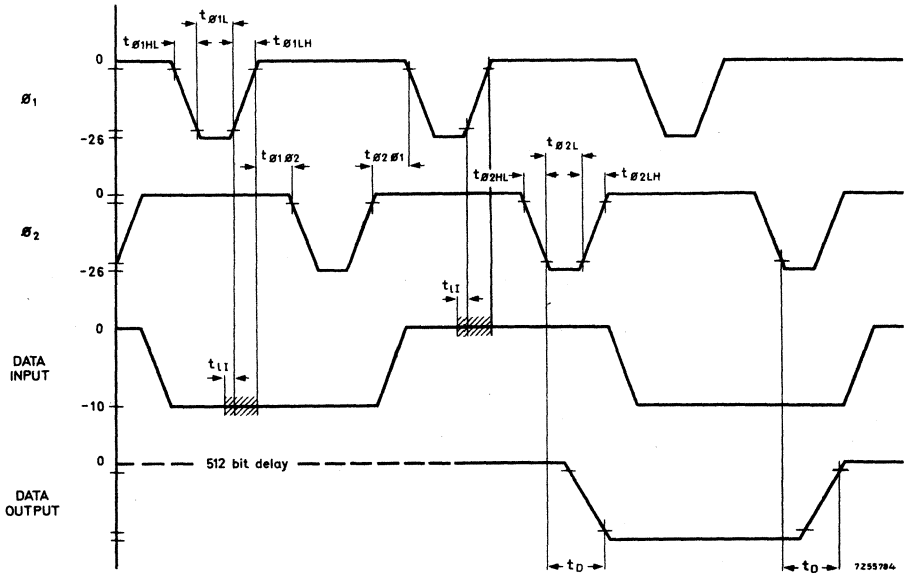
ELECTRICAL DATA	Symbol	min.	typ.	max.		Conditions and references
Output levels						
HIGH	V_{QH}	−0.5	–	0	V	
LOW	V_{QL}	−14	–	−10	V	
Data input capacitance	C_I	–	2	3.5	pF	V_I = 0 V; f = 1 MHz
Clock input capacitances	$C_{\phi 1}, C_{\phi 2}$	–	90	110	pF	V_ϕ = 0 V; f = 1 MHz
	$C_{\phi 1}, C_{\phi 2}$	–	60	80	pF	V_ϕ = −26 V; f = 1 MHz
Leakage currents						
Data input current	$-I_{IL}$	–	–	1	μA	V_I = −15 V; all other terminals at P_0; T_{amb} = 25 °C
Clock input current	$-I_{\phi L}$	–	–	100	μA	V_ϕ = −28 V; all other terminals at P_0; T_{amb} = 25 °C
Output resistance						
HIGH	R_{QH}	–	250	500	Ω	
LOW	R_{QL}	–	150	300	Ω	V_{P_1} = −5 V
Supply current	$-I_{P_1}$	–	−0.68	−1.0	mA	V_{P_1} = −13 V; f = 1 MHz; T_{amb} = 25 °C; See note
Delay time						
Clock to output	t_D	–	135	275	ns	

Note

The output buffer power supply current is almost entirely dependent on the external load. The value shown is for a load of 50 pF in parallel with 1 MΩ to P_0.

CHARACTERISTICS (continued)

TIMING DIAGRAM



Notes

1. The indicated points on the vertical axis are specified in the glossary of terms.

2. Data inputs must remain valid for the shaded interval to ensure proper entry into the register.

CHARACTERISTICS (continued)

GLOSSARY OF TERMS

1. Clock pulse width: $t_{\phi L}$
   The time for which the clock pulse is LOW: $V_{\phi L} \leq -24$ V.

2. Clock pulse fall time: $t_{\phi HL}$
   The time between the 10% and 90% voltage points as the clock pulse goes from HIGH to LOW.

3. Clock pulse rise time: $t_{\phi LH}$
   The time between the 90% and 10% voltage points as the clock pulse goes from LOW to HIGH.

4. Clock delay time: $t_{\phi 1 \phi 2}$, $t_{\phi 2 \phi 1}$
   The least allowable time between the end of the ϕ_1 (or ϕ_2) clock pulse and the start of the ϕ_2 (or ϕ_1) clock pulse, defined at −2 V.

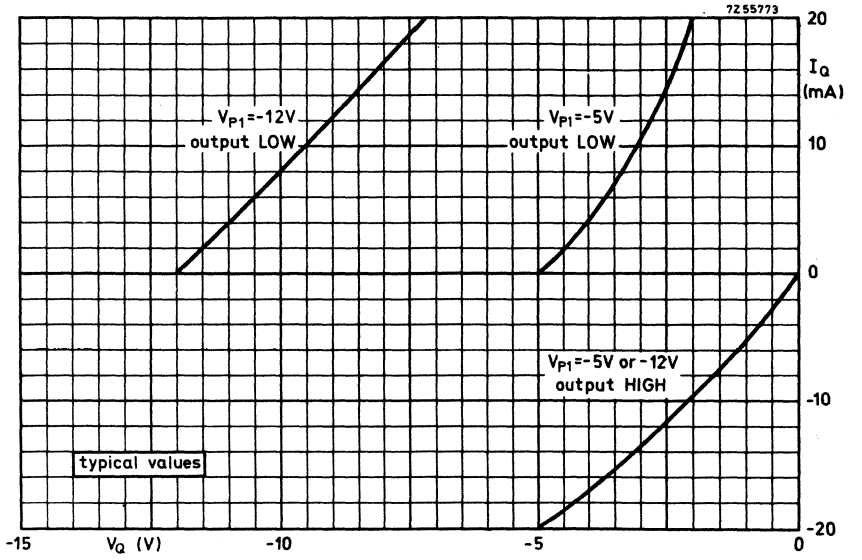
5. Data lead time: $t_{\ell I}$
   The time before the 90% point on the clock pulse ϕ_1 for which the voltage at the data input must be at its specified logic level in order to ensure that the data will be entered in the register.

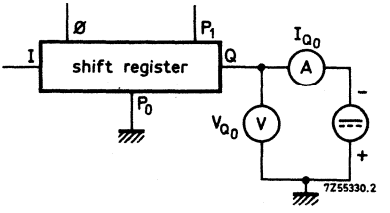
6. Delay time: t_D
   The delay between the clock pulse ϕ_2 reaching LOW and the output reaching its logic level.

OUTPUT BUFFER DESCRIPTION

1. The curves below are typical output buffer voltage-current characteristics for the FDN216A. They show V_Q versus I_Q for the bias V_{P_1} at −5 V and −12 V, for both HIGH and LOW output. The circuit shown may be used to obtain LOW output curves for other values of V_{P_1}.

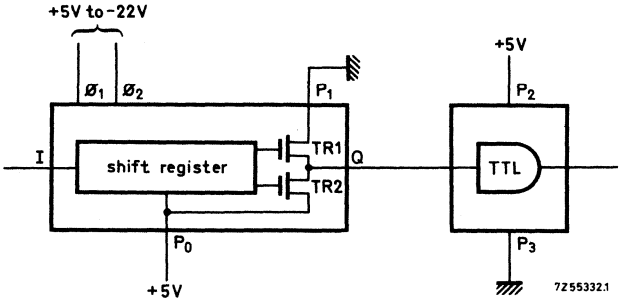
   Note: When operating with high output current levels, the maximum power rating must not be exceeded.





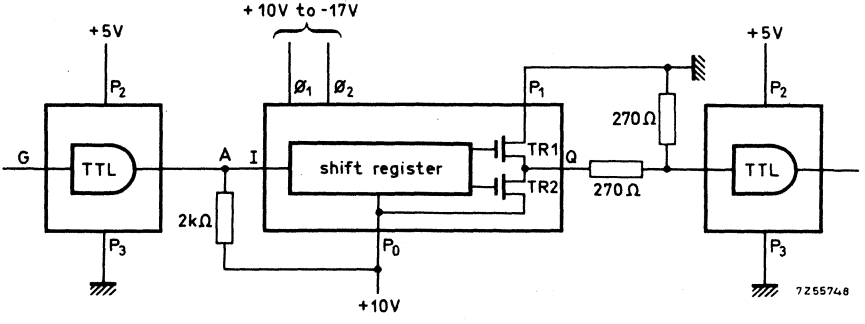
OUTPUT BUFFER DESCRIPTION (continued)

2. Biasing circuit A may be used to drive TTL or DTL loads direct. The MOS input logic levels must be referenced to V_{P0}. TR1 and TR2 are the push-pull output driver transistors of the FDN216A.



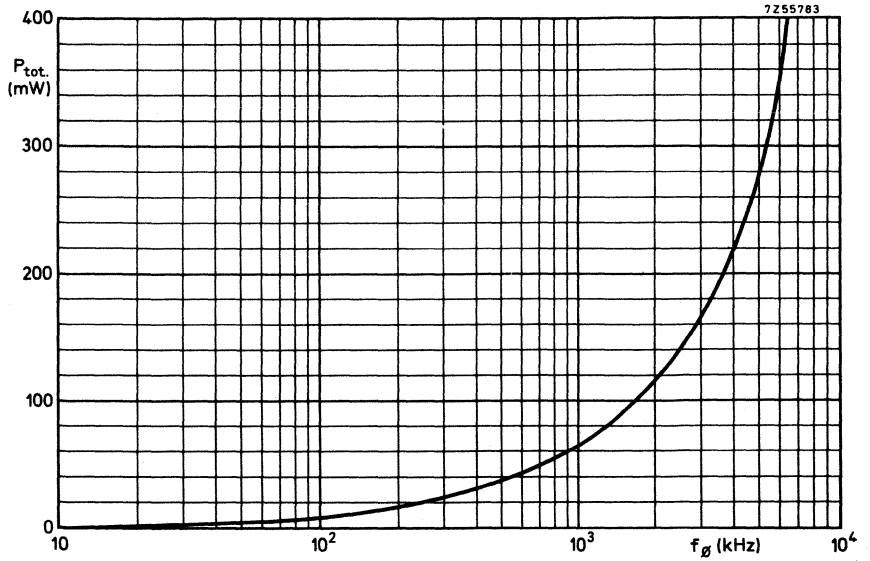
Biasing circuit A

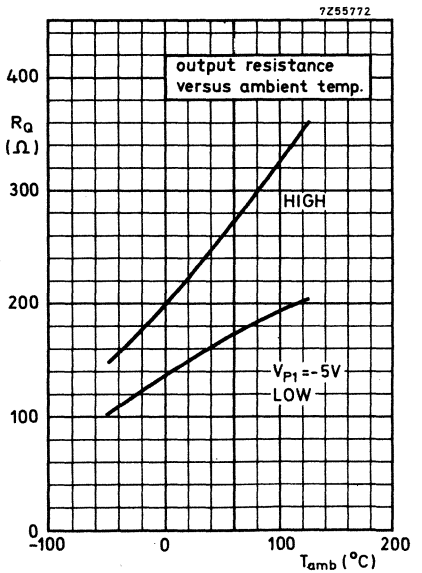
3. Biasing circuit B allows the MOS device to be interfaced with TTL or DTL at the output using only passive interface components.
Note that the TTL or DTL integrated circuit must be able to withstand +10 V applied to the output lead (point A), most circuits of our FC series and most FJ gates satisfy this requirement. Some open collector FJ gates have a minimum output breakdown voltage guarantee of 15 V.
(FJH301/7426; FJH311/7401-S1; FJH321/7405-S1)



Biasing circuit B

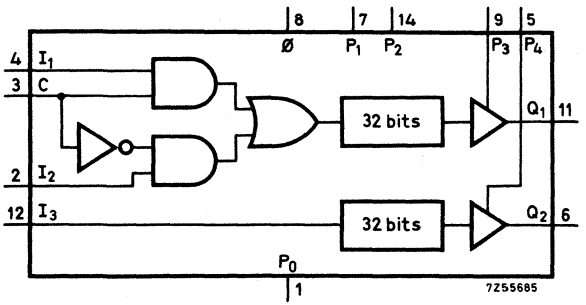
4. To drive MOS loads direct, the bias V_{P1} should be between −12 and −14 V to P_0.

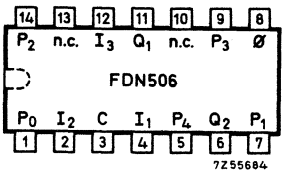

7Z55783
400
$P_{tot.}$ (mW)
300
200
100
0
10
10^2
10^3
f_ϕ (kHz)
10^4


7Z55772
output resistance versus ambient temp.
400
R_Q (Ω)
300
200
100
0
HIGH
V_{P1} = -5V
LOW
-100
0
100
200
T_{amb} (°C)

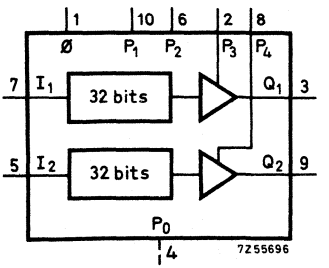
The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

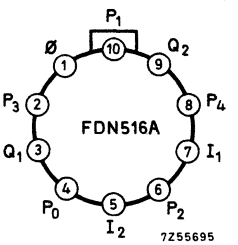
DUAL 32-BIT STATIC REGISTER





P_0 connected to the metal bottom





P_0 connected to the metal case

QUICK REFERENCE DATA			
Supply voltages	V_{P1}	−24 to −28	V
	V_{P2}	−12 to −14	V
Clock frequency	f_ϕ	0 to 1.5	MHz
Power consumption per bit at f_ϕ = 1.5 MHz	P_{av}	typ. 2	mW
Operating ambient temperature	T_{amb}	−55 to +85	°C
D.C. noise margin	M_H, M_L	> 1	V

PACKAGE OUTLINE: FND506; 14 lead ceramic dual in-line (See General Section)
FDN516A; TO-100 (See General Section)

GENERAL DESCRIPTION

The FDN506 and FDN516A are dual 32-bit static shift registers. They require a single phase, low voltage, external clock signal, and may be operated down to d.c. without loss of stored information. Both devices utilize common power and clock lines; the output buffer supplies are separated to facilitate independent biasing for MOS or TTL load drive.

The FDN506 contains the gating, external SELECT command and data inputs for selection of two independent data streams.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages on all data inputs, clock inputs, outputs and supply terminals with reference to P_0				+0.5 to −30	V
Power dissipation up to T_{amb} = 25 °C	FDN506	P_{tot}	max.	800	mW
	FDN516A	P_{tot}	max.	625	mW
Junction temperature		T_j	max.	150	°C
Storage temperature		T_{stg}		−65 to +150	°C
Total current through terminals P_3, P_4		$-I_{P3}$, $-I_{P4}$	max.	40	mA
Output current (per output)		$\pm I_Q$	max.	20	mA

THERMAL RESISTANCE

From junction to ambient	FDN506	$R_{th\ j\text{-}a}$	=	156	°C/W
	FDN516A	$R_{th\ j\text{-}a}$	=	200	°C/W

CHARACTERISTICS at $T_{amb} = -55$ to $+85$ °C

	Symbol	min.	typ.	max.	Conditions and references
Clock rate	f_ϕ	0	–	1.5 MHz	
Clock pulse width	$t_{\phi H}$	0.24	–	50 µs	See timing diagram for parameter definitions
Clock pulse fall time	$t_{\phi HL}$	–	–	0.10 µs	See note
Clock pulse rise time	$t_{\phi LH}$	–	–	1.0 µs	
Clock pulse space	$t_{\phi L}$	0.36	–	– µs	
Clock pulse voltage level					
HIGH	$V_{\phi H}$	−2	0	+0.3 V	
LOW	$V_{\phi L}$	−28	−12	−9 V	
Data/select input logic levels					
HIGH	V_{IH}, V_{CH}	−2	0	+0.3 V	
LOW	V_{IL}, V_{CL}	−28	−12	−9 V	
Data/select lead time	$t_{\ell I}, t_{\ell C}$	50	–	–	
Data/select hold time	t_{hI}, t_{hC}	100	–	–	

Note:

The fall time specified for the FDN506 and FDN516A is to ensure that output data will meet the input hold time requirements of other registers, when more shift registers are operating in series from a common clock. If a register does not drive other registers the clock fall times may be longer.

CHARACTERISTICS (continued)

Test conditions: $V_{P_1} = -24$ V to -28 V; $V_{P_2} = V_{P_3} = V_{P_4} = -12$ V to -14 V; $T_{amb} = -55$ to $+85$ °C; P_0 = grounded; standard load : 50 pF in parallel with 20 kΩ to P_0.

	Symbol	min.	typ.	max.		Conditions and references
ELECTRICAL DATA						
Output levels						
HIGH	V_{QH}	−0.5	–	0	V	
LOW	V_{QL}	−14	–	−10	V	
Data/select input capacitance	C_I, C_C	–	2	3.5	pF	bias: $V_I = V_C = 0$ V; f = 1 MHz
Clock input capacitance	C_ϕ	–	6	8	pF	bias: $V_\phi = 0$ V; f = 1 MHz
Leakage currents						
Data/select input currents	$-I_{IL}$, $-I_{CL}$	–	–	1	μA	$V_I = V_C = -15$ V; all other terminals at V_{P0}; T_{amb} = 25 °C
Clock input current	$-I_{\phi L}$	–	–	100	μA	$V_\phi = -28$ V; all other terminals at V_{P0}; T_{amb} = 25 °C
Output resistance						
HIGH	R_{QH}	–	360	600	Ω	T_{amb} = 25 °C
LOW	R_{QL}	–	220	500	Ω	$V_{P3} = V_{P4} = -5$ V; T_{amb} = 25 °C
	R_{QL}	–	330	←	Ω	$V_{P3} = V_{P4} = -10$ V; T_{amb} = 25 °C
Drive capability (See note 1)	V_{QL}	–	−10	−8	V	R_L = 4 kΩ to reference P_0
Supply current (See note 2)	V_{QL}	–	−4.7	−4.4	V	$V_{P3} = V_{P4} = -5$ V; R_L = 4 kΩ to reference P_0
	$-I_{P2}$	–	4.0	6.0	mA	$V_{P2} = -13$ V; f = 1.5 MHz; T_{amb} = 25 °C
	$-I_{P1}$	–	3.0	4.5	mA	$V_{P1} = -26$ V; f = 1.5 MHz; T_{amb} = 25 °C
Output transition times:						
fall time	t_{THL}	–	80	–	ns	
rise time	t_{TLH}	–	80	–	ns	
Delay times: fall time	t_{DHL}	–	260	–	ns	
rise time	t_{DLH}	–	260	–	ns	
D.C. noise margin	M_L	1.0	–	–	V	
	M_H	1.5	–	–	V	

Note 1

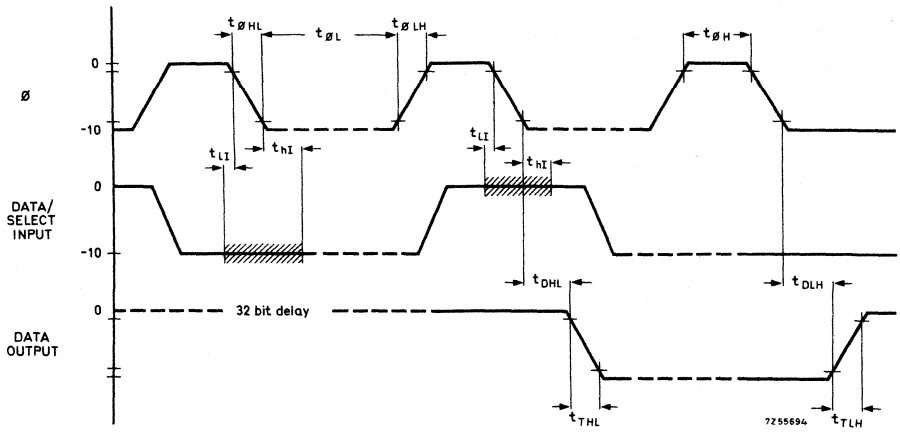
The maximum capacitive load that can be driven depends only on the speed desired and the power dissipation allowable. See the output buffer description on pages 5 and 6 for further information on output drive capability.

Note 2

The output buffer power supply current is almost entirely dependent on the external load.

CHARACTERISTICS (continued)

TIMING DIAGRAM



Notes:

1. Clock pulse ϕ is normally kept LOW.
2. The data and select inputs must remain valid for the shaded interval to ensure proper selection and entry of input data.
3. Data is kept in the register for arbitrarity long periods by keeping the clock LOW.

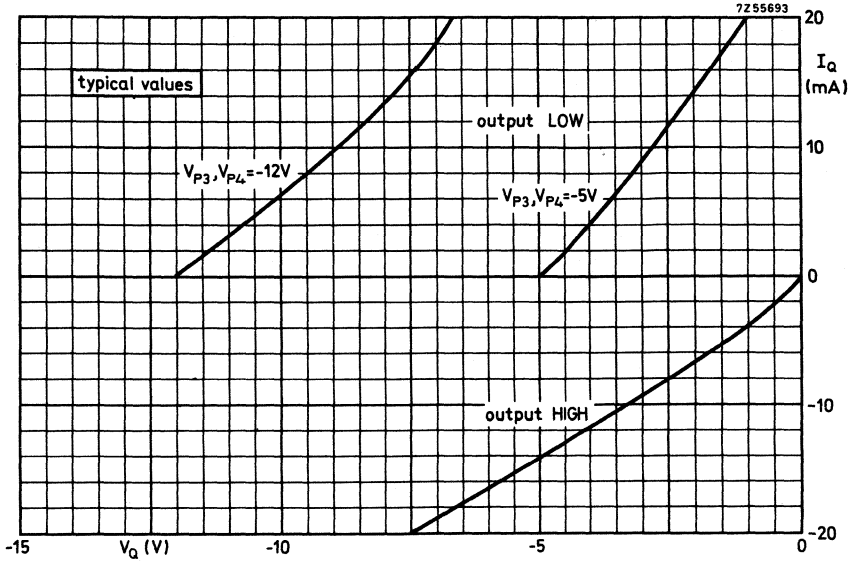
CHARACTERISTICS (continued)

GLOSSERY OF TERMS

1. Clock pulse width: $t_{\phi H}$
   The time for which the clock pulse is HIGH: $V_{\phi H} \geq -2$ V
2. Clock pulse fall time: $t_{\phi HL}$
   The time between the 10% and 90% voltage points as the clock pulse goes from HIGH to LOW.
3. Clock pulse rise time: $t_{\phi LH}$
   The time between the 90% and 10% voltage points as the clock pulse goes from LOW to HIGH.
4. Clock pulse space: $t_{\phi L}$
   The least allowable time between the end of one clock pulse (ϕ) and the start of the next, measured at -9 V.
5. Data lead time: $t_{\ell L}$
   The time before the -2 V point on the clock pulse for which the voltage at the data/select input must be at its specified logic level in order to ensure that the data will be entered in the register.
6. Data hold time: t_{hI}
   The time after the clock pulse ϕ reaches LOW(-9 V) for which the data/select inputs must remain stable in order to ensure that the data will be entered in the register.
7. Output fall transition time: t_{THL}
   The time between the 10% and 90% voltage points as the output goes from HIGH to LOW.
8. Output rise transition time: t_{TLH}
   The time between the 90% and 10% voltage points as the output goes from LOW to HIGH.
9. Fall delay time: t_{DHL}
   The delay between the clock pulse ϕ reaching LOW and the output beginning to change from HIGH to LOW.
10. Rise delay time: t_{DLH}
    The delay between the clock pulse ϕ reaching LOW and the output beginning to change from LOW to HIGH.

OUTPUT BUFFER DESCRIPTION

1. The curves below are typical output buffer voltage-current characteristics for the FDN506 and FDN516A.
   The output buffer supply voltages may be varied between 0 and −14 V according to the output voltage swing required. It does not affect the operating speed of the register.

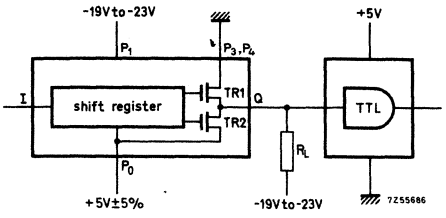


Note

When operating with high output current levels, the maximum power rating must not be exceeded.

OUTPUT BUFFER DESCRIPTION (continued)

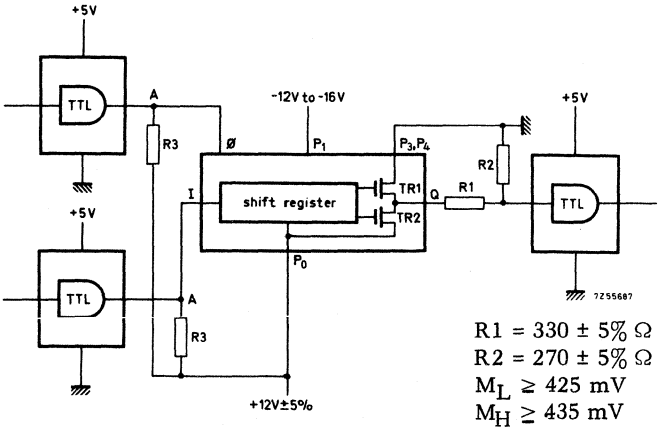
2. Biasing circuit A may be used to drive TTL or DTL loads direct. The MOS input logic levels must be referenced to V_{P0}. TR1 and TR2 are the push-pull output driver transistors of the FDN506 and FDN516A.



R_L = 22 ± 5% kΩ
$M_L \geq$ 450 mV
$M_H \geq$ 1.5 V
Steady HIGH state dissipation < 1 mW

Biasing circuit A

3. Biasing circuit B allows the MOS device to be interfaced with TTL or DTL at both input and output using only passive interface components. Note that the TTL or DTL integrated circuit must be able to withstand +12 V applied to the output lead (point A), most circuits of our FC series (non-R_C types) satisfy this requirement. The open collector FJ gates FJH301, FJH311 and FJH321 have a minimum output breakdown voltage guarantee of 15 V.



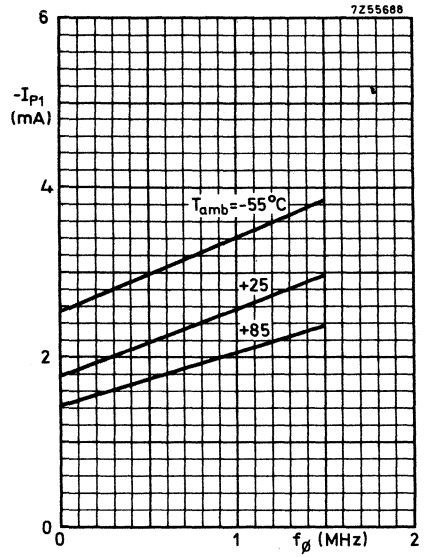
R1 = 330 ± 5% Ω
R2 = 270 ± 5% Ω
$M_L \geq$ 425 mV
$M_H \geq$ 435 mV
Steady HIGH state dissipation ≤ 63 mW

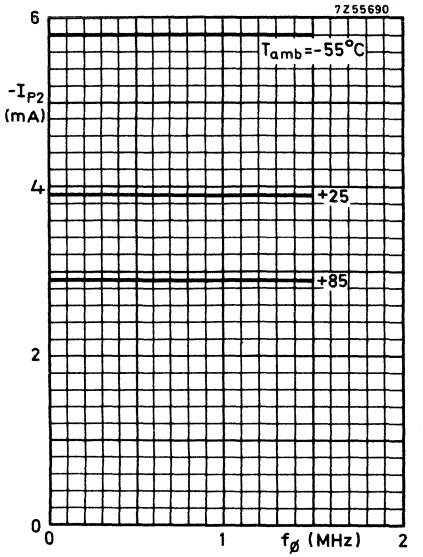
Biasing circuit B

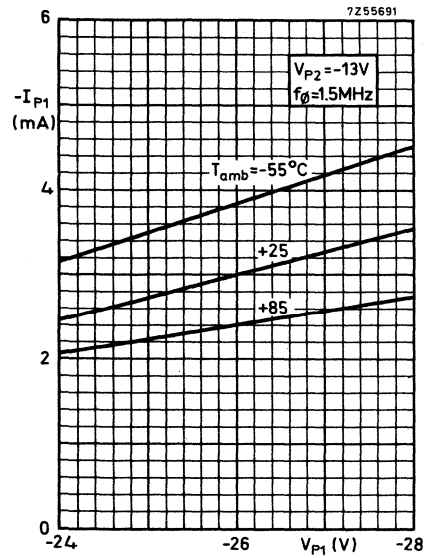
4. To drive MOS loads direct, the bias V_{P3} and V_{P4} should be between −12 and −14 V to P_0.

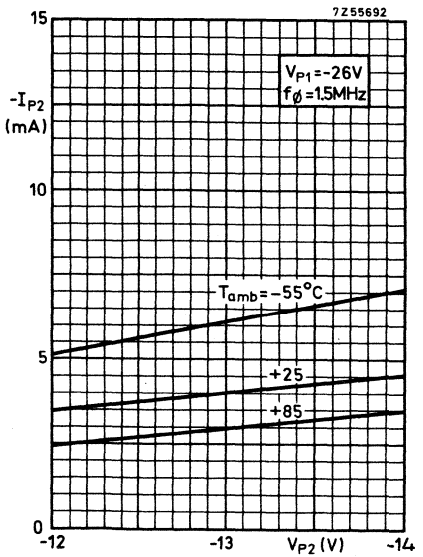
TYPICAL PERFORMANCE at P_0 = grounded; standard load : 50 pF in parallel with 20 kΩ to P_0.

Test condition: $V_{P1} = -26$ V; $V_{P2} = -13$ V



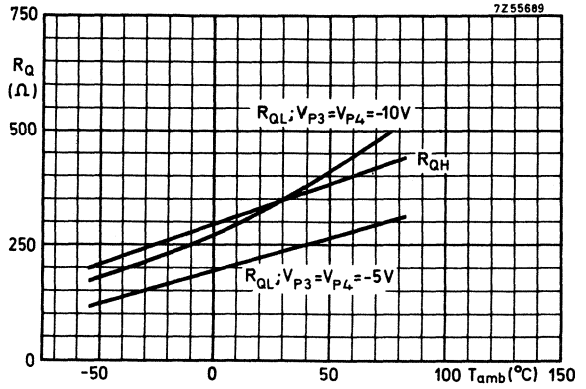






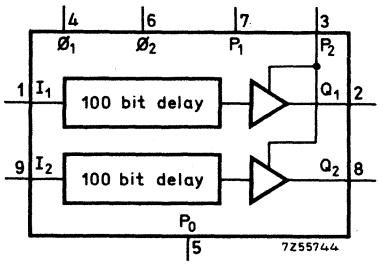
TYPICAL PERFORMANCE (continued)

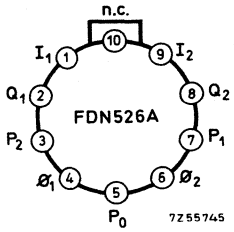
Test conditions: P_0 = grounded; $V_{P1} = -26$ V; $V_{P2} = -13$ V



The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

DUAL 100-BIT STATIC SHIFT REGISTER





P_0 connected to metal case

QUICK REFERENCE DATA			
Clock rate	f_ϕ	0 to 3	MHz
Supply voltage	V_{P_1}	−24 to −28	V
Power consumption per bit at f_ϕ = 3 MHz	P_{av}	typ. 2	mW
Operating ambient temperature	T_{amb}	−55 to +85	°C
D.C. noise margin	M_H, M_L	> 1	V

PACKAGE OUTLINE: TO-100 (See General Section)

GENERAL DESCRIPTION

The FDN526A is a monolithic dual 100-bit shift register. The two shift registers have each one serial input and output. They operate from common clocks and supply lines. The device has low impedance push-pull output buffers, which, when appropriately biased, are capable of interfacing direct with MOS, TTL, DTL and other loads. The buffer supply terminal P_2 is a separate supply which determines the output LOW signal only. This provides an output level that is independent of supply voltage V_{P_1}, the amplitude and width of the clock pulses.
All inputs, outputs, supply terminals and clock inputs are protected against static voltages.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage on all data inputs, clock inputs, outputs and supply terminals with reference to P_0		+0.5 to −30		V
Power dissipation up to $T_{amb} = 25\ ^oC$	P_{tot}	max.	625	mW
Junction temperature	T_j	max.	150	^oC
Storage temperature	T_{stg}	−65 to +150		^oC
Total current through terminal P_2	$-I_{P_2}$	max.	40	mA
Output current (pér output)	$\pm I_Q$	max.	20	mA

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$	=	200	$^oC/W$

DRIVE REQUIREMENTS at T_{amb} = −55 to +85 °C; P_0 = grounded

	Symbol	min.	typ.	max.		Conditions and references
Clock rate	f_ϕ	0	–	2	MHz	V_{P1}, $V_{\phi L}$=−24 V
		0	–	3	MHz	V_{P1}, $V_{\phi L}$=−26 V
Clock pulse width [1])	$t_{\phi 1L}$	0.2	–	10	µs	V_{P1}, $V_{\phi L}$=−24 V
		0.1	–	10	µs	V_{P1}, $V_{\phi L}$=−26 V
	$t_{\phi 2L}$	0.2	–	–	µs	V_{P1}, $V_{\phi L}$=−24 V
		0.15	–	–	µs	V_{P1}, $V_{\phi L}$=−26 V
Clock pulse space	$t_{\phi 2H}$	–	–	30	µs	
Clock pulse rise time	$t_{\phi LH}$	–	–	0.5	µs	
Clock pulse fall time	$t_{\phi HL}$	–	–	0.5	µs	
Clock delay	$t_{\phi 1\phi 2}$, $t_{\phi 2\phi 1}$	0	–	10	µs	
Clock pulse voltage levels						
HIGH	$V_{\phi H}$	−2	–	+0.3	V	
LOW	$V_{\phi L}$	−28	−26	−24	V	
Data input logic levels						
HIGH	V_{IH}	−2.0	0	+0.3	V	
LOW	V_{IL}	−28	−12	−9	V	
Data lead time	$t_{\ell I}$	20	–	–	ns	

[1]) See timing diagram on page 5.

CHARACTERISTICS

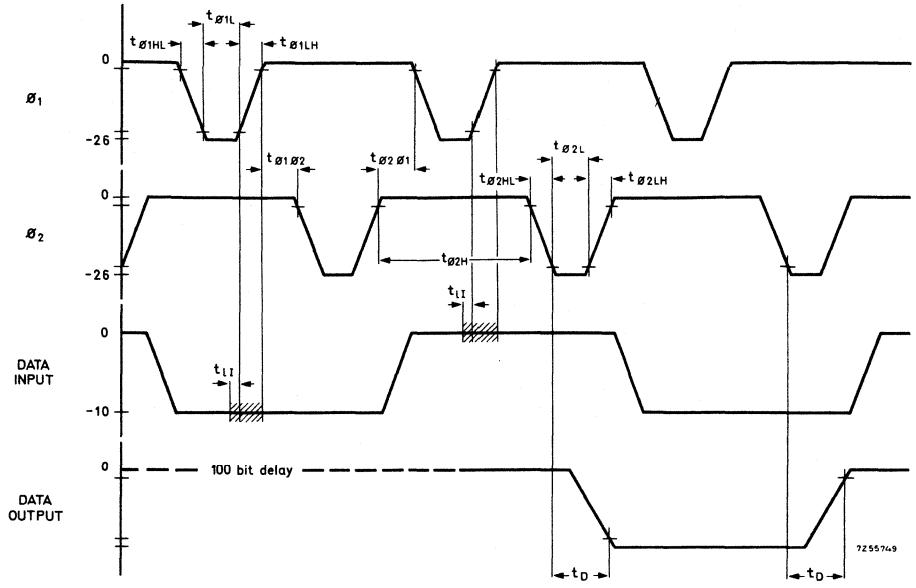
Test conditions: V_{P1} = −24 to −28 V; V_{P2} = −12 to −14 V; T_{amb} = −55 to +85 °C; P_0 = grounded; standard load: 25 pF in parallel with 20 kΩ to P_0.

	Symbol	min.	typ.[1])	max.		Conditions and references
Output levels						
HIGH	V_{QH}	−1	–	0	V	
LOW	V_{QL}	−14	–	−10	V	
Data input capacitance	C_I	–	2	3.5	pF	V_I = 0 V; f = 1 MHz
Clock input capacitances	$C_{\phi 1}, C_{\phi 2}$	–	17	25	pF	V_ϕ = 0 V; f = 1 MHz
	$C_{\phi 1}, C_{\phi 2}$	–	15	22	pF	V_ϕ = −26 V; f = 1 MHz
Leakage currents						
Data input current	$-I_{IL}$	–	–	1	μA	V_I = −15 V; T_{amb} = 25 °C; all other terminals at V_{P0}
Clock input current	$-I_{\phi L}$	–	–	100	μA	V_ϕ = −28 V; T_{amb} = 25 °C; all other terminals at V_{P0}
Output resistance						
HIGH	R_{QH}	–	400	750	Ω	V_Q = −1 V
Drive capability	V_{QL}	–	−11.3	−8	V	R_L = 4 kΩ to P_0; V_{P2} = −5 V
Supply currents	$-I_{P1}$	–	1.1	1.8	mA	V_{P1} = −26 V; f = 1 MHz; T_{amb} = 25 °C; R_L = 1 MHz
	$-I_{P2}$	–	9.3	18	mA	V_{P2} = −13 V; f = 1.5 MHz; T_{amb} = 25 °C; R_L = 1 MHz
Delay times						
Clock to output	t_D	–	150	275	ns	
D.C. noise margin	M_H, M_L	1	–	–	V	

[1]) Typical values measured at: V_{P1} = −26 V; V_{P2} = −13 V; $V_{\phi L}$ = −26 V; T_{amb} = 25 °C.

CHARACTERISTICS (continued)

TIMING DIAGRAM



Notes

1. Data inputs must remain valid for the shaded interval to ensure proper entry into the register.
2. For d.c. operation $\phi 2$ should be kept LOW.

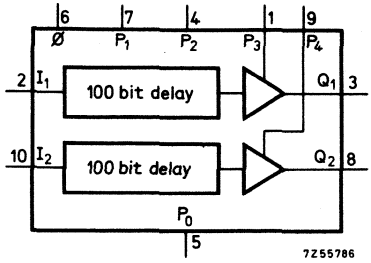
CHARACTERISTICS (continued)

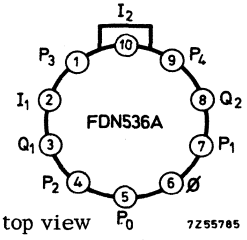
GLOSSARY OF TERMS

1. Clock pulse width: $t_{\phi L}$
   The time for which the clock pulse is LOW: $V_{\phi L} = -26$ V
2. Clock pulse space: $t_{\phi 2H}$
   The time for which the clock pulse $\phi 2$ is HIGH ($V_{\phi} > -2$ V).
3. Clock pulse fall time: $t_{\phi HL}$
   The time between the 10% and 90% voltage points as the clock pulse goes from HIGH to LOW.
4. Clock pulse rise time: $t_{\phi LH}$
   The time between the 90% and 10% voltage points as the clock pulse goes from LOW to HIGH.
5. Clock delay time: $t_{\phi 1 \phi 2}$, $t_{\phi 2 \phi 1}$
   The least allowable time between the end of the ϕ_1 (or $\phi 2$) clock pulse and the start of the $\phi 2$ (or ϕ_1) clock pulse, defined at -2 V.
6. Data lead time: $t_{\ell I}$
   The time before the 90% point on the clock pulse for which the voltage at the data input must be at its specified logic level in order to ensure that the data will be entered in the register.
7. Delay time: t_D
   The delay between the clock pulse reaching LOW and the output reaching its logic level.

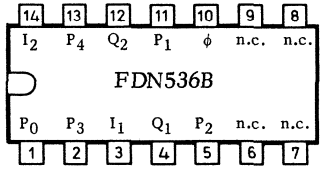
The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

DUAL 100-BIT STATIC SHIFT REGISTER





P_0 connected to the metal case



P_0 connected to metal bottom

QUICK REFERENCE DATA			
Clock rate	$f\phi$	0 to 1.5	MHz
Supply voltages	V_{P1}	−24 to −28	V
	$V_{P2}; V_{P3}; V_{P4}$	−12 to −14	V
Power consumption per bit at $f\phi$ = 1.5 MHz	P_{av}	typ. 1	mW
Operating ambient temperature	T_{amb}	−55 to +85	°C
D.C. noise margin	M_H, M_L	> 1	V

PACKAGE OUTLINE:

FDN536A: TO-100 (See General Section).
FDN536B: 14 lead plastic dual in-line (Type A)(See General Section).

GENERAL DESCRIPTION

The FDN536A is a monolithic dual 100-bit shift register. The two shift registers have each one serial input and output. They operate from common clocks and supply lines. The device has low impedance push-pull output buffers, which, when appropriately biased, are capable of interfacing direct with MOS, TTL, DTL and other loads.
The buffer supply terminals P_3 and P_4 are separate supplies which determine the output LOW signals only. This provides an output level that is independent of supply voltages V_{P_1}, V_{P_2}, the amplitude and width of the clock pulses.
All inputs, outputs, supply terminals and clock inputs are protected against static voltages.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage on all data inputs, clock inputs, outputs and supply terminals with reference ro P_0		+0.5 to	−30	V
Power dissipation up to $T_{amb} = 25\ ^oC$	P_{tot}	max.	625	mW
Junction temperature	T_j	max.	150	^oC
Storage temperature	T_{stg}	−65 to	+150	^oC
Total current through terminals P_2, P_3 and P_4	$-I_{P_2}; -I_{P_3}; -I_{P_4}$	max.	40	mA
Output current (per output)	$\pm I_Q$	max.	20	mA

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$	=	200	$^oC/W$

DRIVE REQUIREMENTS at $T_{amb} = -55$ to $+85\ ^{o}C$; voltages in reference to P_0

	Symbol	min.	typ.	max.	
Clock rate	$f\phi$	0	–	1.5	MHz
Clock pulse width [1])	$t\phi L$	0.36	–	–	µs
Clock pulse spacing	$t\phi H$	0.24	–	10	µs
Clock pulse rise time	$t\phi LH$	–	–	0.5	µs
Clock pulse fall time [2])	$t\phi HL$	–	–	0.1	µs
Clock delay	$t\phi 1\phi 2, t\phi 2\phi 1$	0	–	–	µs
Clock pulse voltage levels					
HIGH	$V_{\phi H}$	−2	–	+0.3	V
LOW	$V_{\phi L}$	−28	−12	−10	V
Data input logic levels					
HIGH	V_{IH}	−2.0	0	+0.3	V
LOW	V_{IL}	−28	−12	−9	V
Data lead time	$t_{\ell I}$	20	–	–	ns
Data hold time	t_{hI}	100	–	–	ns

1) See timing diagram on page 5.

2) The fall time specified for the FDN536A is to ensure that output data will meet the input hold time requirements of other shift registers, when more shift registers operate in series from a common clock. If a register does not drive other registers the clock pulse fall time may be longer.

CHARACTERISTICS

Test conditions: V_{P_1} = −24 to −28 V; V_{P_2} = V_{P_3} = V_{P_4} = −12 to −14 V; T_{amb} = −55 to +85 °C; P_0 = grounded; standard load: 25 pF in parallel with 20 kΩ to P_0.

	Symbol	min.	typ.[1]	max.		Conditions and references
Output levels						
HIGH	V_{QH}	−1	–	0	V	
LOW	V_{QL}	−14	–	−10	V	
Data input capacitance	C_I	–	2	3.5	pF	V_I = 0 V; f = 1 MHz
Clock input capacitances	C_ϕ	–	4	8	pF	V_ϕ = 0 V; f = 1 MHz
Leakage currents						
Data input current	$-I_{IL}$	–	–	1	μA	V_I = −15 V; T_{amb} = 25 °C; all other terminals at V_{P0}
Clock input current	$-I_{\phi L}$	–	–	1	μA	V_ϕ = −28 V; T_{amb} = 25 °C; all other terminals at V_{P0}
Output resistance						
HIGH	R_{QH}	–	400	750	Ω	
Drive capability (see note)	V_{QL}	–	−11.3	−8	V	R_L = 4 kΩ to P_0; V_{P_2} = V_{P_3} = V_{P_4}
	V_{QL}	–	−4.3	−4.6	V	R_L = 4 kΩ to P_0; V_{P_3} = V_{P_4} = −5 V
Supply currents	$-I_{P_1}$	–	2.8	5.5	mA	f = 1 MHz; T_{amb} = 25 °C; $t_{\phi L}$ = 660 ns
	$-I_{P_2}$	–	8.4	18	mA	
	$-I_{P_3}$, $-I_{P_4}$	–	–	–		depends on external load
Delay times						
Clock to output	t_{DHL}, t_{DLH}	–	230	550	ns	
D.C. noise margin	M_H, M_L	1	–	–	V	

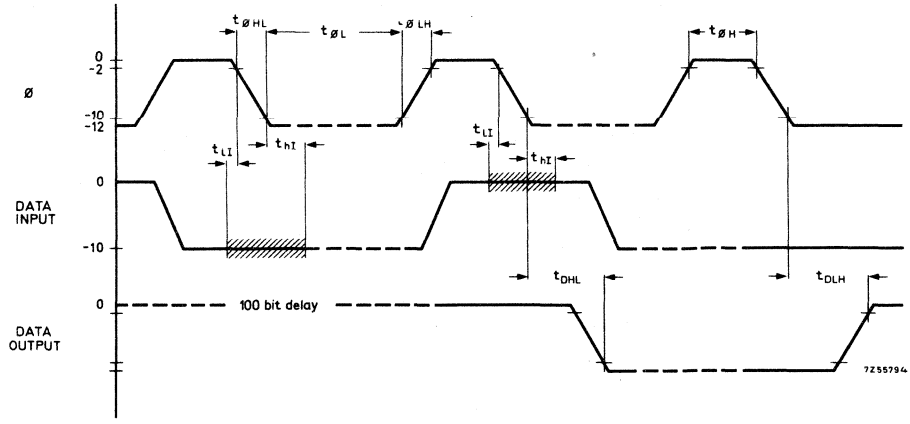
Note

The maximum capacitive load that can be driven depends only on the speed desired and the power dissipation allowable. See the output buffer description on pages 7 and 8 for further information on output drive capability.

[1] Typical values measured at: V_{P_1} = −26 V; V_{P_2} = −13 V; $V_{\phi L}$ = −26 V; T_{amb} = 25 °C.

CHARACTERISTICS (continued)

TIMING DIAGRAM



Notes

1. Data inputs must remain valid for the shaded interval to ensure proper entry into the register.
2. Data is kept in the register for arbitrarity long periods by keeping the clock LOW.
3. Data is transferred into the register at the falling edge of the clock pulse ($t_{\phi HL}$)
4. Output data appears at a time t_{DHL} or t_{DLH} after the falling edge ($t_{\phi HL}$) of the clock pulse.

CHARACTERISTICS (continued)

GLOSSARY OF TERMS

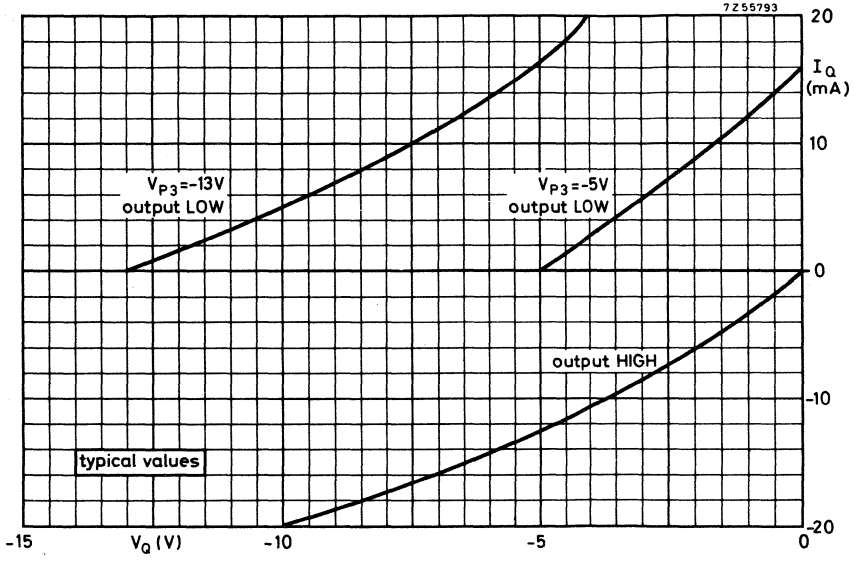
1. Clock pulse width: $t_{\phi L}$
   The time for which the clock pulse is LOW: $V_{\phi L} \leq -24$ V
2. Clock pulse space: $t_{\phi H}$
   The delay between the end of one clock pulse and the initiation of the next.
3. Clock pulse fall time: $t_{\phi HL}$
   The time between the 10% and 90% voltage points as the clock pulse goes from HIGH to LOW.
4. Clock pulse rise time: $t_{\phi LH}$
   The time between the 90% and 10% voltage points as the clock pulse goes from LOW to HIGH.
5. Clock to data output delay: t_{DHL}, t_{DLH}
   The delay between the 90% point on the clock pulse and the 90% point on the new logic state of the output.
6. Data lead time: $t_{\ell I}$
   The time before the start of the HIGH to LOW transition of the clock pulse for which the voltage at the data input must be at its specified logic level in order to ensure that the data will be entered in the register.
7. Data hold time: t_{hI}
   The time after the clock pulse ϕ reaches LOW for which the input data must remain stable to guarantee that it will be entered in the register. This delay is caused by the internal 2-phase clock generator.

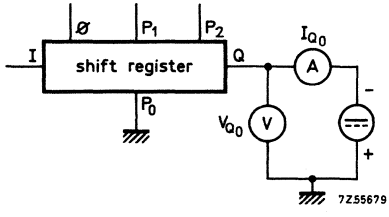
OUTPUT BUFFER DESCRIPTION

1. The curves below are typical output buffer voltage-current characteristics for the FDN536A.

   The circuit shown may be used to obtain LOW output curves for other values of V_{P2}.

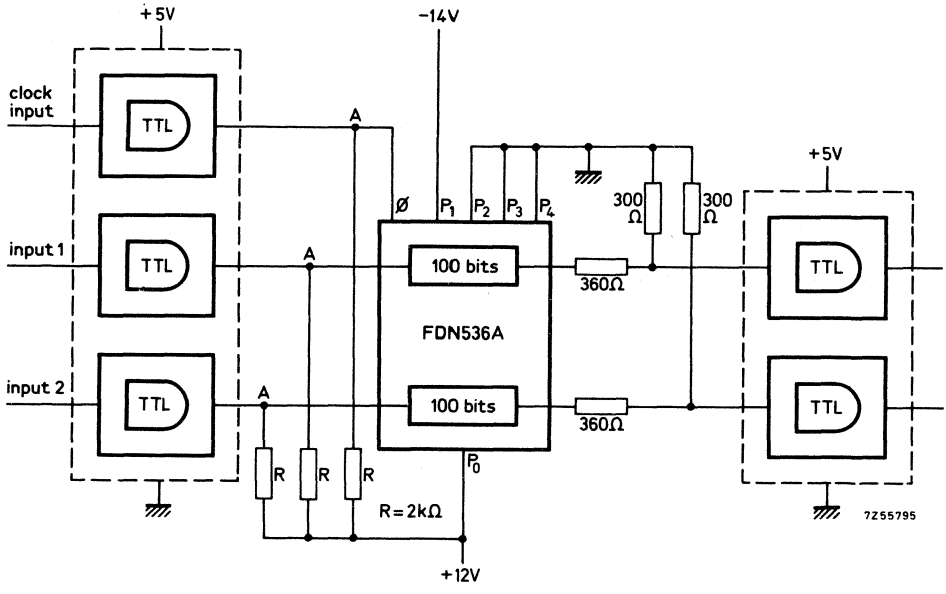
   Note: When operating with high output current levels, the maximum power rating must not be exceeded;

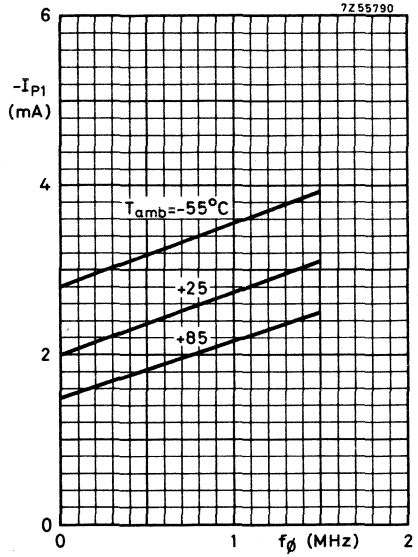


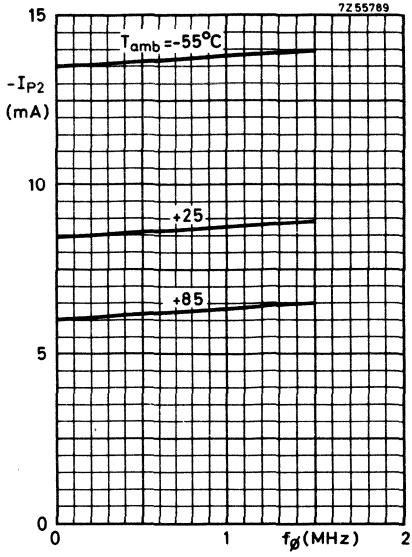


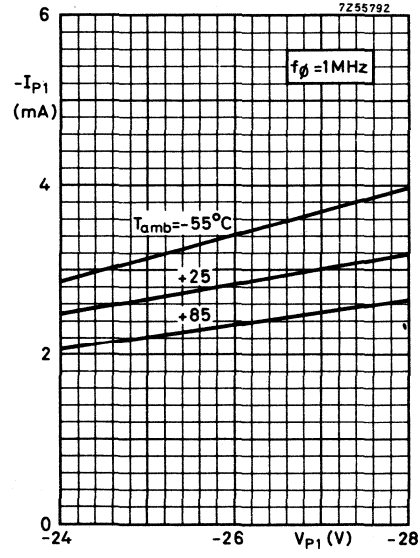
OUTPUT BUFFER DESCRIPTION (continued)

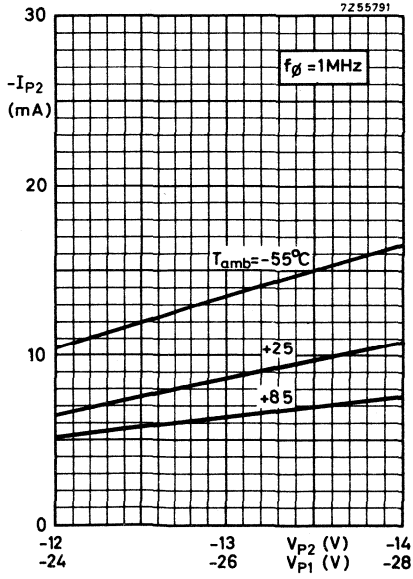
2. The biasing circuit below allows the MOS device to be interfaced with TTL or DTL at both the inputs, outputs and clock using only passive interface components. Note that the TTL or DTL integrated circuit must be able to withstand +12 V applied to the output lead (point A); most non-R_C type circuits of our FC series and most FJ gates satisfy this requirement. Same open collector FJ gates have a minimum output breakdown voltage guarantee of 15 V.
(FJH301/7426; FJH311/7401-S1; FJH321/7405-S1).

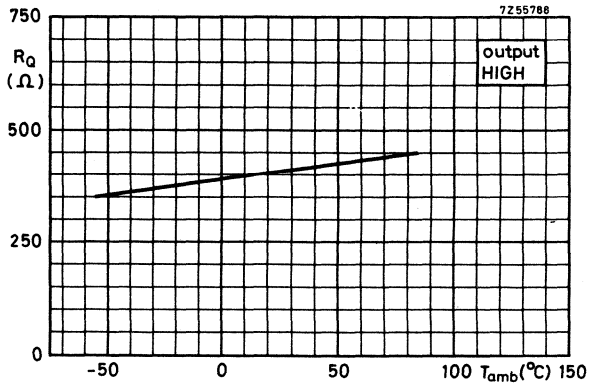


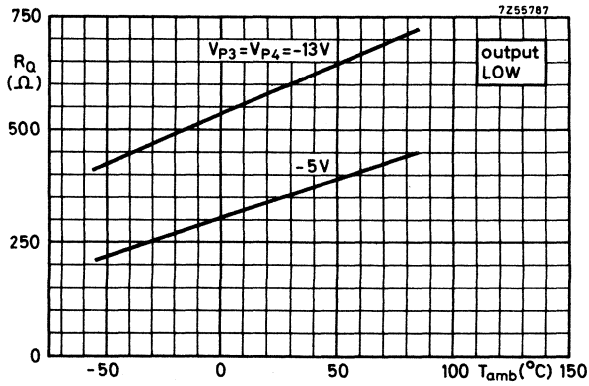

7Z55790
6
4
2
0
-IP1
(mA)
Tamb=-55°C
+25
+85
0
1
fø (MHz)
2


7Z55789
15
10
5
0
-IP2
(mA)
Tamb=-55°C
+25
+85
0
1
fø(MHz)
2


7Z55792
6
4
2
0
-IP1
(mA)
fø =1MHz
Tamb=-55°C
+25
+85
-24
-26
VP1 (V)
-28

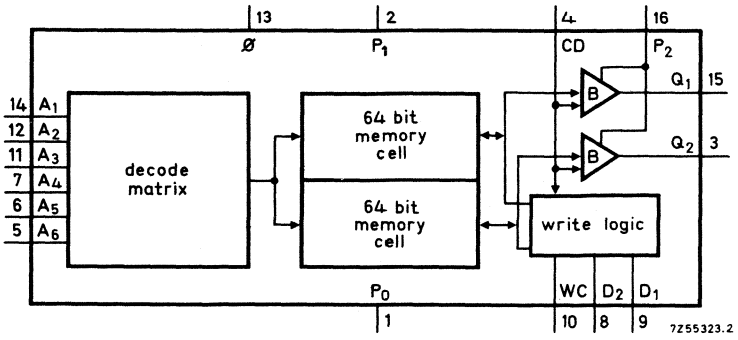

7Z55791
30
20
10
0
-IP2
(mA)
fø =1MHz
Tamb=-55°C
+25
+85
-12
-24
-13
-26
VP2 (V)
VP1 (V)
-14
-28


7Z55788
750
R_Q (Ω)
500
250
0
output HIGH
-50
0
50
100
T_{amb}(°C)
150

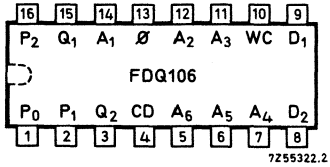

7Z55787
750
R_Q (Ω)
500
250
0
$V_{P3}=V_{P4}=-13V$
-5V
output LOW
-50
0
50
100
T_{amb}(°C)
150

The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

READ/WRITE RANDOM ACCESS MEMORY, 128-BIT, 64 WORD, 2 BITS PER WORD



WC = write control; CD = chip disable



P0 and metal package bottom are connected

QUICK REFERENCE DATA				
Supply voltage	V_{P_1}	−26 to −28		V
Standby power per bit (required clock power)		typ.	3	μW
Total power consumption at 1 MHz read-rate	P_{tot}	typ.	135	mW
Read access time	t_{AR}	<	1	μs
D.C. noise margin	M_L, M_H	>	1	V
Data read rate	f_{DR}	<	1	MHz
Data write rate	f_{DW}	<	1	MHz
Operating ambient temperature	T_{amb}	−55 to +85		°C

PACKAGE OUTLINE: 16 lead metal-ceramic dual in-line (See general section)

GENERAL DESCRIPTION

The FDQ106 is a monolithic, 128 bit random access read/write memory. It is organized as two 64 bit memories with 6 common single-rail address inputs and two separate outputs; it is used as a 64 word, 2-bits per word memory. It requires a single-phase clock strobe pulse to refresh the data stored in all the memory cells simultaneously and to change the data stored in a cell in the write mode.
It also incorporates a chip disable that inhibits both data inputs and output buffers for expanded memory applications. The memory is activated in the write mode by applying a write control pulse; at all other times it is in the read mode.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage on all data inputs, clock inputs, outputs and supply terminals, with reference to P_0		+0.5 to −30		V
Power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	800	mW
Junction temperature	T_j	max.	150	°C
Storage temperature	T_{stg}	−65 to +150		°C
Total current through terminal P_2	$-I_{P_2}$	max.	40	mA
Output current (per output)	$\pm I_Q$	max.	20	mA

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$	=	156	°C/W

CHARACTERISTICS at T_{amb} = −55 to +85 °C

	Symbol	min.	typ.	max.	Conditions and references
Data read rate	f_{DR}	–	–	1 MHz	
Data write rate	f_{DW}	–	–	1 MHz	
Strobe rate	f_{ϕ}	0.01	–	1 MHz	
Strobe pulse width	$t_{\phi H}$	0.08	–	5 μs	see timing diagram for parameter definitions
Write control pulse width	t_{WL}	0.5	–	10 μs	
Write control and strobe pulse rise time:	t_{WLH}	–	–	0.1 μs	
	$t_{\phi LH}$	–	–	0.1 μs	
fall time:	t_{WHL}	–	–	0.1 μs	
	$t_{\phi HL}$	–	–	0.1 μs	
Write control and strobe pulse voltage levels:					
HIGH	V_{WH}; $V_{\phi H}$	−2	0	+0.3 V	
LOW	V_{WH}; $V_{\phi L}$	−28	−27	−26 V	
Address, data, and chip disable input logic levels:					
HIGH	V_{AH}, V_{DH}, V_{CDH}	−2	0	+0.3 V	
LOW	V_{AL}, V_{DL}, V_{CDL}	−28	−12	−9 V	
Write address lead time	$t_{\ell WA}$	0.35	–	– μs	
Strobe address lead time	$t_{\ell \phi A}$	0.76	–	– μs	
Strobe write lead time	$t_{\ell W \phi HL}$	0.40	–	– μs	

CHARACTERISTICS (continued)

Test conditions: V_{P_1} = −26 V to −28 V; V_{P_2} = −12 V to −14 V; T_{amb} = −55 to +85 °C; P_0 = grounded; standard load: 50 pF in parallel with 50 kΩ to P_0.

	Symbol	min.	typ.	max.	Conditions and references
ELECTRICAL DATA					
Read access time	t_{AR}		0.2	0.5 1.0 µs	
Data output logic levels					
HIGH	V_{QH}	−1.0	−	0 V	
LOW	V_{QL}	−14	−	−10 V	
Address and data input capacitance	C_A, C_D	−	4.5	6.0 pF	bias: V_A; V_D = 0 V; f_ϕ = 1 MHz
Chip disable input capacitance	C_{CD}	−	7.0	9.0 pF	bias: V_{CD} = 0 V; f_ϕ = 1 MHz
Strobe input capacitance	C_ϕ	−	56	68 pF	bias: V_ϕ = 0 V; f_ϕ = 1 MHz
	C_ϕ	−	28	35 pF	bias: V_ϕ = −26 V; f_ϕ = 1 MHz
Write control input capacitance	C_W	−	7.9	9.2 pF	bias: V_{WC} = 0 V; f_ϕ = 1 MHz
	C_W	−	5.8	7.0 pF	bias: V_{WC} = −26 V; f_ϕ = 1 MHz
Data output capacitance	C_Q	−	3.5	4.5 pF	bias: V_Q = 0 V; f_ϕ = 1 MHz
Leakage currents:					
Address, data, chip disable input currents	$-I_{AL}$, $-I_{DL}$, $-I_{CDL}$	−	−	1 µA	bias: V_A; V_D; V_{CD} = −15 V; see note 2
Strobe and write control input currents	$-I_{\phi L}$, $-I_{WL}$	−	−	100 µA	bias: V_ϕ; V_{WC} = −28 V; all see note 2
Output leakage current	$-I_Q$	−	−	10 µA	V_Q = 10 V; CD = LOW; T_{amb} = 25 °C
Output resistances:					
HIGH	R_{QH}	−	250	600 Ω	
LOW	R_{QL}	−	250	600 Ω	V_{P_2} = −5 V
Power supply current drain: at V_{P_1}	$-I_{P_1}$	−	4.5	7.5 mA	V_{P_1} = −28 V; f_ϕ = 1 MHz; T_{amb} = 25 °C
at V_{P_2} (see note 1)	$-I_{P_2}$	−	0.8	1.0 mA	V_{P_2} = −13 V; f_ϕ = 1 MHz; T_{amb} = 25 °C
Output transition times:					
fall time	t_{THL}	−	100	− ns	
rise time	t_{TLH}	−	100	− ns	
D.C. noise margin	M_L, H_M	1	−	− V	

Notes

1. I_{P_2} is almost entirely dependent on the external load.
2. T_{amb} = 25 °C; all other terminals at V_{P0}

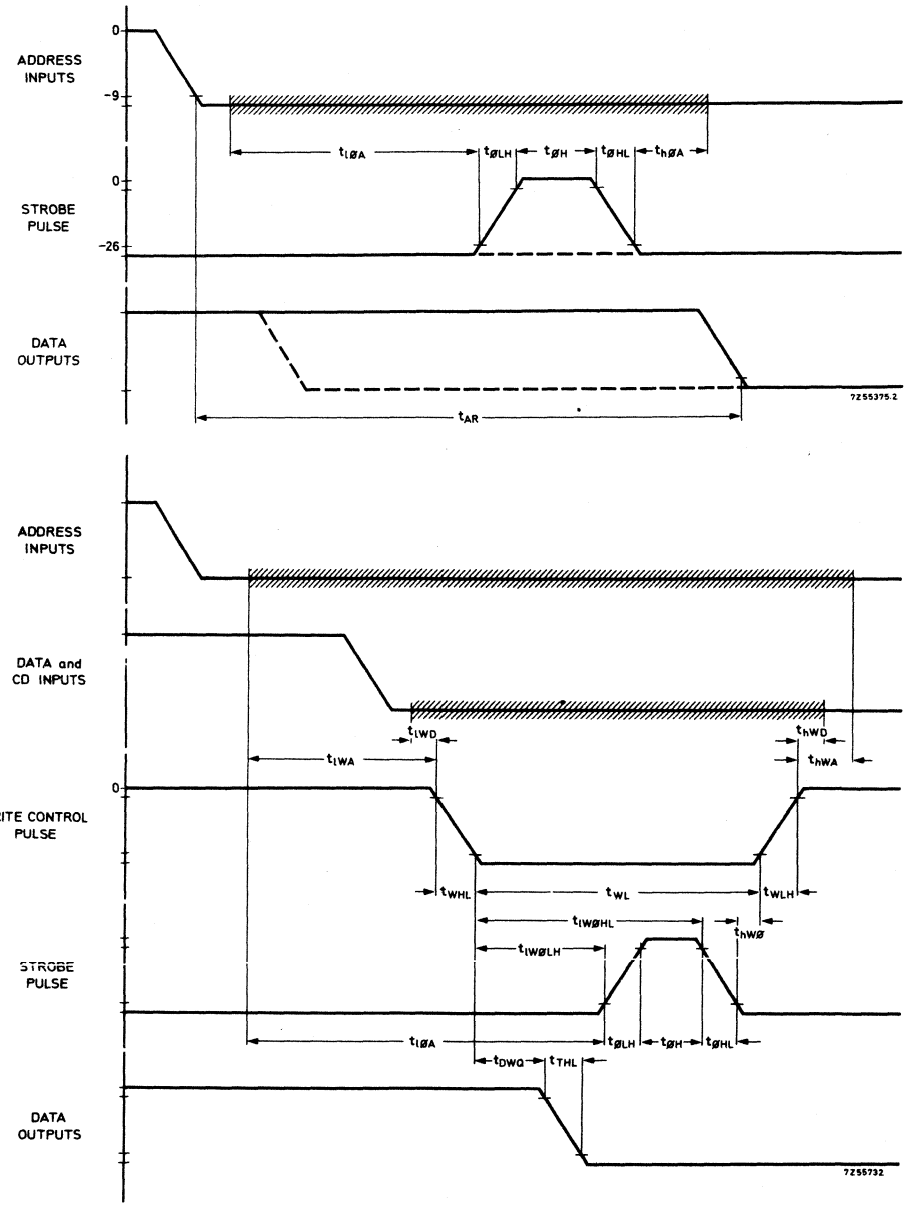
CHARACTERISTICS (continued)

STAND-BY POWER CONSIDERATIONS

If the FDQ106 is to be kept in stand-by condition with all d.c. power to it shut off, the stored data can be preserved by maintaining a 10 kHz strobe clock rate.
Since essentially all d.c. power dissipation is in the address input inverters, decode circuits and output buffers, the power required to preserve the stored data is limited to reactive strobe power and whatever leakage current occurs at the strobe input lead. Since the reactive strobe power is frequency dependent, the lowest allowable frequency should be used for stand-by operation. A strobe frequency of less than 10 kHz may be used if the ambient temperature is less than +85 ^{o}C.
D.C. power may be switched on and off only at those moments when a change of address is also allowable.
After re-application of d.c. power, a series of about 10 strobe pulses is required before the circuit is fully operational.

CHARACTERISTICS (continued)

TIMING DIAGRAM



CHARACTERISTICS (continued)

Timing diagram notes

1. To avoid destroying data in non-addressed memory cells, the address inputs must not be made to change state during the shaded intervals in the timing diagrams.
2. When the CD input is LOW, the WRITE logic is inoperative and the output is floating. The CD input affects the output directly, with a propagation delay of about 100 ns. It may change state an any time except during the shaded interval in the timing diagram.
3. No strobe pulse is required during a READ cycle; however, a minimum strobe frequency of 10 kHz is required and strobe pulses may occur during READ cycles if the requirement of note 1 is observed.
4. To write into the device, a WRITE control pulse and a strobe pulse are required, and the CD input must be HIGH.
   During a WRITE cycle the memory outputs are active and the new data will appear at the outputs after t_{DWQ} ($\leq$ 200 ns).
   However, data is actually written into the memory cell by the trailing edge of the strobe pulse.
5. Wheter they are in READ or WRITE cycles, all memory cells are simultaneously refreshed during a strobe pulse. No cycling through addresses is required.
6. If the address inputs remain unchanged, the data outputs appear as d.c. levels, no return to zero.

GLOSSARY OF TERMS

1. Strobe pulse width: $t_{\phi H}$
   The time for which the strobe pulse is in the HIGH state (ϕ is nominally LOW)
2. Write control pulse width: t_{WL}
   The time for which the WRITE control pulse is LOW ($V_{WL} \leq -26$ V)
3. Pulse fall time: t_{WHL} and $t_{\phi HL}$
   The time between the 10 % and 90 % voltage points as the pulse goes from HIGH to LOW.
4. Pulse rise time: t_{WLH} and $t_{\phi LH}$
   The time between the 90 % and 10 % voltage points as the pulse goes from LOW to HIGH.
5. Strobe address lead time: $t_{\ell \phi A}$
   The time before the 10 % strobe pulse voltage point for which the address must be present.
6. Write address lead time: $t_{\ell WA}$
   The time before the 10 % write control pulse voltage point for which the address must be present.
7. Write data lead time: $t_{\ell WD}$
   The time before the 10 % write control pulse voltage point for which the data must be present at the data inputs ($t_{\ell WD} \geq 0$)
8. Read access time: t_{AR}
   After the address inputs reach the correct level, the time that elapses before the outputs start to change state.

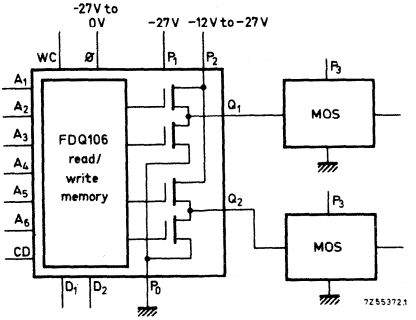
CHARACTERISTICS (continued)

9. Write-pulse-to-output propagation time: t_{DWQ}
   After the write control pulse reaches the LOW state, the time that elapses before the outputs start to change state.
10. Output fall transition time: t_{THL}
    The time between the 10% and 90% voltage points as the output goes from HIGH to LOW.
11. Output rise transition time: t_{TLH}
    The time between the 90% and 10% voltage points as the output goes from LOW to HIGH.
12. Write address and write data hold times: t_{hWA} and t_{hWD}
    The time for which the write control pulse must be in the HIGH state before the address or inputs may change state ($t_{hWA} \geq 0$ and $t_{hWD} \geq 0$).
13. Strobe address hold time: $t_{h\phi A}$
    The time for which the strobe pulse must be LOW before the address may change state ($t_{h\phi A} \geq 0$)
14. Write control-strobe pulse lead times: $t_{\ell W\phi LH}$ and $t_{\ell W\phi HL}$
    The time before the 10% voltage point on the strobe pulse leading edge, or the 90% voltage point on the strobe pulse trailing edge, for which the write control pulse must be in the LOW state ($t_{\ell W\phi LH} \geq 0$; $t_{\ell W\phi HL} \geq 400$ ns).
15. Write control-strobe pulse hold time: $t_{hW\phi}$
    The time after the strobe pulse has returned to LOW for which the write control pulse remain LOW ($t_{hW\phi} \geq 0$).

OUTPUT BUFFER DESCRIPTION

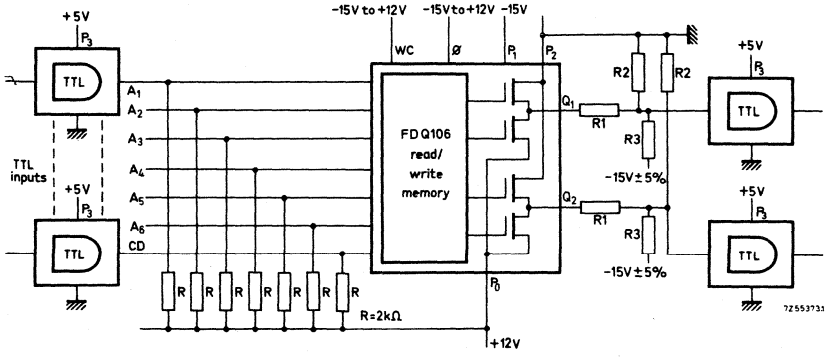
The output buffers used on the FDQ106 are identical to these used on the FDN106, FDN116, FDN126 and FDN136 dynamic shift registers. The V_Q versus I_Q characteristics shown in the data sheets for these shift registers also apply, therefore, to the FDQ106. The V_P supply voltage may be varied between 0 and −28 V according to the load requirements.

1. Biasing circuit A may be used to drive MOS loads.
   Normal MOS input signals must drive the address and other input signals in accordance with the specified electrical characteristics.



Biasing circuit A

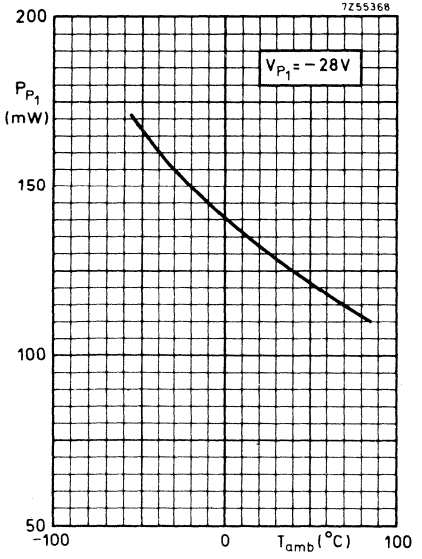
2. Biasing circuit B allows the MOS device to be interfaced with TTL or DTL at both data inputs and data outputs. Note that the TTL or DTL integrated circuit must be able to withstand +12 V applied to the output lead, most of our FC gates [1]) and FJ gates [1]) satisfy this requirement. Some open collector FJ gates have a minimum output breakdown voltage guarantee of 15 V. ([1]) non-R_C types)

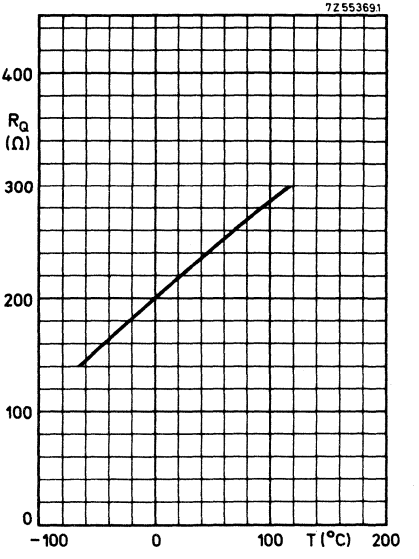


Fan-out = 1		Fan-out = 2	
R1 = 1.2 kΩ	M_H = 600 mV	R1 = 560 Ω	M_H = 450 mV
R2 = 1 kΩ	M_L = 750 mV	R2 = 1 kΩ	M_L = 500 mV
R3 = 10 kΩ	P_{HIGH} = 13 mW	R3 = 4.7 kΩ	P_{HIGH} = 41 mV

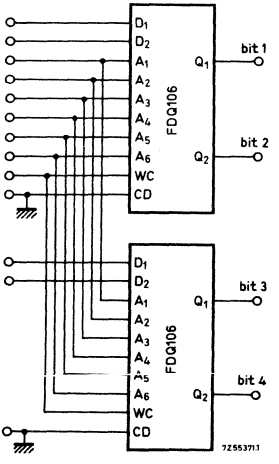
Biasing circuit B

TYPICAL PERFORMANCE

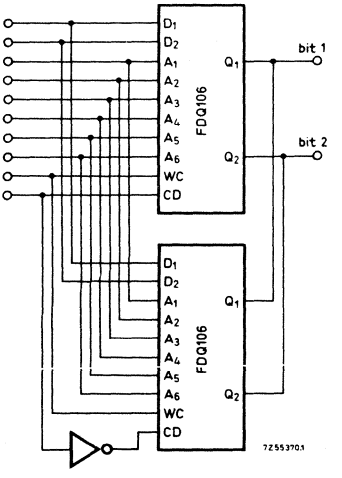




EXPANDED MEMORIES



64 word, 4 bits per word



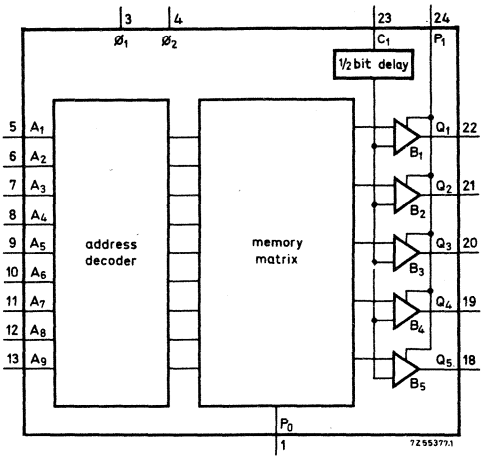
128 word, 2 bits per word

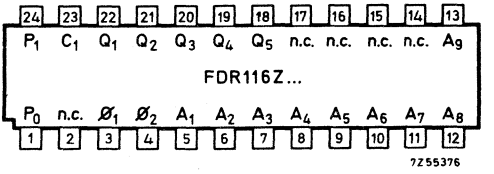
A LOW state at the chip **disable** input will cause both push-pull output buffers to turn off. In the off state, the output impedance of the output transistors becomes very high (approximately 5 MΩ) making it possible to use wired-or configurations with other FDQ106 outputs.

Chip disable also inhibits write, which allows common bussing of data input lines.

The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

READ-ONLY MEMORY, 512 WORD, 5 BITS PER WORD





QUICK REFERENCE DATA				
Read access time	t_{AR}	max.	850	ns
Clock rate	f_ϕ	max.	1.2	MHz
Power dissipation at f_ϕ = 1 MHz	P_ϕ	typ.	90	mw
D.C. noise margin	M_L, M_H	>	1	V
Operating ambient temperature	T_{amb}	−55 to +85		°C

PACKAGE OUTLINE 24 lead metal-ceramic dual in-line (See General Section)

GENERAL DESCRIPTION

The FDR116Z is a monolithic 2560 bit read only memory. When ordering an FDR116Z the customer must send a bit pattern matrix with the desired content. For performance evaluation, we can supply specimens of FDR116Z1, which is identical to the FDR116Z but contains a bit pattern of our own. The FDR116Z requires a two phase clock, but the outputs remain steady as long as the address remains unchanged. The normal configuration is as a 512 word, 5 bits per word, parallel output ROM. An output inhibit control allows the use of multiple FDR116Z in a wired-OR configuration.

The memory matrix is programmed with the aid of a mask pattern during manufacture. The only d.c. supply is the output buffer supply, which is variable and can be biased to drive bipolar output loads direct.

The patterns permanently stored in the memory matrix of the FDR116Z1 are described in the following data sheets.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages on all data inputs, clock inputs, outputs and supply terminals, with reference to P_0		+0.5 to	−30	V
Power dissipation up to $T_{amb} = 25\,^{o}C$	P_{tot}	max.	1	W
Junction temperature	T_j	max.	150	^{o}C
Storage temperature	T_{stg}	−65 to	+150	^{o}C
Total current through terminal P_2	$-I_{P_2}$	max.	40	mA
Output current (per output)	$\pm I_Q$	max.	20	mA

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	125	$^{o}C/W$

CHARACTERISTICS at T_{amb} = −55 to +85 °C

ELECTRICAL DRIVE REQUIREMENTS	Symbol	min.	typ.	max.	Conditions and references
Clock rate	f_ϕ	0.1	–	1.2 MHz	see note
Clock pulse width	$t_{\phi 1L}$	0.50	–	1.0 μs	see timing diagram for parameter definitions
	$t_{\phi 2L}$	0.25	–	1.0 μs	
Clock pulse fall time	$t_{\phi HL}$	–	–	0.10 μs	see note
Clock pulse rise time	$t_{\phi LH}$	–	–	0.10 μs	
Clock delay time	$t_{\phi 1\phi 2}$	0	–	4.5 μs	
Clock delay time	$t_{\phi 2\phi 1}$	0	–	4.5 μs	
Clock input voltage level					
HIGH	$V_{\phi H}$	−2	0	+0.3 V	
LOW	$V_{\phi L}$	−28	−26	−24 V	
Address input and output inhibit input logic levels:					
HIGH	V_{AH}, V_{CH}	−2	0	+0.3 V	
LOW	V_{AL}, V_{CL}	−14	−12	−9 V	

Note

At frequencies higher than 870 kHz, $t_{\phi 1Lmax}$ and $t_{\phi 2Lmin}$ will be determined by $t_{\phi LHmax}$ and $t_{\phi HLmax}$.

CHARACTERISTICS

Test conditions: V_{P_1} = −12 V to −14 V; T_{amb} = −55 to +85 °C; P_0 = grounded; **standard load: 30 pF in parallel with 150 kΩ to P_0.**

ELECTRICAL DATA	Symbol	min.	typ.	max.		Conditions and references
Read access time	t_{AR}	–	750	850	ns	see note 1
Output levels:						
HIGH	V_{QH}	−1	–	0	V	
LOW	V_{QL}	−14	–	−10	V	
Address input capacitance	C_A	–	3.2	4.0	pF	bias: V_A = 0 V; f_ϕ = 1 MHz
Output inhibit input capacitance	C_C	–	3.2	4.0	pF	bias: V_C; V_ϕ = 0 V; f_ϕ = 1 MHz
Clock input capacitance	$C_{\phi 1}$	–	21	30	pF	bias: V_C; V_ϕ = 0 V; f_ϕ = 1 MHz
	$C_{\phi 2}$	–	13	18	pF	bias: V_C; V_ϕ = 0 V; f_ϕ = 1 MHz
	$C_{\phi 1}$	–	13	18	pF	bias: V_ϕ = −26 V; f_ϕ = 1 MHz
	$C_{\phi 2}$	–	7.4	10	pF	bias: V_ϕ = −26 V; f_ϕ = 1 MHz
Leakage currents:						
Address input and output inhibit input currents	$-I_{AL}$, $-I_{CL}$	–	–	1	μA	V_A = V_C = −15 V; all other terminals at V_{P_0}; T_{amb} = 25 °C
Clock input current	$-I_{\phi L}$	–	–	100	μA	V_ϕ = −28 V; all other terminals at V_{P_0}; T_{amb} = 25 °C
Output resistance						
HIGH	R_{QH}	–	300	–	Ω	
LOW	R_{QL}	–	170	–	Ω	V_{P_1} = −5 V
Clock power dissipation (see note 2)	P_ϕ	–	36	–	mW	f_ϕ = 1 MHz
Input current (see note 3)	$-I_{P_1}$	–	4.0	–	mA	V_{P_1} = −13 V; f_ϕ = 1 MHz; T_{amb} = 25 °C
Output transition times:						
fall time	t_{THL}	–	100	–	ns	
rise time	t_{TLH}	–	100	–	ns	
Delay times: fall time	t_{DHL}	–	20	–	ns	
rise time	t_{DLH}	–	20	–	ns	
D.C. noise margin	M_L, M_H	1	–	–	V	

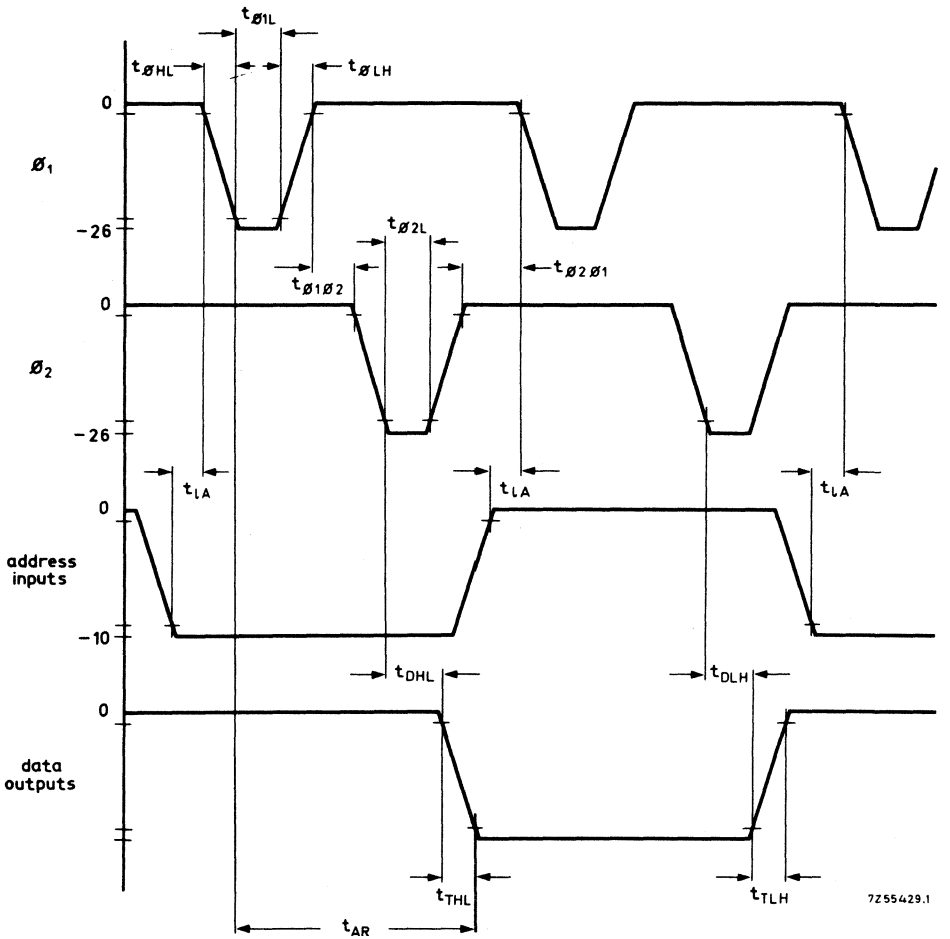
Note 1: The minimum access time assumes the summation of the rise time of ϕ_1 and the fall time of ϕ_2 is less than 40 ns.

Note 2: No d.c. power is dissipated in the decoder or memory matrix; the quoted power dissipation is a.c. only.

Note 3: I_{P_1} is almost entirely dependent on the external load.

CHARACTERISTICS (continued)

TIMING DIAGRAM



Note

The indicated points on the vertical axis are specified in the glossary of terms.

Address and output inhibit timing requirements:

1. Address input (and output inhibit input) signals are clocked into the memory during ϕ_1, and must remain present throughout ϕ_1. Address lead time ($t_{\ell A}$) must be ≥ 0.
2. The output signals remain steady **for as many clock cycles as the address and output** inhibit signals remain unchanged.

CHARACTERISTICS (continued)

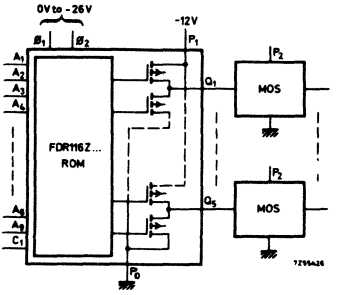
GLOSSARY OF TERMS

1. Clock pulse width: $t_{\phi L}$
   The time for which the clock pulse is LOW; $V_\phi \leq -24$ V
2. Clock pulse fall time: $t_{\phi HL}$
   The time between the 10% and 90% voltage points as the clock pulse goes from HIGH to LOW.
3. Clock pulse rise time: $t_{\phi LH}$
   The time between the 90% and 10% voltage points as the clock pulse goes from LOW to HIGH.
4. Clock delay time: $t_{\phi 1 \phi 2}$; $t_{\phi 2 \phi 1}$
   The least allowable time between the end of the ϕ_1 (or ϕ_2) clock pulse and the start of the ϕ_2 (or ϕ_1) clock pulse, defined at −2 V.
5. Fall delay time: t_{DHL}
   After the clock pulse ϕ_2 reaches LOW, the time that elapses before the output starts to change from HIGH to LOW.
6. Rise delay time: t_{DLH}
   After the clock pulse ϕ_2 reaches LOW, the time that elapses before the output starts to change from LOW to HIGH.
7. Output fall transition time: t_{THL}
   The time between the 10% and 90% voltage points as the output goes from HIGH to LOW.
8. Output rise transition time: t_{TLH}
   The time between the 90% and 10% voltage points as the output goes from LOW to HIGH.
9. Read access time: t_{AR}
   The time between the 90% point on the negative going edge of the clock pulse ϕ_1 and the time at which the output is present, defined at 90%.

OUTPUT BUFFER DESCRIPTION

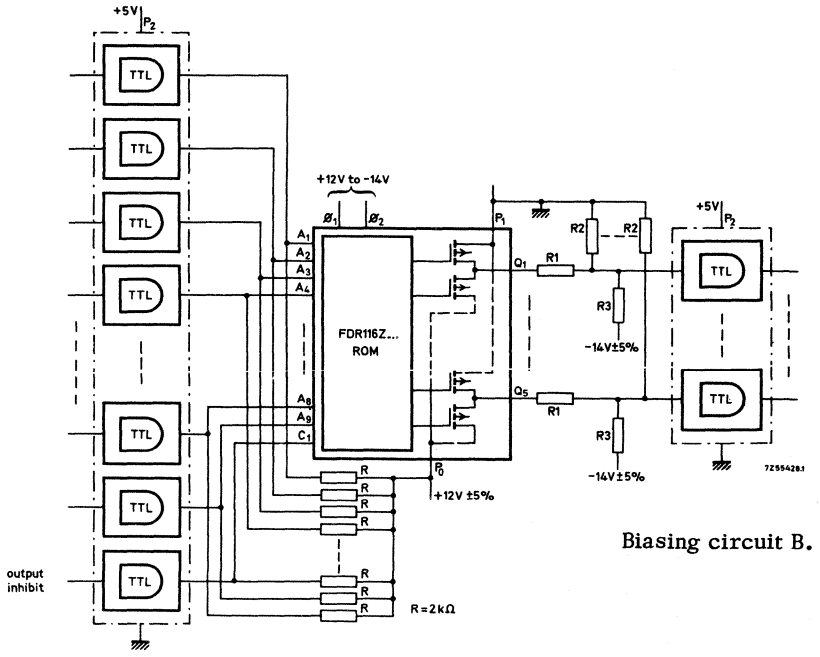
The only d.c. supply required is V_{P_1}, the push-pull output buffer supply. V_{P_1} may be varied between 0 and −28 V according to the output voltage swing required. It does not affect the operating speed of the memory.

1. Biasing circuit A is used when driving MOS loads. Normal MOS input signals must drive the address and inhibit inputs.



Biasing circuit A.

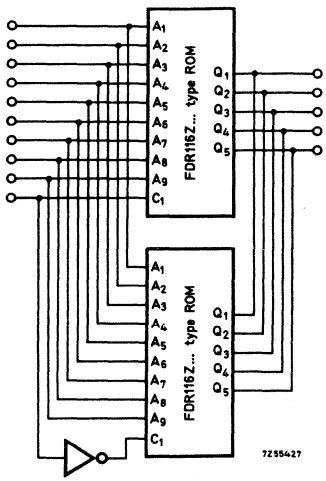
2. Biasing circuit B may be used to interface with TTL, both at the input and the output of the ROM. Note that no active interface devices are required. At the address and C inputs any TTL devices can be used that will sustain a minimum of +12 V at their output terminals.



Biasing circuit B.

WIRED-OR APPLICATIONS

Use of wired-or output capability:
Applying a LOW signal to the output inhibit leads will cause both of the push pull output transistors associated with each output driver to turn off. Their output impedances are then very high (about 5 MΩ) and they can be wired-OR with other ROM output buffers without affecting the output drive capability of any buffer operating in the low impedance mode. This output inhibit wired-OR capability makes it possible to use the FDR116Z type ROM in many different applications, such as the one shown here.



1024 words, 5 bits per word ROM

PROCEDURE FOR ORDERING A SPECIAL BIT PATTERN

To ensure accuracy when ordering a special bit pattern for a Read Only Memory (ROM) mask, customers should make use of the form on page 12. Eight forms are needed for 512 word memories. The completed forms enable us to transfer any desired bit pattern into a standard ROM without error. After receipt of the forms our procedure is as follows:

1. An IBM card is punched for each row of each sheet of the form. (If he prefers to do so, the customer may punch his own cards and supply them to us, provided their format is identical with that of the forms).
2. The punched card are incorporated in a computer program that originates the following:
   - a duplicate of the ordered bit pattern, for verification.
   - a control tape for programming final electrical testing of the customers's ROM.
   - a control tape embodying the ordered pattern of ones and zeros to govern the movement of the automatic plotter used in mask making.
3. The computer print-out is checked against the original order forms; a copy is also sent to the customer for his verification and signature.
4. Upon receipts of the customer's signed verification, full scale masks embodying the desired pattern are made.

INSTRUCTION FOR COMPLETING THE FORMS

A. Customer block: ON EACH FORM

Enter Name, Date and Authorized Signature in the spaces provided.

B. The ADDRESS INPUTS and CONTENTS

Each page of the ROM Bit Pattern Form is laid out for 64 consecutive words; 16 in each of the four columns (00, 01, 10 and 11).

1. ADDRESS INPUTS

   a) There are nine Address Inputs; the right-hand bit is always bit 1 and is the least significant bit; the left-hand bit is bit 9, it is the most significant. The Address Input leads on the ROM package are labelled A_1, A_2, etc., to correspond.

   b) The states of bits 1 to 4 are listed consecutively down the page. The state of bits 5 and 6 are at the head of each of four output columns. The Address Input of 64 consecutive words are thus uniquely specified on each page.

   c) Bit 7, 8 and 9 specify sets of memory locations, 1 set of 64 words per page. These spaces should be filled by the customer using a consecutive full binary code. The first position on page 1 of your specification should be three (or two) zeros. [1])
   Memories of 512 words need 8 pages, of specifications.

   d) Only ones (1 = LOW) or zeros (0 = HIGH) should be used in completing the form.

1) See example on page 12

PROCEDURE FOR ORDERING A SPECIAL BIT PATTERN (continued)

2. CONTENTS (DATA OUTPUTS)

   a) Each column has provision for words of 10 bits numbered 1 to 10, bit 1 is always the right-hand bit. The output leads of the ROM package are labelled Q_1, Q_2, etc., to correspond.
   b) The requisite bit pattern should be inserted under headings 1 to 5 using only *ones* (1 = LOW) and *zeros* (0 = HIGH).

3. AUTHORIZED SIGNATURE

   Having completed the bit pattern, the customer should check that the forms are numbered, dated, and signed, as they constitute formal evidence of his request. In the event that the customer provides his own punched cards the signature on the computer duplicate will serve as formal evidence.

CHARACTER GENERATION

The FDR116Z1 is meant for generating ASCII characters for display in a system in which each character is made up of seven 5-bit rows that are traced one at a time. It is capable of storing 64 different characters, each having its own 6-bit address.

To generate a line of characters for display, word addresses are applied in sequence to the WORD SELECT inputs A_1 to A_3 and character addresses to the CHARACTER SELECT inputs A_4 to A_9. First, the row to be traced is selected by applying its address (3 bits) to inputs A_1 to A_3; then the desired characters are selected by applying their addresses (6 bits each) to inputs A_4 to A_9. When one row in a line of characters has been traced, the next row is generated by applying a new word address (inputs A_1 to A_3) and repeating the same sequence of character addresses as before. After the sequence of character addresses has been repeated in conjunction with the word addresses for all seven rows, the full line of characters has been generated. Of the FDR116Z1, a selection is available, which has a maximum read rating of 1.67 MHz (cycle time 600 ns).

PHILIPS
Electronic Components
and Materials
Integrated Circuits

Read Only Memory Bit Pattern

FDR 116...

page of

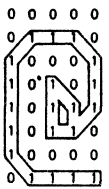
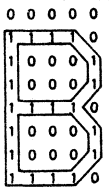
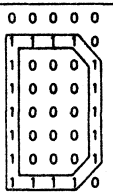
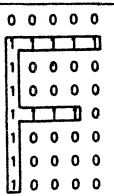
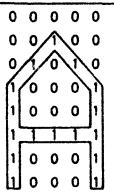
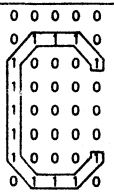
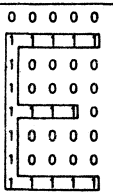
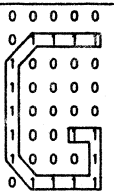
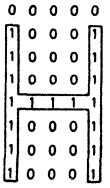
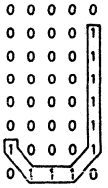
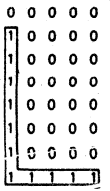
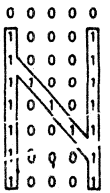
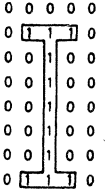
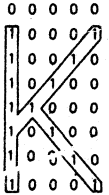
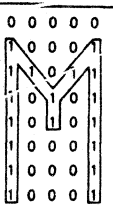
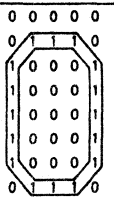
AUTHORIZED SIGNATURE

CUSTOMER NAME:

DATE

Note: 1 = LOW; 0 = HIGH

ADDRESS INPUTS 9 8 7 6 5 4 3 2 1	CONTENTS 00 OUTPUTS 10 9 8 7 6 5 4 3 2 1	01 OUTPUTS 10 9 8 7 6 5 4 3 2 1	10 OUTPUTS 10 9 8 7 6 5 4 3 2 1	11 OUTPUTS 10 9 8 7 6 5 4 3 2 1
	1 2 3 - - 4 5 6 7	8 9 10 11 12 13 14 15 16 17	18 19 20 21 22 23 24 25 26 27	28 29 30 31 32 33 34 35 36 37	38 39 40 41 42 43 44 45 46 47
X X 0 0 0 0				
X X 0 0 0 1				
X X 0 0 1 0				
X X 0 0 1 1				
X X 0 1 0 0				
X X 0 1 0 1				
X X 0 1 1 0				
X X 0 1 1 1				
X X 1 0 0 0				
X X 1 0 0 1				
X X 1 0 1 0				
X X 1 0 1 1				
X X 1 1 0 0				
X X 1 1 0 1				
X X 1 1 1 0				
X X 1 1 1 1				

ASCII CHARACTER ADDRESS INPUTS	WORD SELECT INPUTS	OUTPUTS			
A9 A8 A7 A6 A5 A4	A3 A2 A1	Q5 Q4 Q3 Q2 Q1	Q5 Q4 Q3 Q2 Q1	Q5 Q4 Q3 Q2 Q1	Q5 Q4 Q3 Q2 Q1
X X		00	01	10	11
0 0 0 X X 0	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1				
0 0 0 X X 1	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1				
0 0 1 X X 0	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1				
0 0 1 X X 1	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1				

ASCII CHARACTER ADDRESS INPUTS	WORD SELECT INPUTS	OUTPUTS			
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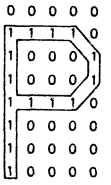
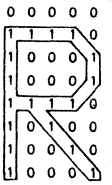
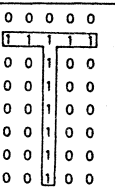
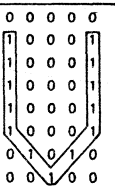
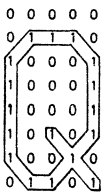
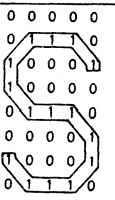
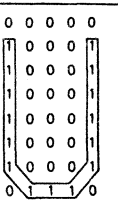
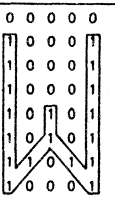
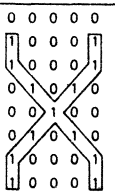
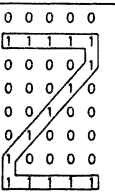
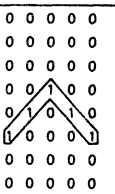
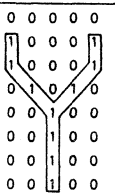
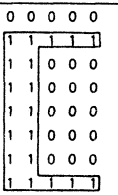
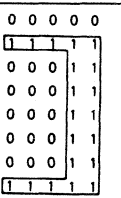
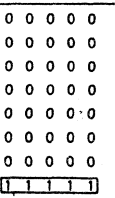
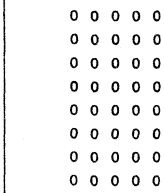
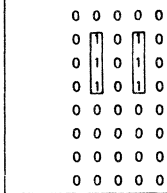
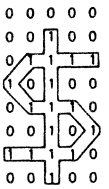
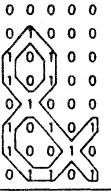
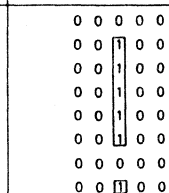
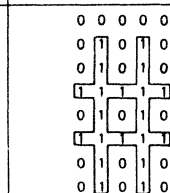
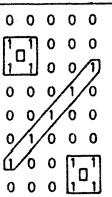
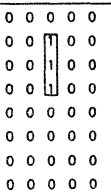
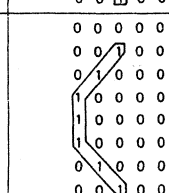
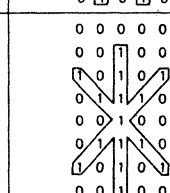
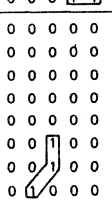
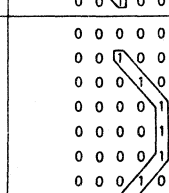
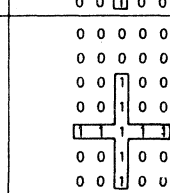
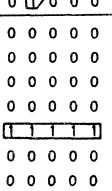
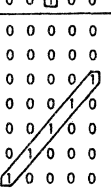
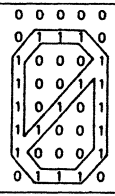
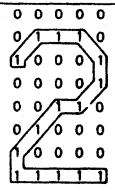
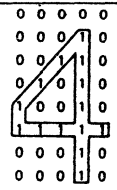
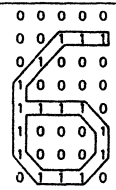
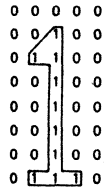
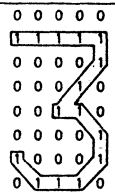
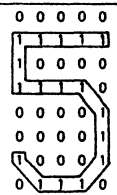
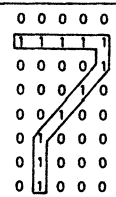
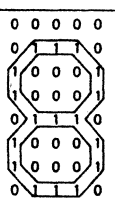
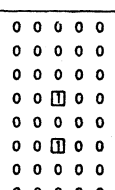
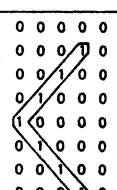
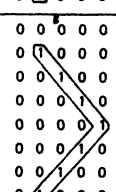
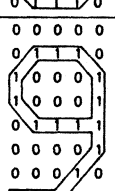
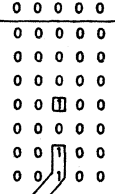
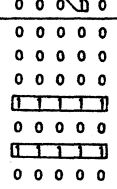
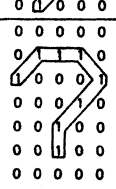
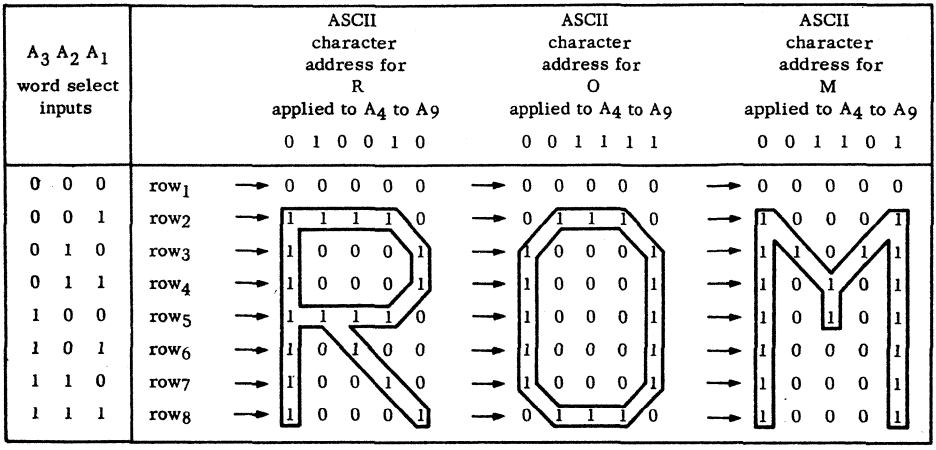
X X		00	01	10	11
0 1 0 X X 0	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1				
0 1 0 X X 1	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1				
0 1 1 X X 0	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1				
0 1 1 X X 1	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1				

ASCII CHARACTER ADDRESS INPUTS	WORD SELECT INPUTS	OUTPUTS			
$A_9\ A_8\ A_7\ A_6\ A_5\ A_4$	$A_3\ A_2\ A_1$	$Q_5\ Q_4\ Q_3\ Q_2\ Q_1$	$Q_5\ Q_4\ Q_3\ Q_2\ Q_1$	$Q_5\ Q_4\ Q_3\ Q_2\ Q_1$	$Q_5\ Q_4\ Q_3\ Q_2\ Q_1$
X X		00	01	10	11
1 0 0 X X 0	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1				
1 0 0 X X 1	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1				
1 0 1 X X 0	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1				
1 0 1 X X 1	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1				

ASCII CHARACTER ADDRESS INPUTS	WORD SELECT INPUTS	OUTPUTS			
A_9 A_8 A_7 A_6 A_5 A_4	A_3 A_2 A_1	Q_5 Q_4 Q_3 Q_2 Q_1	Q_5 Q_4 Q_3 Q_2 Q_1	Q_5 Q_4 Q_3 Q_2 Q_1	Q_5 Q_4 Q_3 Q_2 Q_1
X X		00	01	10	11
1 1 0 X X 0	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1				
1 1 0 X X 1	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1				
1 1 1 X X 0	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1				
1 1 1 X X 1	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1				

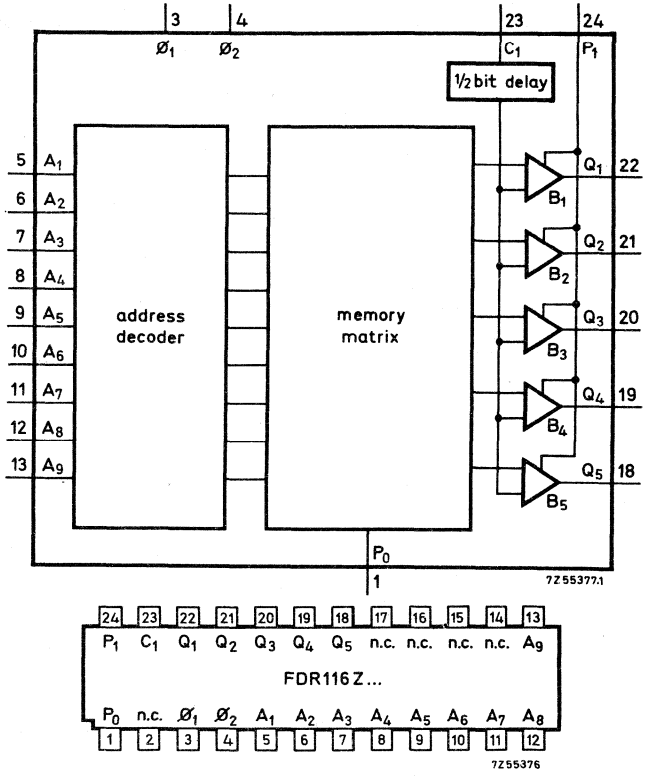
ROM ORGANISATION

In this example, with the word select input address fixed, the ASCII character addresses are sequentially altered to produce one line of three different characters, left to right. After 8 sequential binary word select iterations using the same character address sequence, the complete line of characters is formed, including a SPACE line.



The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

CHARACTER GENERATOR (5 × 7 DOT MATRIX; ROW SCAN SYSTEM)



P_0 and metal lid on bottom of the package are connected

QUICK REFERENCE DATA				
Read acces time	t_{AR}	max.	850	ns
Clock rate	f_ϕ	max.	1.2	MHz
Power dissipation at f_ϕ = 1 MHz	P_ϕ	typ.	90	mW
D.C. noise margin	M_L, M_H	>	1	V
Operating ambient temperature	T_{amb}	−55 to	+85	°C

PACKAGE OUTLINE 24 lead metal-ceramic dual in-line (See General Section).

GENERAL DESCRIPTION

The FDR116Z2 is a pre-programmed specimen of the FDR116Z.
It is intended for use as character generator in display systems, using a 5 x 7 dot matrix, where the characters are built-up with one horizontal row at a time.
The device contains a sub-set of the ASCII character set viz. the lower case symbols and a pictorial representation of the control symbols.
When the device is used in combination with the FDR116Z1, the full 7-bit ASCII code character set can be displayed.

RATINGS

CHARACTERISTICS

OUTPUT BUFFER DESCRIPTION

For this information see data sheets of FDR116Z

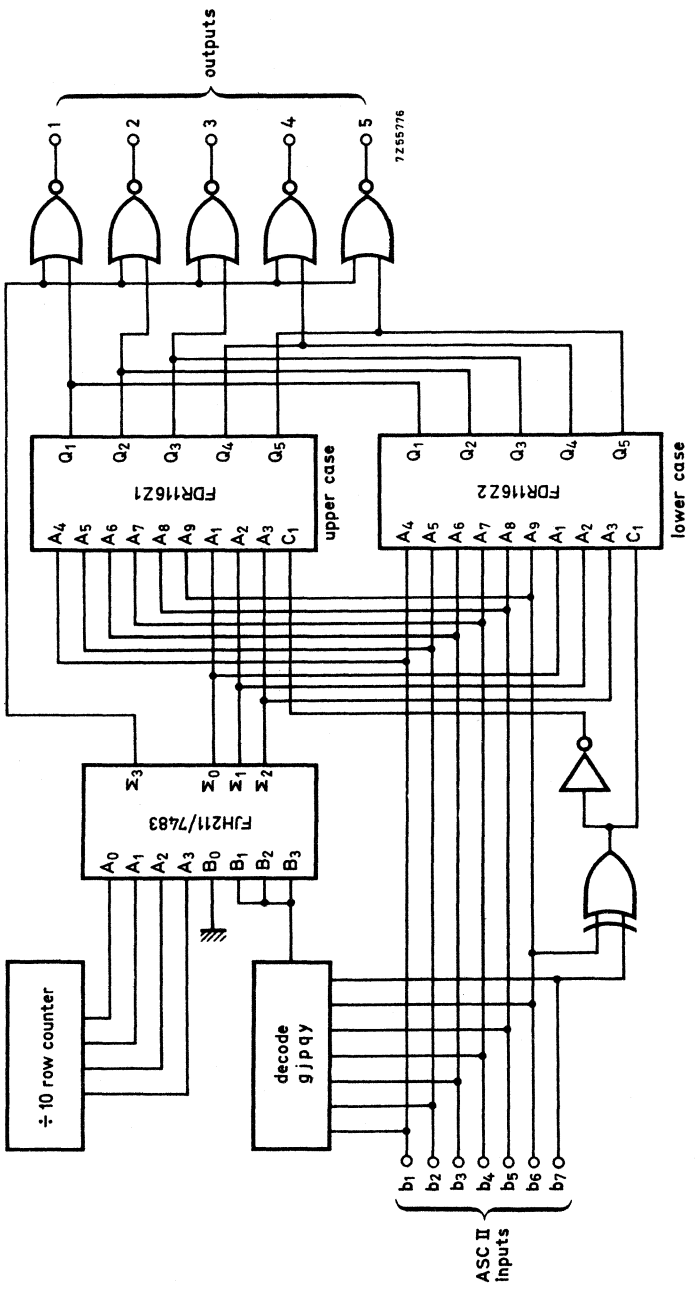
APPLICATION INFORMATION

To use the FDR116Z2 as a character generator, the ASCII code of the character to be displayed should be applied to the address inputs A_4 to A_9 with the following correspondence:

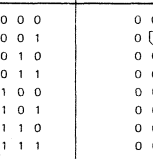
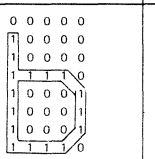
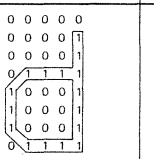
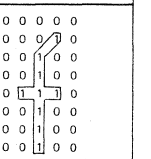
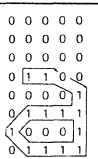
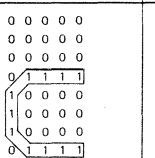
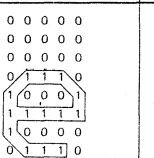
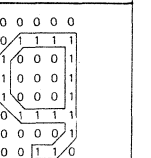
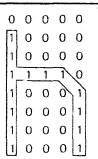
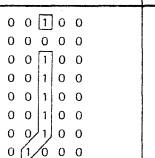
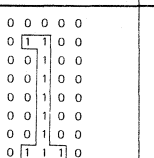
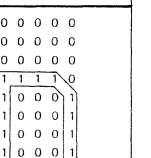
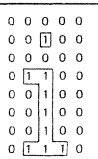
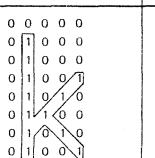
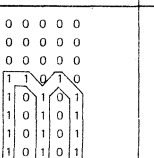
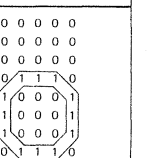
ASCII bit	address input
b_1	A_4
b_2	A_5
b_3	A_6
b_4	A_7
b_5	A_8
b_6	A_9

For row selection a three bit binary number should be applied to address inputs A_1 to A_3 (A_1 being the least significant bit).
On page 5 a 128 character ASCII character generator is given.
The diagram incorporates a "descender" circuit, with which the lower case g, j, p, q and y can be lowered two rows.
For this purpose an adder circuit is inserted between the row counter and the READ ONLY MEMORIES.
When a lower case g, j, p, q or y is detected a binary 2 is substracted from the row number (actually the binary number 14 is added), which causes the character to be displayed two rows lower.
The output Σ_3 of the adder is used to blank all outputs in order to avoid a repeated display of the character during rows 9 and 10 in the "normal" position, or during rows 0 and 1 in the "descended" position.

APPLICATION INFORMATION (continued)

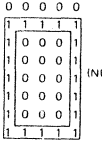
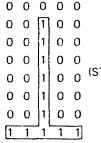
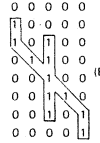
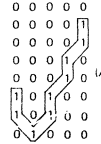
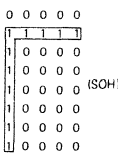
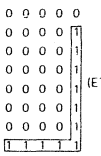
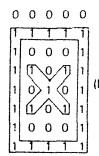
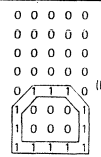
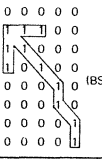
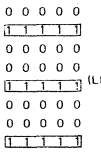
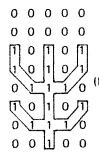
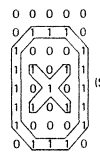
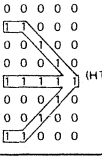
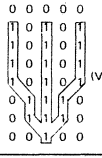
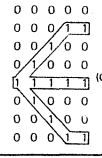
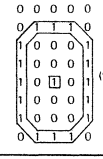


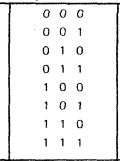
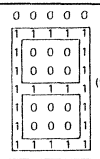
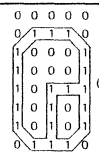
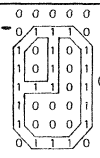
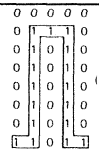
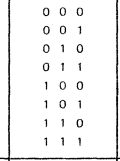
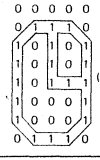
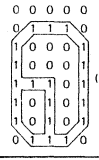
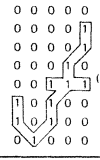
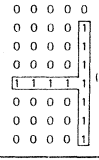
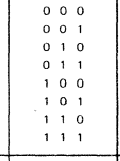
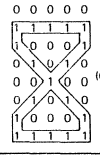
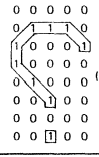
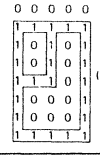
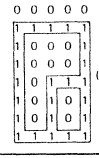
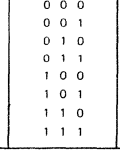
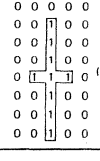
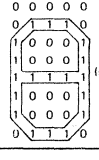
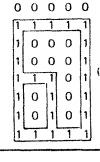
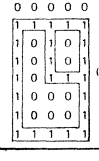
FDR116Z2 BIT PATTERN AND FONT

ASCII CHARACTER ADDRESS INPUTS $b_6\ b_5\ b_4\ b_3\ b_2\ b_1$	LINE SELECT INPUTS	OUTPUTS			
$A_9\ A_8\ A_7\ A_6\ A_5\ A_4$	$A_3\ A_2\ A_1$	$Q_5\ Q_4\ Q_3\ Q_2\ Q_1$	$Q_5\ Q_4\ Q_3\ Q_2\ Q_1$	$Q_5\ Q_4\ Q_3\ Q_2\ Q_1$	$Q_5\ Q_4\ Q_3\ Q_2\ Q_1$
X X		00	01	10	11
1 0 0 X X 0	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1				
1 0 0 X X 1	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1				
1 0 1 X X 0	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1				
1 0 1 X X 1	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1				

NOTE: 1 = LOW; 0 = HIGH

FDR116Z2 BIT PATTERN AND FONT (continued)

ASCII CHARACTER ADDRESS INPUTS $b_6\ b_5\ b_4\ b_3\ b_2\ b_1$	LINE SELECT INPUTS	OUTPUTS			
$A_9\ A_8\ A_7\ A_6\ A_5\ A_4$	$A_3\ A_2\ A_1$	$Q_5\ Q_4\ Q_3\ Q_2\ Q_1$	$Q_5\ Q_4\ Q_3\ Q_2\ Q_1$	$Q_5\ Q_4\ Q_3\ Q_2\ Q_1$	$Q_5\ Q_4\ Q_3\ Q_2\ Q_1$
X X		00	01	10	11
0 0 0 X X 0	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	 (NUL)*	 (STX)*	 (EOT)*	 (ACK)*
0 0 0 X X 1	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	 (SOH)*	 (ETX)*	 (ENQ)*	 (BEL)*
0 0 1 X X 0	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	 (BS)*	 (LF)*	 (FF)*	 (SO)*
0 0 1 X X 1	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	 (HT)*	 (VT)*	 (CR)*	 (SI)*

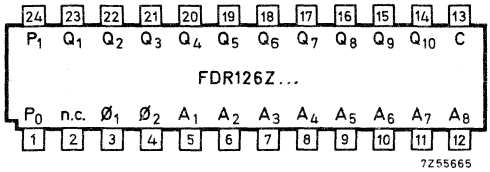
0 1 0 X X 0		 (DLE)*	 (DC2)*	 (DC4)*	 (SYN)*
0 1 0 X X 1		 (DC1)*	 (DC3)*	 (NAK)*	 (ETB)*
0 1 1 X X 0		 (CAN)*	 (SUB)*	 (FS)*	 (RS)*
0 1 1 X X 1		 (EM)*	 (ESC)*	 (GS)*	 (US)*

* The letters in parenthesis identify the control code corresponding to the appropriate 35 Bit pictorial representation. These representations were obtained from the USASI x 3.2 Code Practice Manual.

NOTE: 1 = LOW; 0 = HIGH

The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

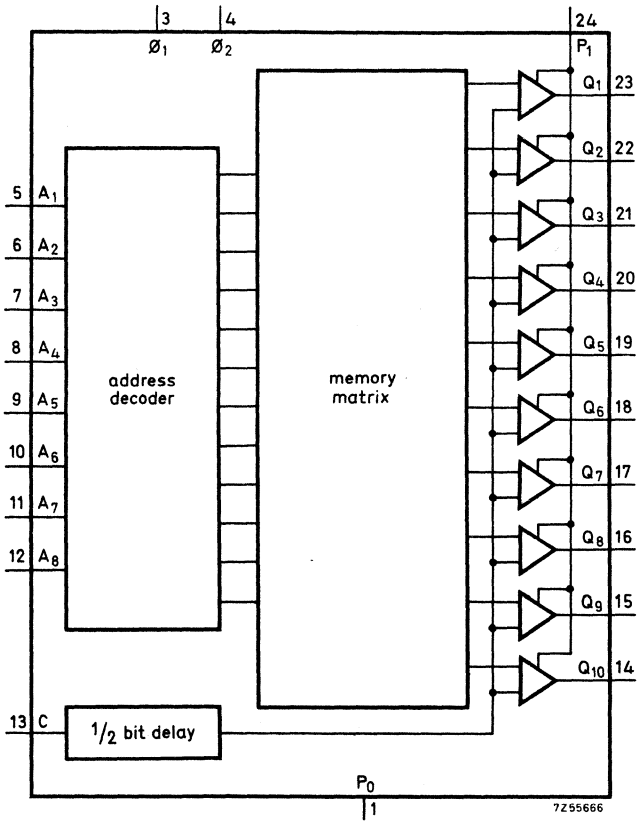
READ ONLY MEMORY, 256 WORD, 10 BITS PER WORD



P_0 and metal package bottom are connected.

QUICK REFERENCE DATA				
Read access time	t_{AR}	max.	1	µs
Clock rate	f_ϕ	0.1 to	1	MHz
Power dissipation at f_ϕ = 1 MHz	P_{av}	typ.	100	mw
D.C. noise margin	M_H, M_L	>	1.0	V
Operating ambient temperature	T_{amb}	−55 to +85		°C

PACKAGE OUTLINE 24 lead ceramic dual in-line. (See General Section)


3
Ø1
4
Ø2
24
P1
Q1 23
Q2 22
Q3 21
Q4 20
Q5 19
Q6 18
Q7 17
Q8 16
Q9 15
Q10 14
5 A1
6 A2
7 A3
8 A4
9 A5
10 A6
11 A7
12 A8
address decoder
memory matrix
13 C
1/2 bit delay
P0
1
7Z55666

GENERAL DESCRIPTION

The FDR126Z is a monolithic 2560 bit read only memory. When ordering an FDR126Z the customer must send a bit pattern matrix (see example on pages 12, 14 to 17) with the desired content. For performance evaluation, we can supply specimens of FDR126Z1, which is identical to the FDR126Z but contains a bit pattern of our own. The FDR126Z requires a two phase clock; the outputs remain steady as long as the address remains unchanged.
The memory matrix is programmed with the aid of a mask pattern during manufacture. The only d.c. supply is the output buffer supply, which is variable and can be biased to drive bipolar output loads direct.
The FDR126Z1 is a pre-programmed version of the FDR126Z READ-ONLY memory. It is intended to convert from ASCII to SELECTRIC line code and vice versa.
When 7-bit address of either code is applied to the inputs of the ROM, the corresponding 7-bits of the other code will appear at the outputs.
The three remaining outputs are used for parity and control code indications.
The electrical characteristics of the FDR126Z1 are equal to those of the FDR126Z.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages on all data inputs, clock inputs, outputs and supply terminals, with reference to P_0		+0.5 to	−30	V
Power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Junction temperature	T_j	max.	150	°C
Storage temperature	T_{stg}	−65 to	+150	°C
Total current through terminal P_1	$-I_{P_1}$	max.	40	mA
Output current (per output)	$\pm I_Q$	max.	20	mA

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	125	°C/W

Note
All terminals are protected against over-voltage caused by static charges.

CHARACTERISTICS at T_{amb} = −55 to +85 °C

ELECTRICAL DRIVE REQUIREMENTS	Symbol	min.	typ.	max.		Conditions and references
Clock rate	f_ϕ	0.01	–	1.0	MHz	
Clock pulse width	$t_{\phi 1L}$	0.60	–	5.0	µs	see timing diagram for parameter definitions
	$t_{\phi 2L}$	0.25	–	5.0	µs	
Clock pulse fall time	$t_{\phi HL}$	–	–	0.10	µs	
Clock pulse rise time	$t_{\phi LH}$	–	–	0.10	µs	
Clock delay time	$t_{\phi 1\phi 2}$	0	–	45	µs	
Clock delay time	$t_{\phi 2\phi 1}$	0	–	45	µs	
Clock input voltage level						
HIGH	$V_{\phi H}$	−2	0	+0.3	V	
LOW	$V_{\phi L}$	−28	−26	−24	V	
Address input and output inhibit input logic levels:						
HIGH	V_{AH}, V_{CH}	−2	0	+0.3	V	
LOW	V_{AL}, V_{CL}	−28	−12	−9	V	

CHARACTERISTICS (continued)

Test conditions: V_{P_1} = −12 V to −14 V; T_{amb} = −55 to +85 °C; P_0 = grounded; standard load: 30 pF in parallel with 150 kΩ to P_0.

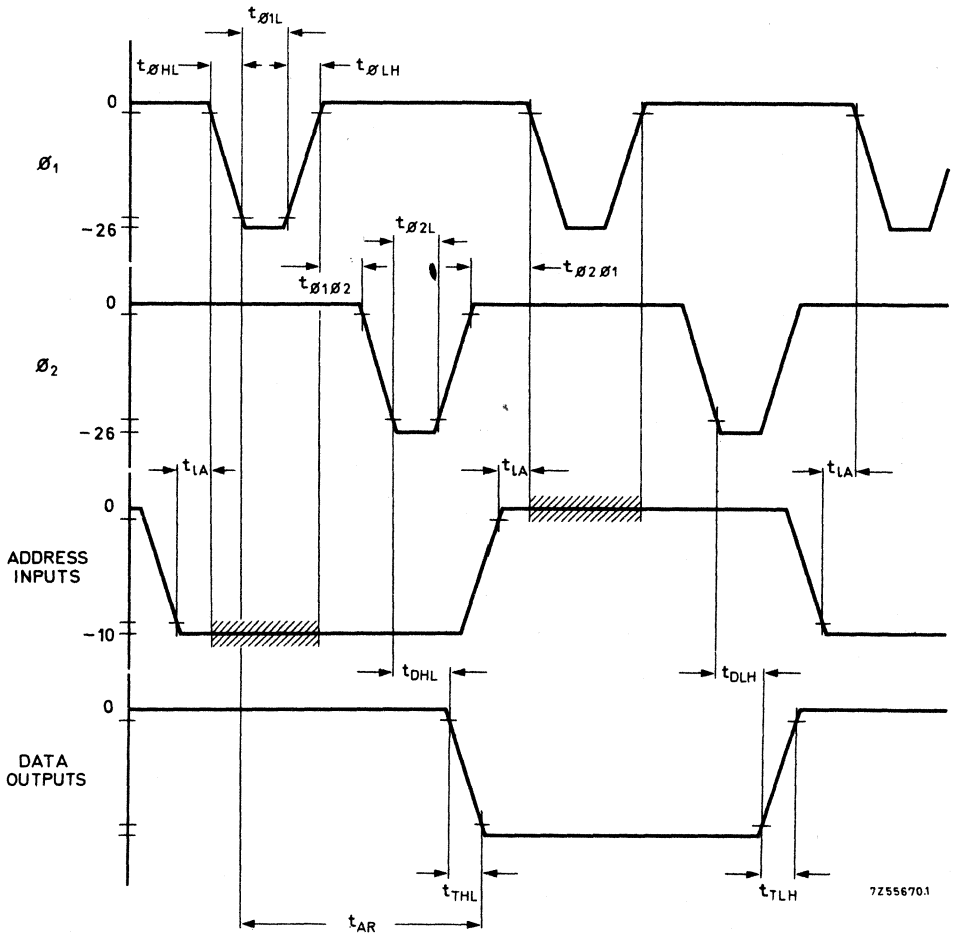
ELECTRICAL DATA	Symbol	min.	typ.	max.		Conditions and references
Read access time	t_{AR}	–	0.75	1	µs	
Output levels:						
HIGH	V_{QH}	−1	–	0	V	
LOW	V_{QL}	−14	–	−10	V	
Address input capacitance	C_A	–	3.6	5.0	pF	bias: V_A = 0 V; f_ϕ = 1 MHz
Output inhibit input capacitance	C_C	–	3.2	4.0	pF	bias: $V_C = V_\phi$ = 0 V; f_ϕ = 1 MHz
Clock input capacitance	$C_{\phi 1}$	–	19	30	pF	bias: $V_C = V_\phi$ = 0 V; f_ϕ = 1 MHz
	$C_{\phi 2}$	–	20	30	pF	bias: $V_C = V_\phi$ = 0 V; f_ϕ = 1 MHz
	$C_{\phi 1}$	–	11	20	pF	bias: V_ϕ = −26 V; f_ϕ = 1 MHz
	$C_{\phi 2}$	–	12	20	pF	bias: V_ϕ = −26 V; f_ϕ = 1 MHz
Leakage currents:						
Address input and output inhibit input currents	$-I_{AL}$, $-I_{CL}$	–	–	1	µA	$V_A = V_C$ = −15 V; all other terminals at V_{P_0}; T_{amb} = 25 °C
Clock input current	$-I_{\phi L}$	–	–	100	µA	V_ϕ = −28 V; all other terminals at V_{P_0}; T_{amb} = 25 °C
Output resistance						
HIGH	R_{QH}	–	400	–	Ω	
LOW	R_{QL}	–	300	–	Ω	V_{P_1} = −5 V
Clock power dissipation (see note 1) ($\phi_1 + \phi_2$)	P_ϕ	–	36	–	mW	f_ϕ = 1 MHz
Supply current (see note 2)	$-I_{P_1}$	–	5.0	–	mA	V_{P_1} = −13 V; f_ϕ = 1 MHz; T_{amb} = 25 °C
Output transition times:						
fall time	t_{THL}	–	100	–	ns	
rise time	t_{TLH}	–	100	–	ns	
Delay times: fall time	t_{DHL}	–	20	–	ns	
rise time	t_{DLH}	–	20	–	ns	
D.C. noise margin	M_L, M_H	1	–	–	V	

Note 1: No d.c. power is dissipated in the decoder or memory matrix; the quoted power dissipation is a.c. only.

Note 2: I_{P_1} is almost entirely dependent on the external load.

CHARACTERISTICS (continued)

TIMING DIAGRAM



Address and output inhibit timing requirements:

1. Address and output inhibit signals are clocked into the memory during ϕ_1, and must remain present throughout ϕ_1. Address and output inhibit lead time ($t_{\ell A}$) must be ≥ 0, during the shaded interval.
2. The output signals remain steady for as many clock cycles as the address and output inhibit signals remain unchanged.

Note:
The indicated points on the vertical axis are specified in the glossary of terms.

CHARACTERISTICS (continued)

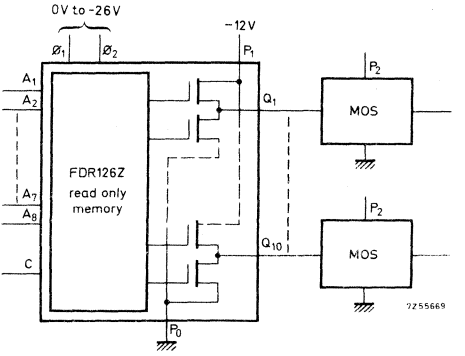
GLOSSARY OF TERMS

1. Clock pulse width: $t_{\phi L}$
   The time for which the clock pulse is LOW; $V_\phi \leq -24$ V.
2. Clock pulse fall time: $t_{\phi HL}$
   The time between the 10% and 90% voltage points as the clock pulse goes from HIGH to LOW.
3. Clock pulse rise time: $t_{\phi LH}$
   The time between the 90% and 10% voltage points as the clock pulse goes from LOW to HIGH.
4. Clock delay time: $t_{\phi 1\phi 2}$; $t_{\phi 2\phi 1}$
   The least allowable time between the end of the ϕ_1 (or ϕ_2) clock pulse and the start of the ϕ_2 (or ϕ_1) clock pulse, defined at −2 V.
5. Fall delay time: t_{DHL}
   After the clock pulse ϕ_2 reaches LOW, the time that elapses before the output starts to change from HIGH to LOW.
6. Rise delay time: t_{DLH}
   After the clock pulse ϕ_2 reaches LOW, the time that elapses before the output starts to change from LOW to HIGH.
7. Output fall transition time: t_{THL}
   The time between the 10% and 90% voltage points as the output goes from HIGH to LOW.
8. Output rise transition time: t_{TLH}
   The time between the 90% and 10% voltage points as the output goes from LOW to HIGH.
9. Output inhibit time: t_{CL}
   The minimum time that the output inhibit signal must be present during ϕ_2 in order to inhibit the output, defined at −2 V.
10. Read access time: t_{AR}
    The time between the 90% point on the leading edge of the clock pulse ϕ_1 and the time at which the output is present.

OUTPUT BUFFER DESCRIPTION

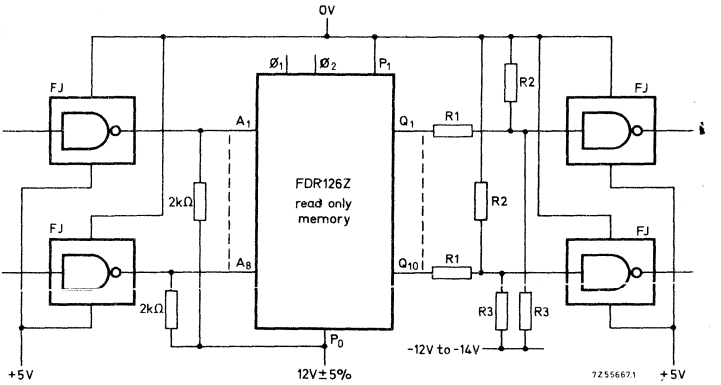
The only d.c. supply required is V_{P_1}, the push-pull output buffer supply. V_{P_1} may be varied between 0 and −28 V according to the output voltage swing required. It does not affect the operating speed of the memory.

1. Biasing circuit A is used when driving MOS loads. Normal MOS input signals must drive the address and inhibit inputs.



Biasing circuit A

2. Biasing circuit B is used when driving TTL loads direct from each output buffer. This circuit allows also to drive MOS circuits direct from TTL. For this purpose special TTL gates are available (FJH301, FJH311 and FJH321), with a guaranteed minimum output breakdown voltage of 15 V.

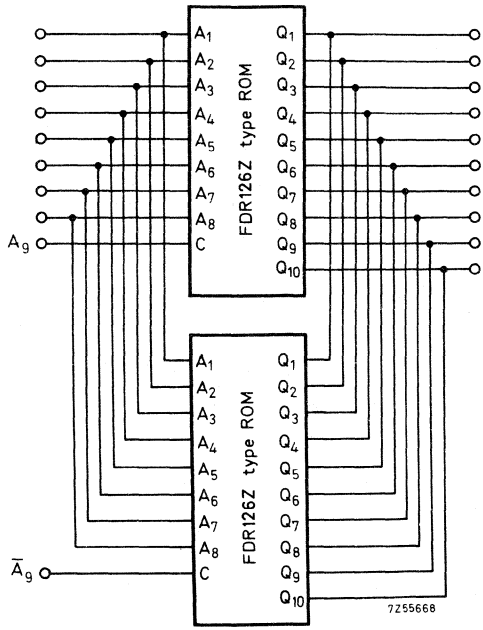


R1 = 820 Ω
R2 = 820 Ω
R3 = 12 kΩ
All resistors: ± 5%

Biasing circuit B

WIRED-OR APPLICATIONS

Use of wired-or output capability:
Applying a LOW signal to the output inhibit leads will cause both of the push pull output transistors associated with each output driver to turn off. Their output impedances are then very high (about 5 MΩ) and they can be wired-or with other ROM output buffers without affecting the output drive capability of any buffer operating in the low impedance mode. This output inhibit wired-or capability makes it possible to use the FDR126Z type ROM in many different applications, such as those shown here. Note that the terminals A9 and $\overline{A9}$ although shown as address inputs, must actually be output inhibit signals synchronous with the address.



PROCEDURE FOR ORDERING A SPECIAL BIT PATTERN

To ensure accuracy when ordering a special bit pattern for a Read Only Memory (ROM) mask, customers should make use of the form on page 12. Four forms are needed for 256 word memories. The completed forms enable us to transfer any desired bit pattern into a standard ROM without error. After receipt of the forms our procedure is as follows:

1. An IBM card is punched for each row of each sheet of the form. (If he prefers to do so, the customer may punch his own cards and supply them to us, provided their format is identical with that of the forms).
2. The punched card are incorporated in a computer program that originates the following:
   - a duplicate of the ordered bit pattern, for verification.
   - a control tape for programming final electrical testing of the customers's ROM.
   - a control tape embodying the ordered pattern of ones and zeros to govern the movement of the automatic plotter used in mask making.
3. The computer print-out is checked against the original order forms; a copy is also sent to the customer for his verification and signature.
4. Upon receipts of the customer's signed verification, full scale masks embodying the desired pattern are made and the unique type number suffix is assigned.

INSTRUCTION FOR COMPLETING THE FORMS

A. Customer block: ON EACH FORM

Enter Name, Date and Authorized Signature in the spaces provided.

B. The ADDRESS INPUTS and CONTENTS

Each page of the ROM Bit Pattern Form is laid out for 64 consecutive words; 16 in each of the four columns (00, 01, 10 and 11).

1. ADDRESS INPUTS
   a) There are nine Address Inputs; the right-hand bit is always bit 1 and is the least significant bit; the left hand bit is bit 9, it is the most significant. The Address Input leads on the ROM package are labelled A_1, A_2, etc., to correspond.
   b) The states of bits 1 to 4 are listed consecutively down the page. The state of bits 5 and 6 are at the head of each of four output columns. The Address Input of 64 consecutive words are thus uniquely specified on each page.
   c) Bits 7, 8 and 9 (or bits 7 and 8 only, for 256 word memories) specify sets of memory locations, 1 set of 64 words per page. These spaces should be filled by the customer using a consecutive full binary code. The first position on page 1 of your specification should be three (or two) zeros. [1]
   Memories of 256 words need 4 pages, of specifications.
   d) Only ones (1 = LOW) or zeros (0 = HIGH) should be used in completing the form except where, as with 256 word memories, column 9 is unused and is, therefore, left blank.

[1]) See example on page 12.

2. CONTENTS (DATA OUTPUTS)
   a) Each column has provision for words of 10 bits numbered 1 to 10, bit 1 is always the right-hand bit. The output leads of the ROM package are labelled Q_1, Q_2, etc., to correspond.
   b) The requisite bit pattern should be inserted under headings 1 to 10 using only ones (1 = LOW) and zeros (0 = HIGH), except where a column is unused and is, therefore, left blank.

3. AUTHORIZED SIGNATURE
   Having completed the bit pattern, the customer should check that the forms are numbered, dated, and signed, as they constitute formal evidence of his request. In the event that the customer provides his own punched cards the signature on the computer duplicate will serve as formal evidence.

PHILIPS
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Integrated Circuits

Read Only Memory Bit Pattern FDR 126 ...

page of

AUTHORIZED SIGNATURE

CUSTOMER NAME:

DATE

ADDRESS INPUTS	CONTENTS			
	00	01	10	11
9 8 7 6 5 4 3 2 1	10 9 8 7 6 5 4 3 2 1	10 9 8 7 6 5 4 3 2 1	10 9 8 7 6 5 4 3 2 1	10 9 8 7 6 5 4 3 2 1
	OUTPUTS	OUTPUTS	OUTPUTS	OUTPUTS
1 2 3 4 5 6 7	8 9 10 11 12 13 14 15 16 17	18 19 20 21 22 23 24 25 26 27	28 29 30 31 32 33 34 35 36 37	38 39 40 41 42 43 44 45 46 47
X X 0 0 0 0				
X X 0 0 0 1				
X X 0 0 1 0				
X X 0 0 1 1				
X X 0 1 0 0				
X X 0 1 0 1				
X X 0 1 1 0				
X X 0 1 1 1				
X X 1 0 0 0				
X X 1 0 0 1				
X X 1 0 1 0				
X X 1 0 1 1				
X X 1 1 0 0				
X X 1 1 0 1				
X X 1 1 1 0				
X X 1 1 1 1				

Note: 1 = LOW; 0 = HIGH

GENERAL DESCRIPTION of FDR126Z1

The FDR126Z1 is a version of the FDR126Z pre-programmed to convert from ASCII to SELECTRIC line code and vice versa.
When any 7-bit address of either code is presented to the input the FDR126Z1 will deliver the corresponding word at its output.
The direction of conversion is selected with the eighth address input.
The correspondence between code bits and inputs and outputs is shown in the table below.

address input	ASCII bit	SELECTRIC bit	output
A_1	b_1	1	Q_1
A_2	b_2	2	Q_2
A_3	b_3	4	Q_3
A_4	b_4	8	Q_4
A_5	b_5	A	Q_5
A_6	b_6	B	Q_6
A_7	b_7	S	Q_7

A_8 = LOW: conversion from SELECTRIC line code to ASCII.

A_8 = HIGH: conversion from ASCII to SELECTRIC line code.

Output Q_8 adds an odd parity bit to the 7-bit output code on Q_1 to Q_7 (see note).

Output Q_9 LOW indicates odd parity at the input.

Comparison of the Q_9 output with the parity bit added to the input word indicates whether or not the input code is correct.

If Q_{10} is LOW, the word on outputs Q_1 to Q_7 is a line control code.

Note:
$\overline{1}$ = LOW; 0 = HIGH

ASCII CODE

b7 → / b6 → / b5 →		0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
b4 b3 b2 b1 ↓	column → / row ↓	0	1	2	3	4	5	6	7
0 0 0 0	0	NUL / IL1	DLE / PRE2	SPACE / SPACE1	0 / 0	@ / @	P / P	\ / |	p / p
0 0 0 1	1	SOH / b	DC1 / RS2	! / !	| / |	A / A	Q / Q	a / a	q / q
0 0 1 0	2	STX / 9	DC2 / PN1	" / "	2 / 2	B / B	R / R	b / b	r / r
0 0 1 1	3	ETX / EOB1	DC3 / RS1	# / #	3 / 3	C / C	S / S	c / c	s / s
0 1 0 0	4	EOT / EOT1	DC4 / PF1	$ / $	4 / 4	D / D	T / T	d / d	t / t
0 1 0 1	5	ENQ / UC2	NAK / !	% / %	5 / 5	E / E	U / U	e / e	u / u
0 1 1 0	6	ACK / -	SYN / IL2	& / &	6 / 6	F / F	V / V	f / f	v / v
0 1 1 1	7	BEL / LC1	ETB / EOB2	/ / |	7 / 7	G / G	W / W	g / g	w / w

Note: 1 = LOW; 0 = HIGH

ASCII CODE (continued)

b7 → b6 → b5 →		0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
b4 ↓ b3 ↓ b2 ↓ b1 ↓	column → / row ↓	0	1	2	3	4	5	6	7
1 0 0 0	8	BS / BS1	CAN / !	(/ (	8 / 8	H / H	X / X	h / h	x / x
1 0 0 1	9	HT / HT1	EM / RES1	) /)	9 / 9	I / I	Y / Y	i / i	y / y
1 0 1 0	10	LF / LF1	SUB / BY1	* / *	: / :	J / J	Z / Z	j / j	z / z
1 0 1 1	11	VT / ②	ESC / PRE1	+ / +	; / ;	K / K	[/ ±	k / k	[/ ±
1 1 0 0	12	FF / ⑤	FS / BY2	, / ,	< / o	L / L	\ / ±	! / !	: / ±
1 1 0 1	13	CR / NL1	GS / RES2	- / -	= / =	M / M	] / ±	m / m	] / ±
1 1 1 0	14	SO / UC1	RS / RES2	. / .	> / ¢	N / N	^ / ±	n / n	~ / ±
1 1 1 1	15	SI / LC2	US / BY2	/ / /	? / ?	O / O	- / -	o / o	DEL / DEL1

Note: 1 = LOW; 0 = HIGH

SELECTRIC LINE CODE TO ASCII CODE CORRESPONDENCE

S → B → A →		0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
8 4 2 1 ↓	column → / row ↓	0	1	2	3	4	5	6	7
0 0 0 0	0	SPACE1 / SPACE	t / t	! / !	j / j	SPACE2 / SPACE	T / T	o / <	J / J
0 0 0 1	1	1 / 1	x / x	m / m	g / g	± /]	X / X	M / M	G / G
0 0 1 0	2	2 / 2	n / n	. / .	= / =	@ / @	N / N	. / .	+ / +
0 0 1 1	3	3 / 3	u / u	v / v	f / f	# / #	U / U	V / V	F / F
0 1 0 0	4	5 / 5	e / e	| / /	p / p	% / %	E / E	" / "	P / P
0 1 0 1	5	7 / 7	d / d	r / r	; / ;	& / &	D / D	R / R	: / :
0 1 1 0	6	6 / 6	k / k	i / i	q / q	¢ / >	K / K	I / I	Q / Q
0 1 1 1	7	8 / 8	c / c	a / a	, / ,	* / *	C / C	A / A	, / ,

Note: 1 = LOW; 0 = HIGH

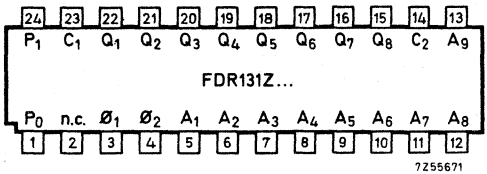
SELECTRIC LINE CODE TO ASCII CODE CORRESPONDENCE (continued)

S → B → A →		0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
8 4 2 1 ↓	column → / row ↓	0	1	2	3	4	5	6	7
1 0 0 0	8	4 / 4	| / |	o / o	/ / /	$ / $	L / L	O / O	? / ?
1 0 0 1	9	0 / 0	h / h	s / s	y / y	) /)	H / H	S / S	Y / Y
1 0 1 0	10	z / z	① / RS	② / VT	③ / RS	Z / Z	④ / RS	⑤ / FF	⑥ / RS
1 0 1 1	11	9 / 9	b / b	w / w	- / -	(/ (	B / B	W / W	- / -
1 1 0 0	12	PN1 / DC2	BY1 / SUB	RES1 / EM	PF1 / DC4	PN2 / DC2	BY2 / FS	RES2 / GS	PF2 / DC4
1 1 0 1	13	RS1 / DC3	LF1 / LF	NL1 / CR	HT1 / HT	RS2 / DC1	LF2 / LF	NL2 / CR	HT2 / HT
1 1 1 0	14	UC1 / SO	EOB1 / ETX	BS1 / BS	LC1 / BEL	UC2 / ENQ	EOB2 / ETB	BS2 / BS	LC2 / SI
1 1 1 1	15	EOT1 / EOT	PRE1 / ESC	IL1 / NUL	DEL1 / DEL	EOT2 / EOT	PRE2 / DLE	IL2 / NUL	DEL2 / NUL

Note: 1 = LOW; 0 = HIGH

The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enchancement mode technology.

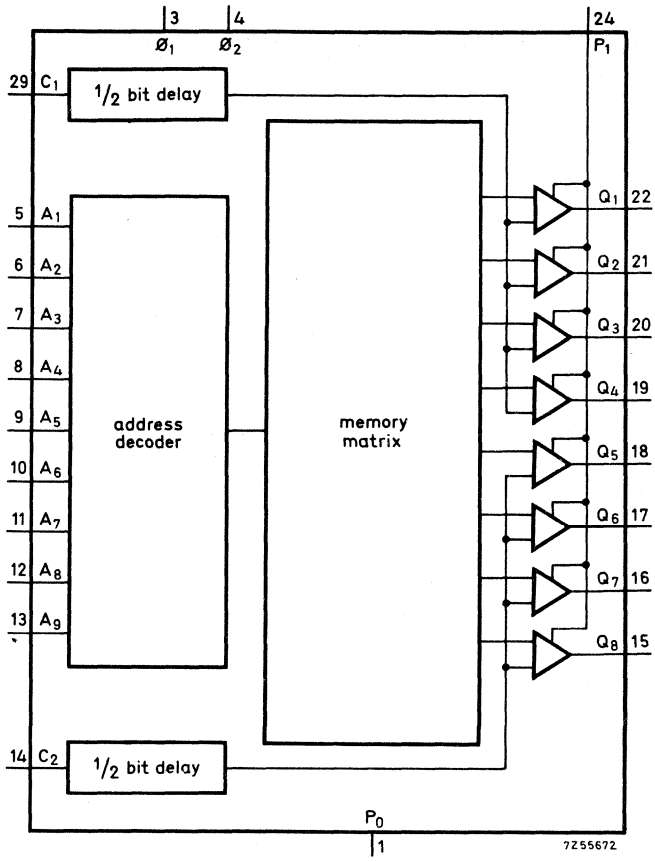
READ ONLY MEMORY, 512 WORD, 8 BITS PER WORD



P_0 and metal lid on bottom of the package are connected

QUICK REFERENCE DATA			
Read access time	t_{AR}	max. 1.5	µs
Clock rate	f_ϕ	max. 0.66	MHz
Power dissipation (MOS load)	P_{tot}	typ. 100	mW
D.C. noise margin	M_H, M_L	> 1.0	V
Operating ambient temperature	T_{amb}	0 to 70	°C

PACKAGE OUTLINE 24 lead ceramic dual in-line. (See page 18)


3
4
24
Ø1
Ø2
P1
29 C1
1/2 bit delay
5 A1
6 A2
7 A3
8 A4
9 A5
10 A6
11 A7
12 A8
13 A9
address decoder
memory matrix
Q1 22
Q2 21
Q3 20
Q4 19
Q5 18
Q6 17
Q7 16
Q8 15
14 C2
1/2 bit delay
P0
1
7Z55672

GENERAL DESCRIPTION

The FDR131Z is a monolithic 4096-bit READ-only memory (ROM) with a capacity of 512 words, 8 bits per word. With two output-inhibit control lines C_1 and C_2 it can also operate as a 1024-word, 4 bits per word memory. The memory matrix is given the desired content by means of a special mask. When ordering, customers have to complete a set of forms specifying the bit pattern to be associated with each address. The output-inhibit control make it possible to use several FDR131Z memories in wired-OR configuration.
The only d.c. supply is the output buffer supply (P_1), which may be adapted to interface direct with either MOS or bipolar DTL/TTL. All terminals of the FD circuits are effectively protected against over voltage caused by static charge.
A pre-programmed specimen of the FDR131Z is the FDR131Z1 given on page 14.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages on all data inputs, clock inputs, outputs and supply terminals, with reference to P_0		+0.5 to −30		V
Power dissipation up to $T_{amb} = 25\,^{o}C$	P_{tot}	max.	1	W
Junction temperature	T_j	max.	150	^{o}C
Storage temperature	T_{stg}	−65 to +150		^{o}C
Total current through terminal P_1	$-I_{P1}$	max.	40	mA
Output current (per output)	$\pm I_Q$	max.	20	mA

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	125	$^{o}C/W$

CHARACTERISTICS at T_{amb} = 0 to +70 °C

ELECTRICAL DRIVE REQUIREMENTS	Symbol	min.	typ.	max.		Conditions and references
Clock rate	f_ϕ	0.1	–	0.66	MHz	(see note)
Clock pulse width	$t_{\phi 1L}$	0.90	–	2.0	µs	see timing diagram for parameter definitions
	$t_{\phi 2L}$	0.35	–	2.0	µs	
Clock pulse rise time (ϕ_1, ϕ_2)	$t_{\phi LH}$	–	–	1.0	µs	See note
Clock pulse fall time	$t_{\phi 1HL}$	0.165	–	1.0	µs	
	$t_{\phi 2HL}$	–	–	1.0	µs	
Clock delay time	$t_{\phi 1\phi 2}$	0	–	4.5	µs	
Clock delay time	$t_{\phi 2\phi 1}$	0	–	4.5	µs	
Clock input voltage level						
HIGH	$V_{\phi H}$	−2	0	+0.3	V	
LOW	$V_{\phi L}$	−28	−26	−24	V	
Address input and output inhibit input logic levels:						
HIGH	V_{AH}, V_{CH}	−2	0	+0.3	V	
LOW	V_{AL}, V_{CL}	−14	−12	−9	V	

Note:
At frequencies higher than 191 kHz the maximum clock pulse rise and fall times will be determined by the minimum ϕ_1 and ϕ_2 pulse width.

CHARACTERISTICS

Test conditions: V_{P1} = −12 V to −14 V; T_{amb} = 0 to +70 °C; P_0 = grounded; standard load: 30 pF in parallel with 150 kΩ to P_0.

ELECTRICAL DATA	Symbol	min.	typ.	max.		Conditions and references
Read access time	t_{AR}	–	1.2	1.5	µs	see note 1
Output levels:						
HIGH	V_{QH}	−1	–	0	V	
LOW	V_{QL}	−14	–	−10	V	
Address input and output inhibit input capacitances	C_A, C_C	–	3.2	4.0	pF	bias: $V_A = V_C$ = 0 V; f_ϕ = 1 MHz
Clock input capacitance	$C_{\phi 1}$	–	18	22	pF	bias: V_ϕ = 0 V; f_ϕ = 1 MHz
	$C_{\phi 2}$	–	16	20	pF	
	$C_{\phi 1}$	–	11	14	pF	bias: V_ϕ = −26 V; f_ϕ = 1 MHz
	$C_{\phi 2}$	–	9.5	12	pF	
Leakage currents:						
Address input and output inhibit input currents	$-I_{AL}$, $-I_{CL}$	–	–	1	µA	$V_A = V_C$ = −15 V; all other terminals at V_{P0}; T_{amb} = 25 °C
Clock input current	$-I_{\phi L}$	–	–	100	µA	V_ϕ = −28 V; all other terminals at V_{P0}; T_{amb} = 25 °C
Output resistance						
HIGH	R_{QH}	–	500	–	Ω	
LOW	R_{QL}	–	350	–	Ω	V_{P1} = −5 V
Clock power dissipation (see note 2) ($\phi_1 + \phi_2$)	P_ϕ	–	36	–	mW	f_ϕ = 1 MHz
Supply current (see note 3)	$-I_{P1}$	–	4.0	–	mA	V_{P1} = −13 V; f_ϕ = 1 MHz; T_{amb} = 25 °C
Output transition times:						
fall time	t_{THL}	–	200	–	ns	
rise time	t_{TLH}	–	200	–	ns	
Delay times: fall time	t_{DHL}	–	20	–	ns	
rise time	t_{DLH}	–	20	–	ns	
D.C. noise margin	M_L, M_H	1	–	–	V	

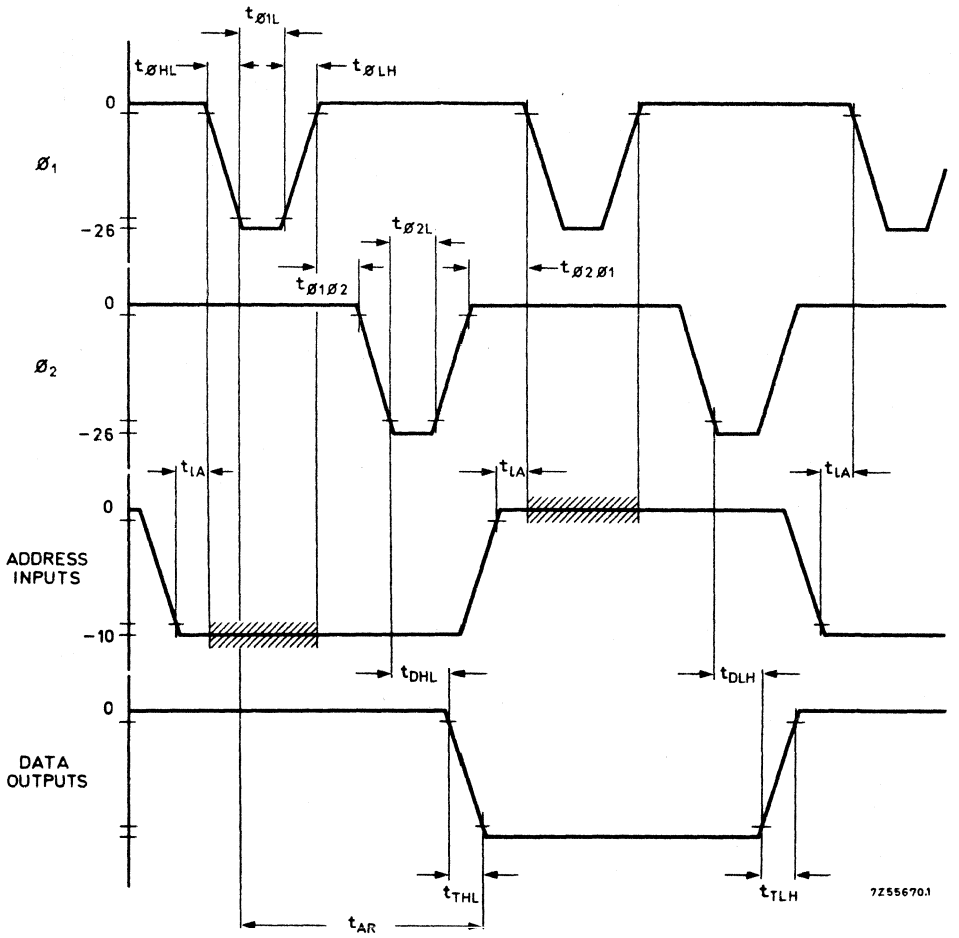
Note 1: Assuming the fall time of ϕ_1 and rise time of ϕ_2 is less than 40 ns.

Note 2: No d.c. power is dissipated in the decoder or memory matrix; the quoted power dissipation is a.c. only.

Note 3: I_{P1} is almost entirely dependent on the external load.

CHARACTERISTICS (continued)

TIMING DIAGRAM



Address and output inhibit requirements:

1. Address and output inhibit signals are clocked into the memory during $\phi 1$, and must remain present during the shaded interval. Address lead time ($t_{\ell A}$) must be ≥ 0.
2. The output signals remain steady when the address and output inhibit signals remain unchanged.

Note:

The indicated points on the vertical axis are specified in the glossary of terms.

CHARACTERISTICS (continued)

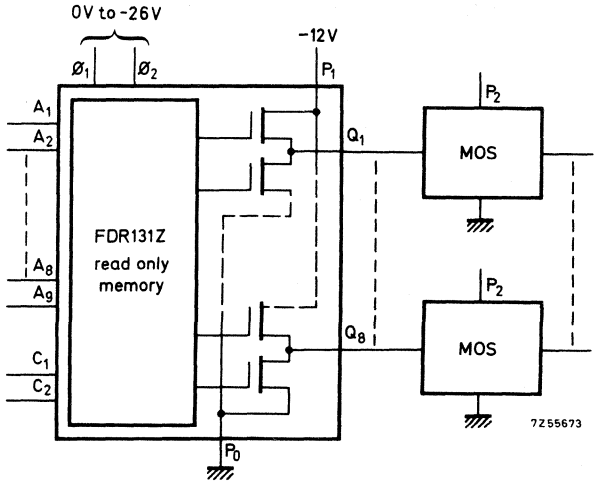
GLOSSARY OF TERMS

1. Clock pulse width: $t_{\phi L}$
   The time for which the clock pulse is LOW; $V_{\phi} \leq -24$ V
2. Clock pulse fall time: $t_{\phi HL}$
   The time between the 10% and 90% voltage points as the clock pulse goes from HIGH to LOW.
3. Clock pulse rise time: $t_{\phi LH}$
   The time between the 90% and 10% voltage points as the clock pulse goes from LOW to HIGH.
4. Clock delay time: $t_{\phi 1 \phi 2}$; $t_{\phi 2 \phi 1}$
   The least allowable time between the end of the ϕ_1 (or ϕ_2) clock pulse and the start of the ϕ_2 (or ϕ_1) clock pulse, defined at -2 V.
5. Fall delay time: t_{DHL}
   After the clock pulse ϕ_2 reaches LOW, the time that elapses before the output start to change from HIGH to LOW.
6. Rise delay time: t_{DLH}
   After the clock pulse ϕ_2 reaches LOW, the time that elapses before the output starts to change from LOW to HIGH.
7. Output fall transition time: t_{THL}
   The time between the 10% and 90% voltage points as the output goes from HIGH to LOW.
8. Output rise transition time: t_{TLH}
   The time between the 90% and 10% voltage points as the output goes from LOW to HIGH.
9. Read acces time: t_{AR}
   The time between the 90% point on the leading edge of the clock pulse ϕ_1 and the time at which the output is present, defined at 90%.

OUTPUT BUFFER DESCRIPTION

The only d.c. supply required is V_{P_1}, the push-pull output buffer supply. V_{P_1} may be varied between 0 and −28 V according to the output voltage swing required. It does not affect the operating speed of the memory.

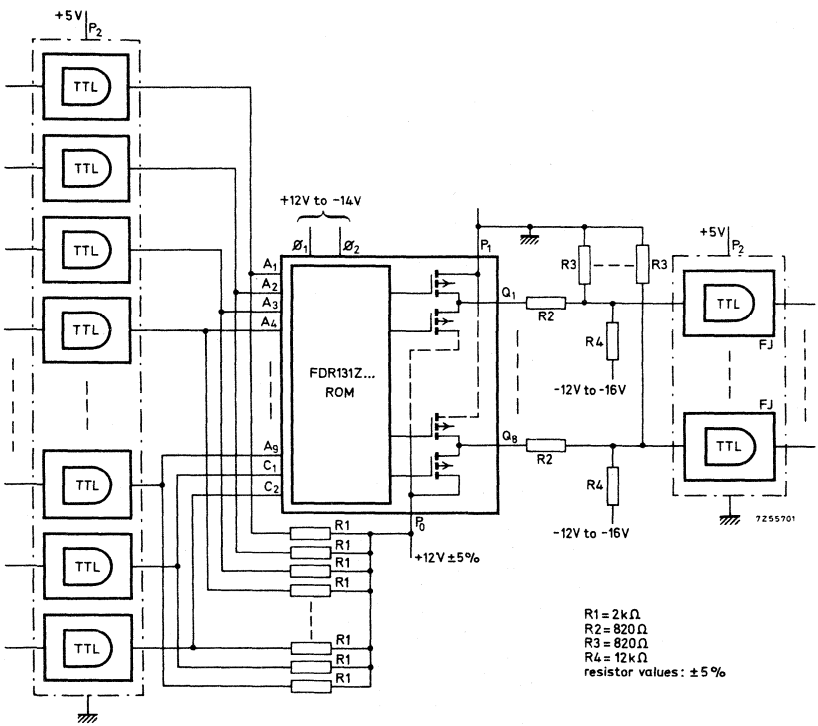
1. Biasing circuit A is used when driving MOS loads. Normal MOS input signals must drive the address and inhibit inputs.



Biasing circuit A

OUTPUT BUFFER DESCRIPTION (continued)

2. Biasing circuit B is used to interface direct with TTL on both the inputs and outputs of the READ-only memory. No active interface components are required. The TTL circuits on the inputs of the ROM must be able to sustain at least +12 V at their outputs.
   The quadruple NAND gate FJH301 and the sextuple inverter FJH321 are especially manufactured with a guaranteed breakdown voltage of 15 V for this purpose.

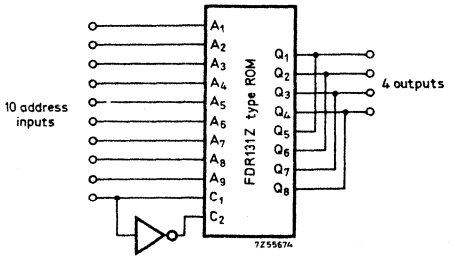


WIRED-OR APPLICATIONS

Use of wired-or output capability:
Applying a LOW signal to the output inhibit leads will cause both of the push pull output transistors associated with each output driver to turn off. Their output impedances are then very high (about 5 MΩ) and they can be wired-or with other ROM output buffers without affecting the output drive capability of any buffer operating in the low impedance mode. C_1 controls output buffers 1 to 4, and C_2 controls output buffers 5 to 8. This output inhibit wired-or capability makes it possible to use the FDR131Z type ROM in many different applications, such as those shown here.

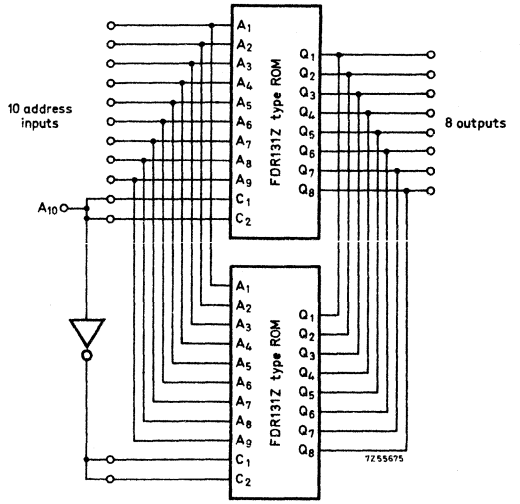
1024 words

4-bits per word



1024 words

8-bits per word



PROCEDURE FOR ORDERING A SPECIAL BIT PATTERN

To ensure accuracy when ordering a special bit pattern for a Read Only Memory (ROM) mask, customers should make use of the form on page 13. Eight forms are needed for 512 word memories. The completed forms enable us to transfer any desired bit pattern into a standard ROM without error. After receipt of the forms our procedure is as follows:

1. An IBM card is punched for each row of each sheet of the form. (If he prefers to do so, the customer may punch his own cards and supply them to us, provided their format is identical with that of the forms).
2. The punched cards are incorporated in a computer program that originates the following:
   - a duplicate of the ordered bit pattern, for verification.
   - a control tape for programming final electrical testing of the customer's ROM.
   - a control tape embodying the ordered pattern of ones and zeros to govern the movement of the automatic plotter used in mask making.
3. The computer print-out is checked against the original order forms; a copy is also sent to the customer for his verification and signature.
4. Upon receipts of the customer's signed verification, full scale masks embodying the desired pattern are made and the unique type number suffix is assigned.

INSTRUCTION FOR COMPLETING THE FORMS

A. Customer block: ON EACH FORM

Enter Name, Date and Authorized Signature in the spaces provided.

B. The ADDRESS INPUTS and CONTENTS

Each page of the ROM Bit Pattern Form is laid-out for 64 consecutive words; 16 in each of the four columns (00, 01, 10 and 11).

1. ADDRESS INPUTS
   a) There are nine Address Inputs; the right-hand bit is always bit 1 and is the least significant bit; the left-hand bit is 9, it is the most significant. The Address Input leads on the ROM package are labelled A_1, A_2, etc., to correspond.
   b) The states of bits 1 to 4 are listed consecutively down the page. The state of bits 5 and 6 are at the head of each of four output columns. The Address Input of 64 consecutive words are thus uniquely specified on each page.
   c) Bit 7, 8, and 9 (or bits 7 and 8 only, for 256 word memories) specify sets of memory locations, 1 set of 64 words per page. These spaces should be filled by the customer using a consecutive full binary code. The first position on page 1 of your specification should be three (or two) zeros. [1]
   Memories of 256 words need 4 pages, of specifications.
   d) Only ones (1 = LOW) or zeros (0 = HIGH) should be used in completing the form except where, a column is unused and is, therefore, left blank.

[1]) See example on page 13

2. CONTENTS (DATA OUTPUTS)
   a) Each column has provision for words of 10 bits numbered 1 to 10, bit 1 is always the right-hand bit. The output leads of the ROM package are labelled Q_1, Q_2, etc., to correspond.
   b) The requisite bit pattern should be inserted under headings 1 to 10 using only ones (1 = LOW) and zeros (0 = HIGH), except where a column is unused and is, therefore, left blank.

3. AUTHORIZED SIGNATURE
   Having completed the bit pattern, the customer should check that the forms are numbered, dated, and signed, as they constitute formal evidence of his request. In the event that the customer provides his own punched cards the signature on the computer duplicate will serve as formal evidence.

Note: 1 = LOW; 0 = HIGH

PHILIPS
Electronic Components
and Materials
Integrated Circuits

Read Only Memory Bit Pattern FDR 131...

page of

AUTHORIZED SIGNATURE

CUSTOMER NAME:

DATE

ADDRESS INPUTS	CONTENTS			
	00	01	10	11
9 8 7 6 5 4 3 2 1	OUTPUTS	OUTPUTS	OUTPUTS	OUTPUTS
	10 9 8 7 6 5 4 3 2 1	10 9 8 7 6 5 4 3 2 1	10 9 8 7 6 5 4 3 2 1	10 9 8 7 6 5 4 3 2 1
X X 0 0 0 0				
X X 0 0 0 1				
X X 0 0 1 0				
X X 0 0 1 1				
X X 0 1 0 0				
X X 0 1 0 1				
X X 0 1 1 0				
X X 0 1 1 1				
X X 1 0 0 0				
X X 1 0 0 1				
X X 1 0 1 0				
X X 1 0 1 1				
X X 1 1 0 0				
X X 1 1 0 1				
X X 1 1 1 0				
X X 1 1 1 1				

GENERAL DESCRIPTION of FDR131Z1

The FDR131Z1 is a version of the FDR131Z pre-programmed to convert from ASCII to EBCDIC and vice versa.
When the standard 7-bit ASCII code plus parity is presented to address inputs A_1 to A_8, the FDR131Z1 will deliver the corresponding 8-bit EBCDIC code at its outputs, when the A_9 input is HIGH. Conversely, when the standard 8-bit EBCDIC code is presented to inputs A_1 to A_8, the corresponding ASCII code plus parity will be delivered at the outputs when A_9 is LOW. The code conversion circuits from ASCII to EBCDIC are provided in duplicate to accomodate either odd or even parity. The correspondence between code bits and inputs and outputs is shown in the tables below and on the following pages.

Conversion from ASCII to EBCDIC

ASCII-bits	ROM inputs [1]	ROM outputs	EBCDIC-bits
b_1 (least significant bit)	A_1	Q_1	7 (least significant bit)
b_2	A_2	Q_2	6
b_3	A_3	Q_3	5
b_4	A_4	Q_4	4
b_5	A_5	Q_5	3
b_6	A_6	Q_6	2
b_7 (most significant bit)	A_7	Q_7	1
b_8 (odd or even paratity)	A_8	Q_8	0 (most significant bit)

Correspondence of ASCII(A) to EBCDIC(E) code

To find the 7-bit ASCII code for a particular symbol, (see table on page 15) write down the binary coded decimal number belonging to that symbol; e.g., the number belonging to the letter g is 103, which means that the corresponding binary digits for bits b_7 to b_1 of the ASCII code are 1100111.

[1] Condition: A_9 is HIGH

Correspondence of ASCII(A) to EBCDIC(E) code (continued)

	0-15		16-31		32-47		48-63		64-79		80-95		96-111		112-127	
	A	E	A	E	A	E	A	E	A	E	A	E	A	E	A	E
0	NUL	NUL	DLE	DLE	SP	SP	0	0	@	@	P	P	\	¦	p	p
1	SOH	SOH	DC1	DC1	!	!	1	1	A	A	Q	Q	a	a	q	q
2	STX	STX	DC2	DC2	"	"	2	2	B	B	R	R	b	b	r	r
3	ETX	ETX	DC3	DC3	#	#	3	3	C	C	S	S	c	c	s	s
4	EOT	EOT	DC4	DC4	$	$	4	4	D	D	T	T	d	d	t	t
5	ENQ	ENQ	NAK	NAK	%	%	5	5	E	E	U	U	e	e	u	u
6	ACK	ACK	SYN	SYN	&	&	6	6	F	F	V	V	f	f	v	v
7	BEL	BEL	ETB	EOB	´	'	7	7	G	G	W	W	g	g	w	w
8	BS	BS	CAN	CAN	(	(	8	8	H	H	X	X	h	h	x	x
9	HT	HT	EM	EM	)	)	9	9	I	I	Y	Y	i	i	y	y
10	LF	LF	SUB	SUB	*	*	:	:	J	J	Z	Z	j	j	z	z
11	VT	VT	ESC	PRE	+	+	;	;	K	K	[	(	k	k	{	(
12	FF	FF	FS	IFS	,	,	<	<	L	L	\	/	l	l	:	¦
13	CR	CR	GS	IGS	-	-	=	=	M	M	]	)	m	m	]	)
14	SO	SO	RS	IRS	.	.	>	>	N	N	^	¬	n	n	~	¢
15	SI	SI	US	IUS	/	/	?	?	O	O	_	_	o	o	DEL	DEL

Explanation of symbols

NUL = null
SOH = start of heading
STX = start of text
ETX = end of text
EOT = end of transmission
ENQ = enquiry
ACK = acknowledge
BEL = bell
BS = backspace
HT = horizontal tab
FF = form-feed
CR = carriage return
SO = shift out
SI = shift in

DLE = data link escape
DC1 to DC4 = device control
NAK = negative acknowledge
SYN = synchronous idle
ETB = end of transmission block
CAN = cancel
EM = end of medium
SUB = substitute
ESC = escape
FS = file separator
GS = group separator
RS = record separator
US = unit separator
DEL = delete (rub out)

The ASCII to EBCDIC characters for which there was no correspondence have been converterd as follows:

128-ASCII	256-EBCDIC
[	(
\	/
]	)
^	¬

128-ASCII	256-EBCDIC
\	¦ 1)
{	(
}	)
~	¢

1) The EBCDIC to ASCII is ' to ´

Conversion from EBCDIC to ASCII

When the standard 8-bit EBCDIC code is presented to inputs A_1 to A_8, the corresponding ASCII code plus parity will be delivered at the outputs when A_9 is LOW.

EBCDIC-bits	ROM-inputs [1])	ROM-outputs	ASCII-bits
7 (least significant bit)	A_1	Q_1	b_1 (least significant bit)
6	A_2	Q_2	b_2
5	A_3	Q_3	b_3
4	A_4	Q_4	b_4
3	A_5	Q_5	b_5
2	A_6	Q_6	b_6
1	A_7	Q_7	b_7 (most significant bit)
0 (most significant bit)	A_8	Q_8	b_8 (even parity)

Correspondence of EBCDIC to ASC II code

	0-15		16-31		32-47		48-63		64-79		80-95		96-111		112-127	
	E	A	E	A	E	A	E	A	E	A	E	A	E	A	E	A
0	NUL	NUL	DLE	DLE	DS	–	–	–	SP	SP	&	&	–	–	–	–
1	SOH	SOH	DC1	DC1	SOS	–	–	–	–	–	–	–	/	/	–	–
2	STX	STX	DC2	DC2	FS	–	SYN	SYN	–	–	–	–	–	–	–	–
3	ETX	ETX	DC3	DC3	–	–	–	–	–	–	–	–	–	–	–	–
4	PF	–	RES	–	BYP	–	PN	–	–	–	–	–	–	–	–	–
5	HT	HT	NL	–	LF	LF	RS	–	–	–	–	–	–	–	–	–
6	LC	–	BS	BS	EOB	ETB	VC	–	–	–	–	–	–	–	–	–
7	DEL	DEL	IL	–	PRE	ESC	EOT	EOT	–	–	–	–	–	–	–	–
8	–	–	CAN	CAN	–	–	–	–	–	–	–	–	–	–	–	–
9	–	–	EM	EM	–	–	–	–	–	–	–	–	–	–	–	–
10	SMM	–	CC	–	SM	–	–	–	¢	–	!	!	–	–	:	:
11	VT	VT	–	–	–	–	–	–	.	.	$	$	,	,	#	#
12	FF	FF	IFS	FS	–	–	DC4	DC4	<	<	*	*	%	%	@	@
13	CR	CR	IGS	GS	ENQ	ENQ	NAK	NAK	(	(	)	)	–	–	,	'
14	SO	SO	IRS	RS	ACK	ACK	–	–	+	+	;	;	>	>	=	=
15	SI	SI	IUS	US	BEL	BEL	SUB	SUB	|	:	¬	–	?	?	"	"

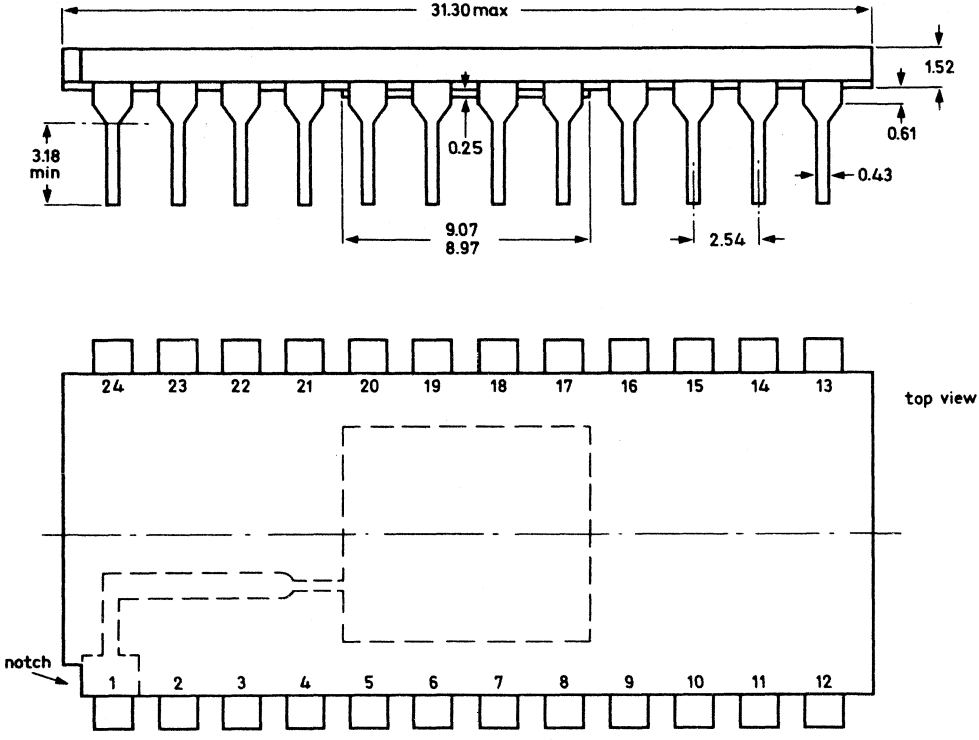
1) Condition: A_9 = LOW

Correspondence of EBCDIC to ASCII code (continued)

To find the 8-bit EBCDIC code for a particular symbol (see table below and on page 16), write down the decimal number belonging to that symbol; e.g., the number belonging to the letter g is 135, which means the corresponding number for the bit positions 0 to 7 of the EBCDIC code is 10000111.

128-143		144-159		160-175		176-191		192-207		208-223		224-239		240-255	
E	A	E	A	E	A	E	A	E	A	E	A	E	A	E	A
–	–	–	–	–	–	–	–	–	–	–	–	–	–	0	0
a	a	j	j	–	–	–	–	A	A	J	J	–	–	1	1
b	b	k	k	s	s	–	–	B	B	K	K	S	S	2	2
c	c	l	l	t	t	–	–	C	C	L	L	T	T	3	3
d	d	m	m	u	u	–	–	D	D	M	M	U	U	4	4
e	e	n	n	v	v	–	–	E	E	N	N	V	V	5	5
f	f	o	o	w	w	–	–	F	F	O	O	W	W	6	6
g	g	p	p	x	x	–	–	G	G	P	P	X	X	7	7
h	h	q	q	y	y	–	–	H	H	Q	Q	Y	Y	8	8
i	i	r	r	z	z	–	–	I	I	R	R	Z	Z	9	9
–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–

PACKAGE OUTLINE 24 lead metal-ceramic dual in-line

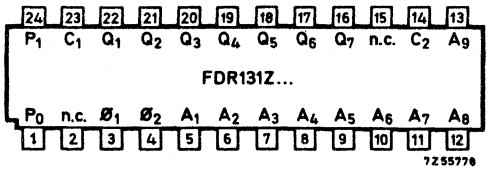


Notes

1. Leads on opposite sides are designed to fit in holes 15.24 mm apart.
2. Pin 1 is marked by a notch and connected to the metal lid on the bottom of the package.

The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enhancement mode technology.

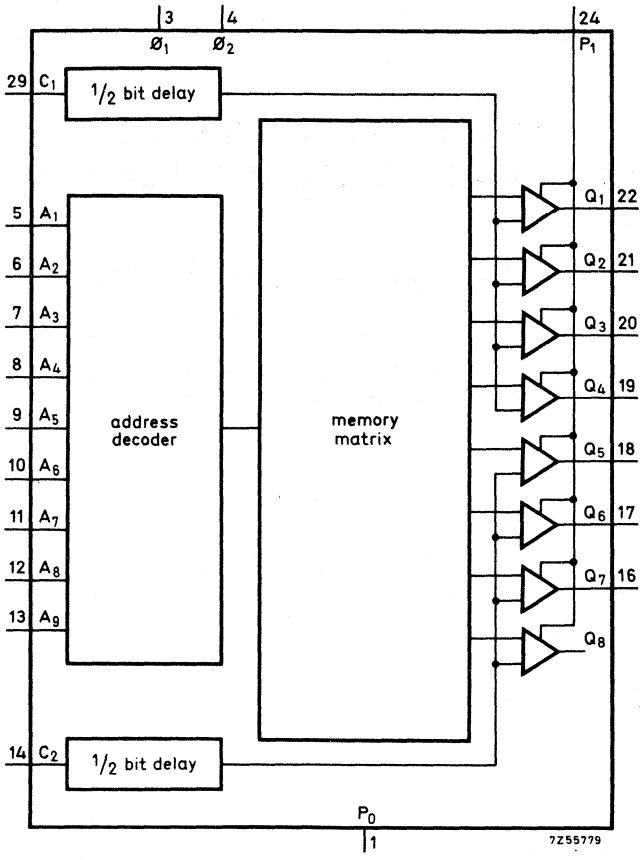
CHARACTER GENERATOR (5 × 7 DOT MATRIX; COLUMN SCAN SYSTEM)



P_0 and metal lid on bottom of the package are connected

QUICK REFERENCE DATA				
Read access time	t_{AR}	max.	1.5	µs
Clock rate	f_ϕ	max.	0.67	MHz
Power dissipation at f_ϕ = 0.67 MHz	P_{av}	typ.	90	mW
D.C. noise margin	M_H, M_L	>	1.0	V
Operating ambient temperature	T_{amb}	0 to	+70	°C

PACKAGE OUTLINE 24 lead ceramic dual in-line (See General Section).



GENERAL DESCRIPTION

The FDR131Z2 is a pre-programmed version of the FDR131Z.
It is inteded for use as alphanumeric character generator in display systems, using a 5 x 7 dot matrix, where the characters are built-up column-wise. The CHARACTER SELECT inputs (A_4 to A_9) accept a six bit ASCII code, for the COLUMN SELECT inputs (A_1 to A_3) a three bit binary number is required, which is internally decoded. Each 7-bit word appears in parallel on the 7 outputs.

RATINGS
CHARACTERISTICS
OUTPUT BUFFER DESCRIPTION

For this information see data sheets of FDR131Z

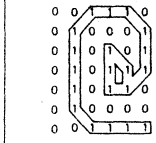
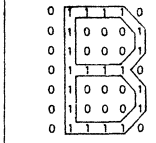
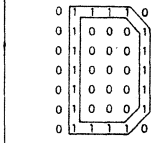
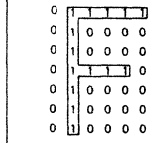
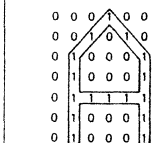
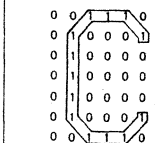
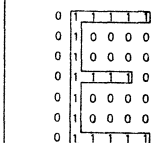
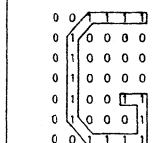
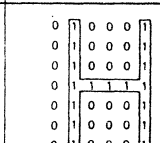
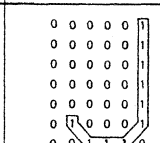
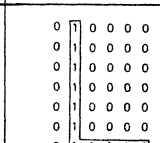
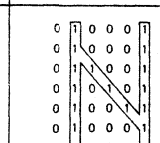
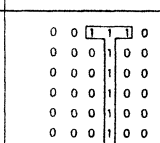
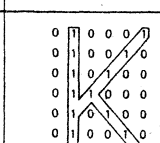
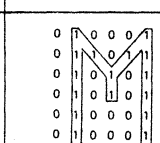
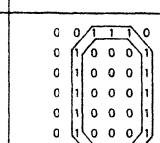
APPLICATION INFORMATION

To use the FDR131Z2 as character generator the ASCII code of the desired character should be applied to the address inputs A_4 to A_9 with the following correspondence:

ASCII bit	address input
b_1	A_4
b_2	A_5
b_3	A_6
b_4	A_7
b_5	A_8
b_6 or $\overline{b_7}$	A_9

Fot column selection, a three bit binary number should be applied to the address inputs A_1 to A_3 (A_1 being the least significant bit).
The character is stored in the columns 001 to 101. Column 000 contains blanks only and can be used to a space between characters.
When a LOW signal is applied to the output inhibit inputs, all outputs become floating. This feature can be used in wired-OR applications.

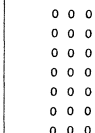
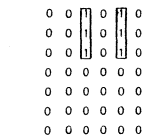
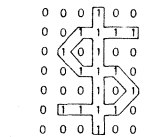
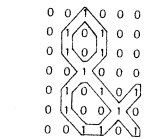
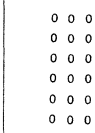
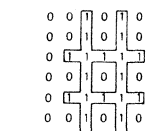
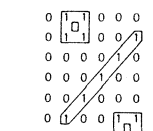
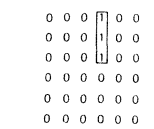
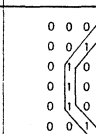
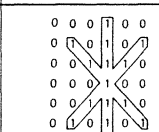
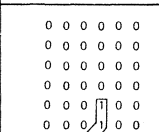
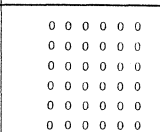
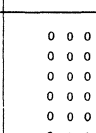
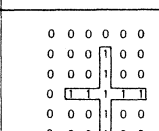
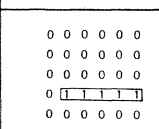
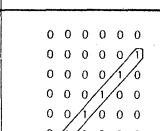
FDR131Z2 BIT PATTERN AND FONT

ASCII CHARACTER ADDRESS INPUTS $b_6\ b_5\ b_4\ b_3\ b_2\ b_1$ / $A_9\ A_8\ A_7\ A_6\ A_5\ A_4$	ROM OUTPUTS	COLUMN SELECT INPUTS $A_1\ A_2\ A_3$ = 0 0 0	0 0 1	0 1 0	0 1 1
		00	01	10	11
0 0 0 X X 0	Q_1				
	Q_2				
	Q_3				
	Q_4				
	Q_5				
	Q_6				
	Q_7				
0 0 0 X X 1	Q_1				
	Q_2				
	Q_3				
	Q_4				
	Q_5				
	Q_6				
	Q_7				
0 0 1 X X 0	Q_1				
	Q_2				
	Q_3				
	Q_4				
	Q_5				
	Q_6				
	Q_7				
0 0 1 X X 1	Q_1				
	Q_2				
	Q_3				
	Q_4				
	Q_5				
	Q_6				
	Q_7				

0 1 0 X X 0	Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7			
0 1 0 X X 1	Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7			
0 1 1 X X 0	Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7			
0 1 1 X X 1	Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7			

NOTE: 1 = LOW; 0 = HIGH

FDR131Z2 BIT PATTERN AND FONT (continued)

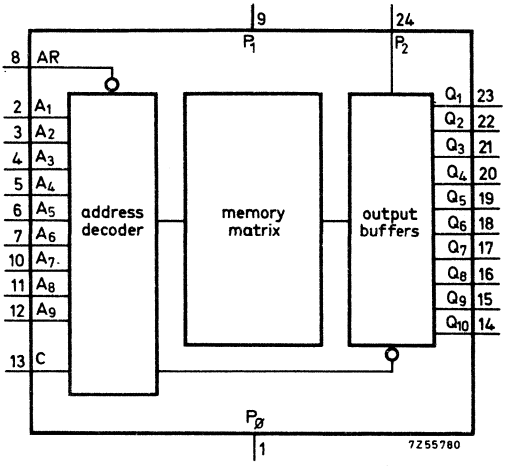
ASCII CHARACTER ADDRESS INPUTS $b_6\ b_5\ b_4\ b_3\ b_2\ b_1$ / $A_9\ A_8\ A_7\ A_6\ A_5\ A_4$	ROM OUTPUTS	COLUMN SELECT INPUTS			
		A_1 0 1 0 1 0 1 A_2 0 0 1 1 0 0 A_3 0 0 0 0 1 1	A_1 0 1 0 1 0 1 A_2 0 0 1 1 0 0 A_3 0 0 0 0 1 1	A_1 0 1 0 1 0 1 A_2 0 0 1 1 0 0 A_3 0 0 0 0 1 1	A_1 0 1 0 1 0 1 A_2 0 0 1 1 0 0 A_3 0 0 0 0 1 1
$X\ X$ →		00	01	10	11
1 0 0 X X 0	Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7				
1 0 0 X X 1	Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7				
1 0 1 X X 0	Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7				
1 0 1 X X 1	Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7				

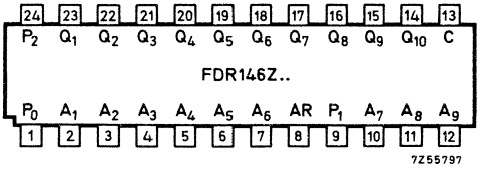
1 1 0 x x 0	Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7						
1 1 0 x x 1	Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7						
1 1 1 x x 0	Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7						
1 1 1 x x 1	Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7						

NOTE: 1 = LOW; 0 = HIGH

The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enchancement mode technology.

READ ONLY MEMORY, 512 WORD, 10 BITS PER WORD





P_0 and metal lid on bottom of the package are connected

QUICK REFERENCE DATA			
Read access time	t_{ac}	max. 725	ns
Supply voltage	V_{P1}	−24 to −28	V
Power dissipation	P_{tot}	typ. 300	mW
D.C. noise margin	M_H, M_L	> 1	V
Operating ambient temperature	T_{amb}	−55 to +85	°C

PACKAGE OUTLINE 24 lead metal ceramic dual in line (See General Section).

GENERAL DESCRIPTION

The FDR146Z is a monolithic 5120-bit, static operated, READ-only memory with a built-in output register. The contents is read into the register after an address READ pulse and the outputs remain steady until the next address READ pulse.
The 5120 bits are organized into 512 10-bit words, making the memory suitable for use in look-up tables, code connectors, message and logic function generators, and in micro-programmers with sufficient capacity for next instruction or flags. It can also be treated as 64 8x10 matrices for high-resolution character generators. The memory is programmed during manufacture with the aid of a pattern made to the customer's specifications.
Internal resistors at the input provide pull-up for TTL sources. For high speed operation these resistors should be shunted and one of the output configurations illustrated in the section on output buffers should be used.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages on all data inputs, clock inputs, outputs and supply terminals, with reference to P_0			+0.5 to −30	V
Power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1.25	W
Junction temperature	T_j	max.	150	°C
Storage temperature	T_{stg}		−65 to +150	°C
Total current through terminal P_1	$\pm I_{P1}$	max.	40	mA
Output current (per output)	$\pm I_Q$	max.	20	mA

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$	=	100	°C/W

CHARACTERISTICS at T_{amb} = −55 to +85 °C; P_0 = grounded.

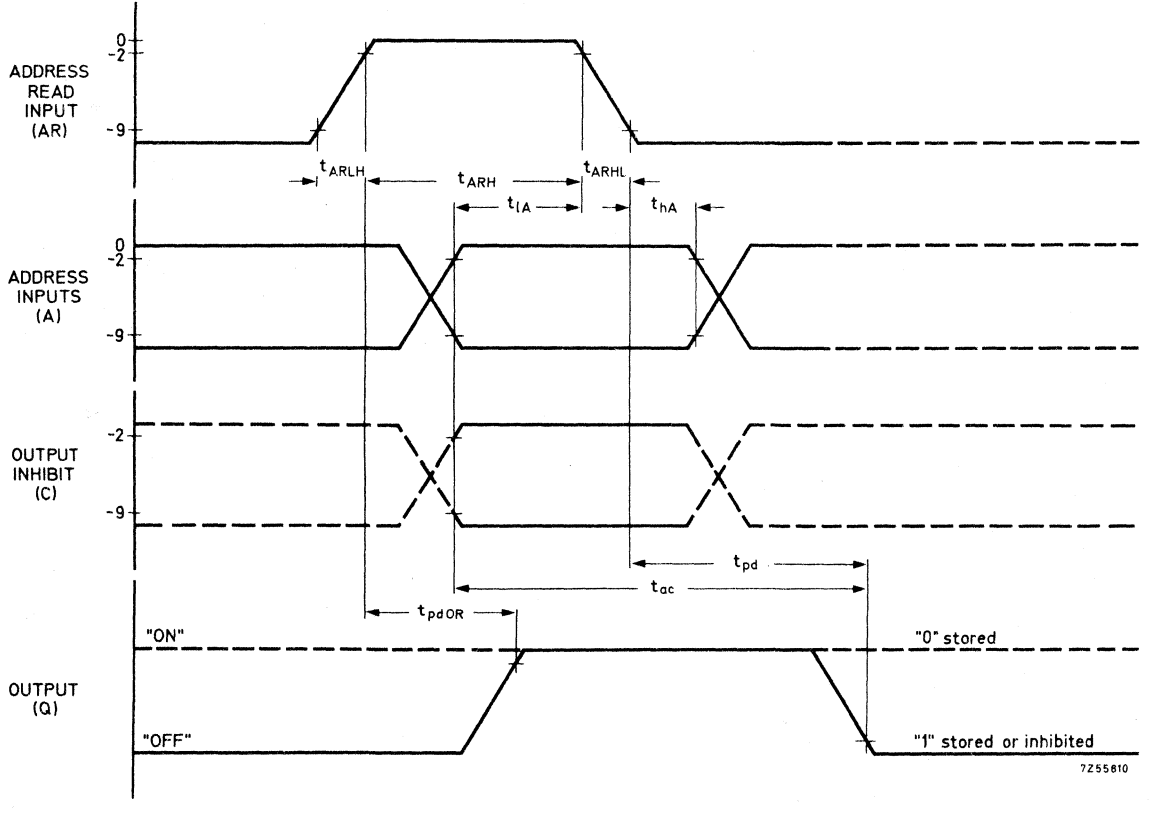
ELECTRICAL DRIVE REQUIREMENTS	Symbol	min.	typ.	max.		conditions and references
Supply voltages						
P_1	$-V_{P1}$	24	–	28	V	
P_2	$-V_{P2}$	0	–	15	V	
Supply current at P_1						
	$-I_{P1}$	–	9	–	mA	V_{P1} = -24 V; T_{amb} = 25°C
	$-I_{P1}$	–	–	18	mA	V_{P1} = -27 V; T_{amb} = 25°C
Logic levels						
(all inputs)						
HIGH	V_{AH}; V_{CH}; V_{ARH}	-2.0	–	+0.3	V	
LOW	V_{AL}; V_{CL};					
	V_{ARL}	-15.0	-12.0	-9	V	
Read rate	f_{AR}	0	–	1.33	MHz	$t_{ARLH} + t_{ARHL}$ = 50 ns
Address read pulse times						
pulse width	t_{ARH}	0.2	–	100	µs	See interface circuit "a" on page 7
rise time	t_{ARLH}	–	–	100	ns	
fall time	t_{ARHL}	–	–	100	ns	
address lead time	$t_{\ell A}$	200	–	–	ns	
address hold time	t_{hA}	50	–	–	ns	

CHARACTERISTICS (continued)

Test conditions: V_{P_1} = −24 V to −28 V; V_{P_2} = 0 to −15 V; T_{amb} = -55 to +85 °C

ELECTRICAL DATA	Symbol	min.	typ.	max.		conditions and refernces
Read access time	t_{ac}	–	–	750	ns	see timing diagram
Propagation delay	t_{pd}	–	–	500	ns	
Output reset delay	$t_{pd}OR$	75	–	400	ns	
Output currents						
"OFF" condition	$-I_Q$	–	–	167	µA	V_{P_2} = 0; V_Q = −10 V; T_{amb} = 25 °C
"ON" condition	$-I_Q$	2.5	4.5	–	mA	V_{P_1} = −23 V; V_{P_2} = 0 V; V_Q = −2.5 V
Input capacitances						
Address input	C_A	–	3.5	4	pF	V_A = 0 V; f = 1 MHz
Address read input	C_{AR}	–	4	4.5	pF	V_{AR} = 0 V; f = 1 MHz
Output inhibit input	C_C	–	4.5	5	pF	
Input resistance						
(all inputs)	R_A;R_{AR};R_C	–	15	35	kΩ	between input and P_0
Output capacitance	C_Q	–	3.5	4.5	pF	V_Q = 0 V; f = 1 MHz

CHARACTERISTICS (continued)



Notes:

1. To enable the device the output inhibit input C should be HIGH during the specified time; to inhibit the device it should be LOW during that time.
2. The indicated points on the vertical axis are specified in the glossary of terms.

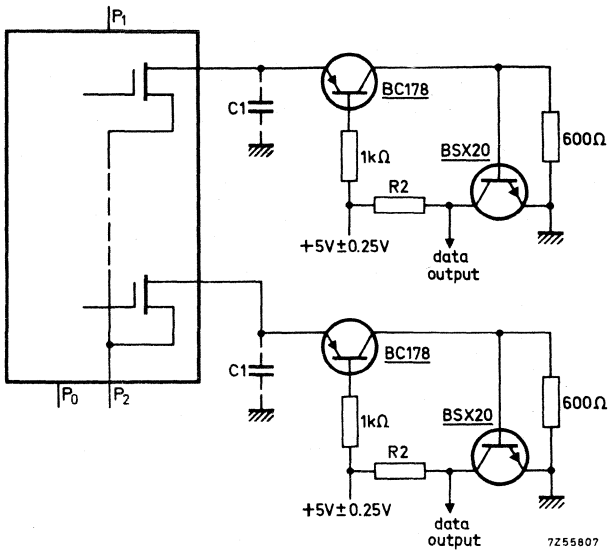
CHARACTERISTICS (continued)

GLOSSARY OF TERMS

1. Address read pulse width: t_{ARH}
   The time for which the address read pulse is HIGH: $V_{AR} \geq -2\,V$.
2. Address read pulse rise time: t_{ARLH}
   The time between the −9 V and −2 V voltage points as the read pulse goes from LOW to HIGH.
3. Address read pulse fall time: t_{ARHL}
   The time between the −2 V and −9 V voltage points as the read pulse goes from HIGH to LOW.
4. Output reset delay: t_{pdOR}
   After the AR pulse reaches HIGH, the time that elapses before the output reaches its "ON" state.
5. Address lead time: $t_{\ell A}$
   The time that the address and output inhibit signals must be valid before the start of the falling edge of the AR pulse.
6. Address hold time: t_{hA}
   The time that the address and output inhibit signals must be valid after the end of the falling edge of the AR pulse.
7. Propagation delay: t_{pd}
   The time between the end of the AR pulse and the output assumes its correct state.
8. Read access time: t_{ac}
   The time between the points, the address and output inhibit signals must be valid and the output assumes its correct state.

OUTPUT BUFFER DESCRIPTION

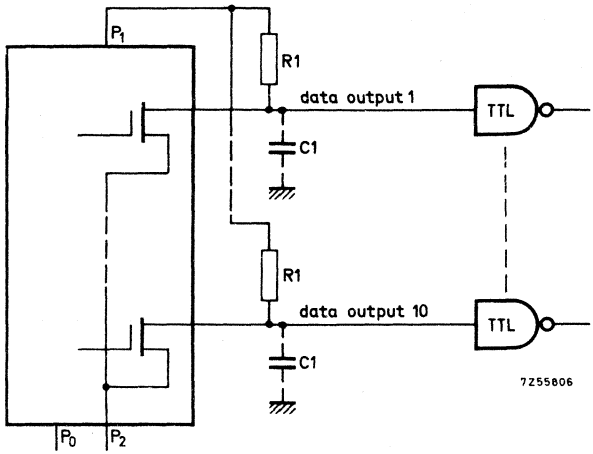
a. Current sense output interface



V_{P1} (V)	V_{P0} (V)	V_{P2} (V)	t_{ARH} (ns)	t_{ac} (ns)	cycle time (ns)	R2 (Ω)	load C1 (pF)	TTL fan-out
−12.5 to −13.5	+12.5 to +13.3	+7.0 to +8.0	> 200	< 725	< 750	> 150	< 100	20

OUTPUT BUFFER DESCRIPTION (continued)

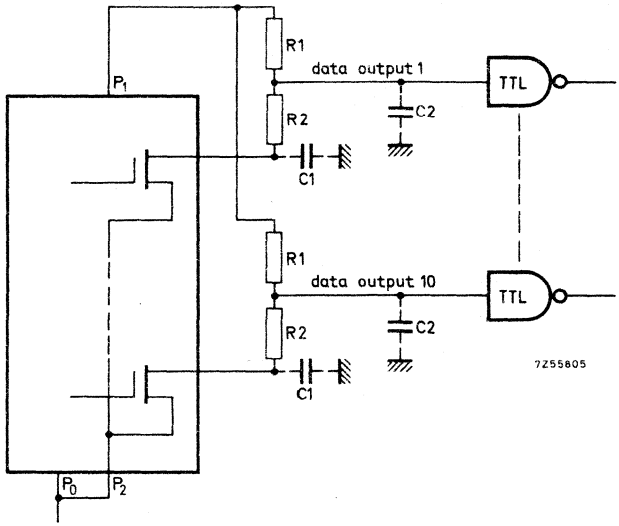
b. Single resistor TTL interface



V_{P1} (V)	V_{P0} (V)	V_{P2} (V)	t_{ARH} (ns)	t_{ac} (ns)	cycle time (ns)	R1 (kΩ)	load C1 (pF)	TTL fan-out
−12.5 to −13.5	+12.5 to 13.5	+5.75 to +6.25	>200	<725	<750	6.8	<15	1
−11.5 to −13.5	+11.5 to 13.5	+5.75 to +6.25	>250	<725	<800	6.8	<15	1
−14.5 to −15.5	+ 9.5 to 10.5	+4.75 to +5.25	>250	<725	<800	8.2	<15	1

OUTPUT BUFFER DESCRIPTION (continued)

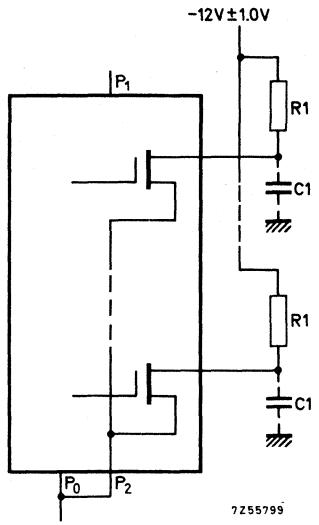
c. Two resistor TTL interface



V_{P1} (V)	V_{P0} (V)	t_{ARH} (ns)	t_{ac} (ns)	cycle time (ns)	R1 (kΩ)	R2 (kΩ)	load C1;C2 (pF)	TTL fan-out
−11.5 to −13.5	+11.5 to +13.5	>725	<625	<800	6.8	3.0	10	1
−12.5 to −13.5	+12.5 to +13.5	>725	<625	<750	6.8	3.0	10	1

OUTPUT BUFFER DESCRIPTION (continued)

d. MOS interface



V_{P1} (V)	V_{P0} (V)	V_{P2} (V)	t_{ARH} (ns)	t_{ac} (ns)	cycle time (ns)	R1 (kΩ)	C1 (pF)
−23.0 to 27.0	0	0	>250	<825	<900	12	15

INPUT INTERFACE

Inputs A_1 to A_9, output inhibit C and address READ AR all have internal pull-up resistors to make them compatible with bipolar (TTL and DTL) circuits without requiring any additional components.

In the typical TTL-to-MOS interface shown below, V_{P1} is biased to −12 V, V_{P0} to +12 V, and the TTL gates to +5 V and ground. A TTL HIGH level at the gate input results in a MOS LOW level at the ROM input. When a TTL LOW level is initiated, the internal resistor R_i provides pull-up for the voltage rise of the TTL output. The external resistor R_S is for the purpose of improving rise time only. The gate can be any TTL device with 15 V output rating.

ROM input rise and fall times are dependent upon the total input capacitive load and the impedance of the TTL driving circuit during turn-off and turn-on respectively.

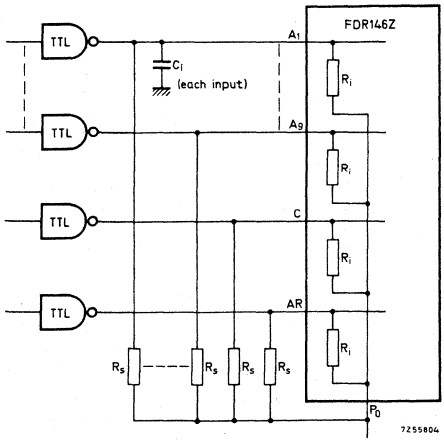
The rise time required for a 0 to 10 V transition is about 2 RC. Because of the relatively high value of R_i (35 kΩ max.), the rise time may approach 700 ns for a 10 pF load; to increase the speed at the input, shunt R_i with an external resistor.

$$\text{Since } t_{ARLH} = 2\,R_t C_i = 2\left(\frac{R_i R_S}{R_i + R_S}\right) C_i$$

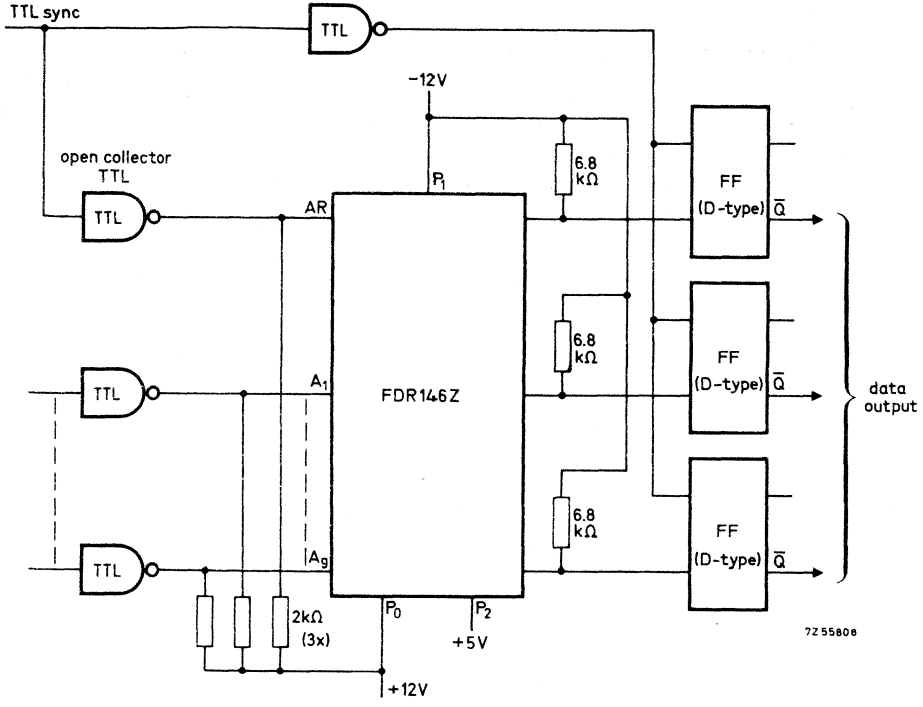
For a 50 ns rise time, R_t would equal 2.5 kΩ, so $R_S = 2.8$ kΩ.

The fall time is given by $t_{ARHL} \approx Ci \cdot V_P / I_{sink}$, where I_{sink} is 50 to 100 mA for the FJ family types, and V_P is the voltage transition. The values of R_i and R_S are not significant in the determination of fall time.

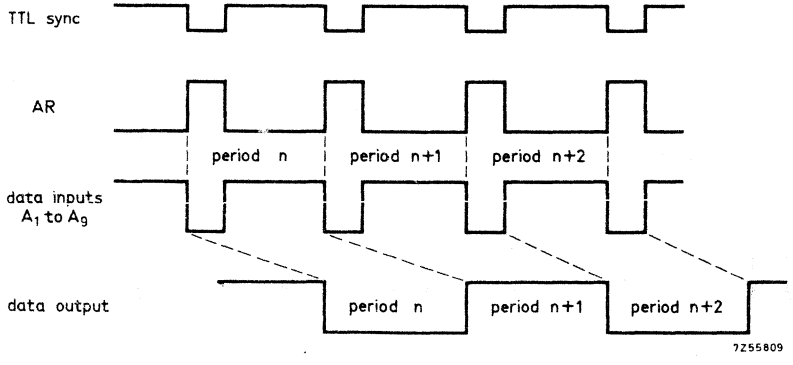
Assume the rise time of 700 ns to be as derived above for the address inputs. Allow 300 ns for the period $t_{\ell A} + t_{hA} + t_{ARHL}$ This indicates that for operating at cycle times greater than 1 μs with a new address available immediately after t_{hA}, no additional components are required at the input circuit. For operating at cycle times faster than 1 μs, the shunt resistor R_S is required.



APPLICATION INFORMATION

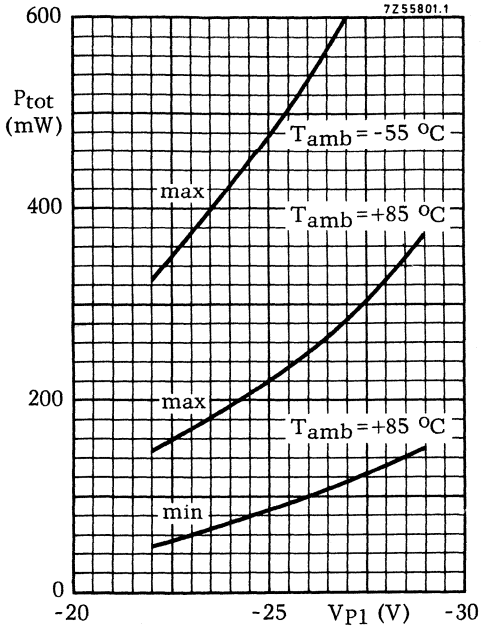


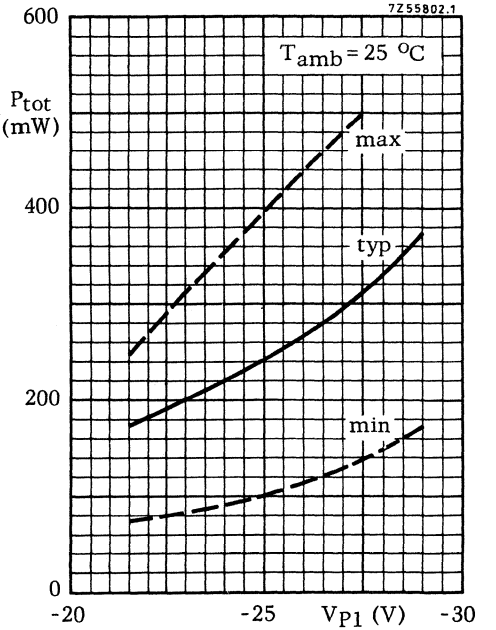
This circuit can be used to obtain NRZ outputs

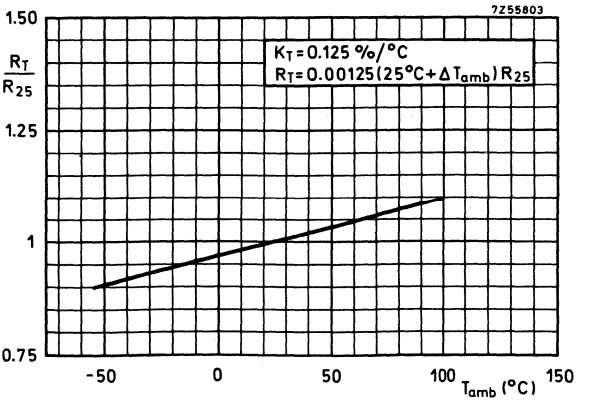


For this example, data stored in address during periods n, n+1 and n+2 have been arbitrarily to be "1", "0", "1" respectively.

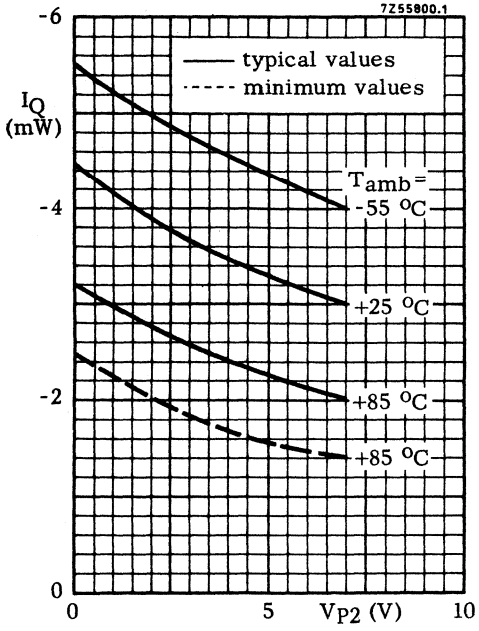
TYPICAL PERFORMANCE



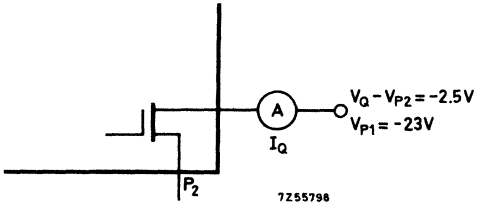




TYPICAL PERFORMANCE (continued)



Test circuit:



PROCEDURE FOR ORDERING A SPECIAL BIT PATTERN

To ensure accuracy when ordering a special bit pattern for a Read Only Memory (ROM) mask, customers should make use of the form on page 17. Eight forms are needed for 512 word memories. The completed forms enable us to transfer any desired bit pattern into a standard ROM without error. After receipt of the forms our procedure is as follows:

1. An IBM card is punched for each row of each sheet of the form. (If he prefers to do so, the customer may punch his own cards and supply them to us, provided their format is identical with that of the forms).
2. The punched cards are incorporated in a computer program that originates the following:
   - a duplicate of the ordered bit pattern, for verification.
   - a control tape for programming final electrical testing of the customer's ROM.
   - a control tape embodying the ordered pattern of ones and zeros to govern the movement of the automatic plotter used in mask making.
3. The computer print-out is checked against the original order forms; a copy is also sent to the customer for his verification and signature.
4. Upon receipts of the customer's signed verification, full scale masks embodying the desired pattern are made and the unique type number suffix is assigned.

INSTRUCTION FOR COMPLETING THE FORMS

A. Customer block: ON EACH FORM

Enter Name, Date and Authorized Signature in the spaces provided.

B. The ADDRESS INPUTS and CONTENTS

Each page of the ROM Bit Pattern Form is laid-out for 64 consecutive words; 16 in each of the four columns (00, 01, 10 and 11).

B. ADDRESS INPUTS

a) There are nine Address Inputs; the right-hand bit is always bit 1 and is the least significant bit; the left-hand bit is 9, it is the most significant. The Address Input leads on the ROM package are labelled A_1, A_2, etc., to correspond.

b) The states of bits 1 to 4 are listed consecutively down the page. The state of bits 5 and 6 are at the head of each of four output columns. The Address Input of 64 consecutive words are thus uniquely specified on each page.

c) Bit 7, 8, and 9 (or bits 7 and 8 only, for 256 word memories) specify sets of memory locations, 1 set of 64 words per page. These spaces should be filled by the customer using a consecutive full binary code. The first position on page 1 of your specification should be three (or two) zeros. [1]
Memories of 256 words need 4 pages, of specifications.

d) Only ones (1 = "OFF") or zeros (0 = "ON") should be used in completing the form except where, a column is unused and is, therefore, left blank.

---

[1]) See example on page 17

p.t.o.

2. CONTENTS (DATA OUTPUTS)
   a) Each column has provision for words of 10 bits numbered 1 to 10, bit 1 is always the right-hand bit. The output leads of the ROM package are labelled Q_1, Q_2, etc., to correspond.
   b) The requisite bit pattern should be inserted under headings 1 to 10 using only ones (1 = "OFF") and zeros (0 = "ON"), except where a column is unused and is, therefore, left blank.

3. AUTHORIZED SIGNATURE
   Having completed the bit pattern, the customer should check that the forms are numbered, dated, and signed, as they constitute formal evidence of his request. In the event that the customer provides his own punched cards the signature on the computer duplicate will serve as formal evidence.

PHILIPS
Electronic Components and Materials
Integrated Circuits

Read Only Memory Bit Pattern **FDR 146 ...**

page of

CUSTOMER NAME:

DATE

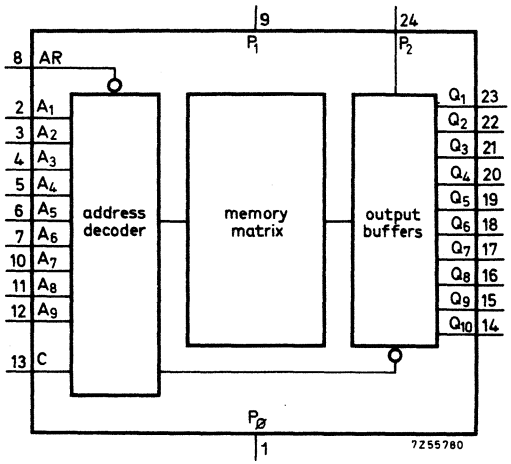
AUTHORIZED SIGNATURE

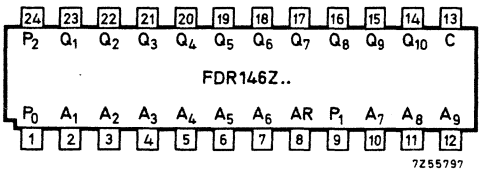
ADDRESS INPUTS 9 8 7 6 5 4 3 2 1	00 OUTPUTS 10 9 8 7 6 5 4 3 2 1	01 OUTPUTS 10 9 8 7 6 5 4 3 2 1	CONTENTS 10 OUTPUTS 10 9 8 7 6 5 4 3 2 1	11 OUTPUTS 10 9 8 7 6 5 4 3 2 1
XX0000				
XX0001				
XX0010				
XX0011				
XX0100				
XX0101				
XX0110				
XX0111				
XX1000				
XX1001				
XX1010				
XX1011				
XX1100				
XX1101				
XX1110				
XX1111				

Note: 1 = "OFF"; 0 = "ON"

The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enchancement mode technology.

CHARACTER GENERATOR
(7 x 9 DOT MATRIX; COLUMN SCAN SYSTEM)





P_0 and metal lid on bottom of the package are connected

QUICK REFERENCE DATA			
Read access time	t_{ac}	max. 725	ns
Supply voltage	V_{P1}	−24 to −28	V
Power dissipation	P_{tot}	typ. 300	mW
D.C. noise margin	M_H, M_L	> 1	V
Operating ambient temperature	T_{amb}	−55 to +85	°C

PACKAGE OUTLINE 24 lead metal ceramic dual in line (See General Section).

GENERAL DESCRIPTION

The FDR146Z1 is a pre-programmed version of the FDR146Z and contains 64 ASCII encoded symbols.
Each high resolution character is a 7 x 9 dot matrix organized for column scanning (7 columns with 9 parallel output lines).
The input code is 6-bit ASCII. The 3-bit column code is internally decoded on the chip. Access times of 725 ns or better are achievable by utilizing the appropriate output configuration.

RATINGS
CHARACTERISTICS
OUTPUT BUFFER DESCRIPTION

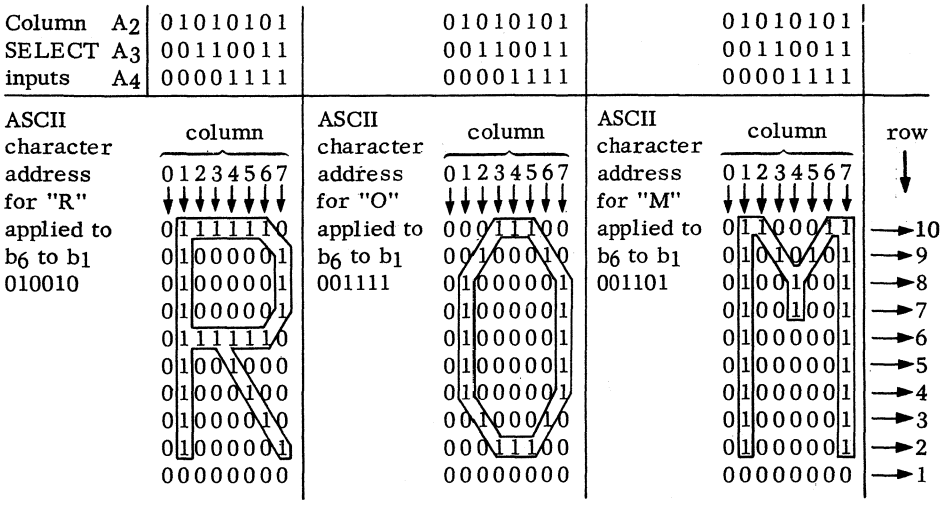
For this information see data sheets of FDR146Z....

CHARACTER GENERATOR ORGANIZATION

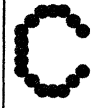
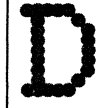
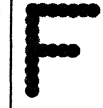
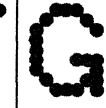
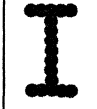
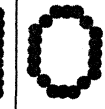
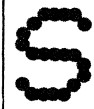
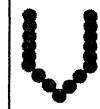
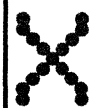
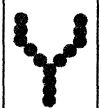
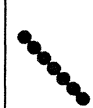
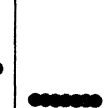
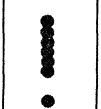
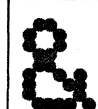
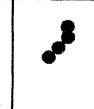
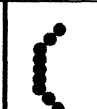
The FDR146Z1 is primarily intended for generation of high resolution character fonts for vertical scan displays.
Each 63 bit character is composed of 7 distinct 9-bit columns. One of the 64 characters is selected by a 6-bit address applied to inputs A_5, A_6, A_7, A_8, A_9 and A_1 corresponding to the ASCII code bits b_6 to b_1 respectively.
The particular 9-bit column is determined by the 3-bit address applied to address inputs A_2, A_3 and A_4 (column SELECT inputs).
After seven successive column addresses, the entire character is completed. The 7 x 9 font is fitted to an 8 x 10 matrix, with column address 000 programmed with all zeros to provide character space and line space. Other usefull applications include a low speed horizontal scan usage (as in line printers) requiring high resolution.
The technique involved to rotate the character is illustrated in the APPLICATION INFORMATION on page 5.

EXAMPLE

In this example, with the ASCII character address fixed, the column select inputs are sequentially altered to produce one complete character of 8 successive columns. After 8 sequential binary column select iterations, the character address is changed and the column select procedure repeated.
All the 0 column select input addresses produce a space column.



CHARACTER FONT AND INPUT CODE

ASCII INPUT ADDRESS	$b_3b_2b_1$ 000	001	010	011	100	101	110	111
$b_6b_5b_4$ 000								
001								
010								
011								
100								
101								
110								
111								

APPLICATION INFORMATION

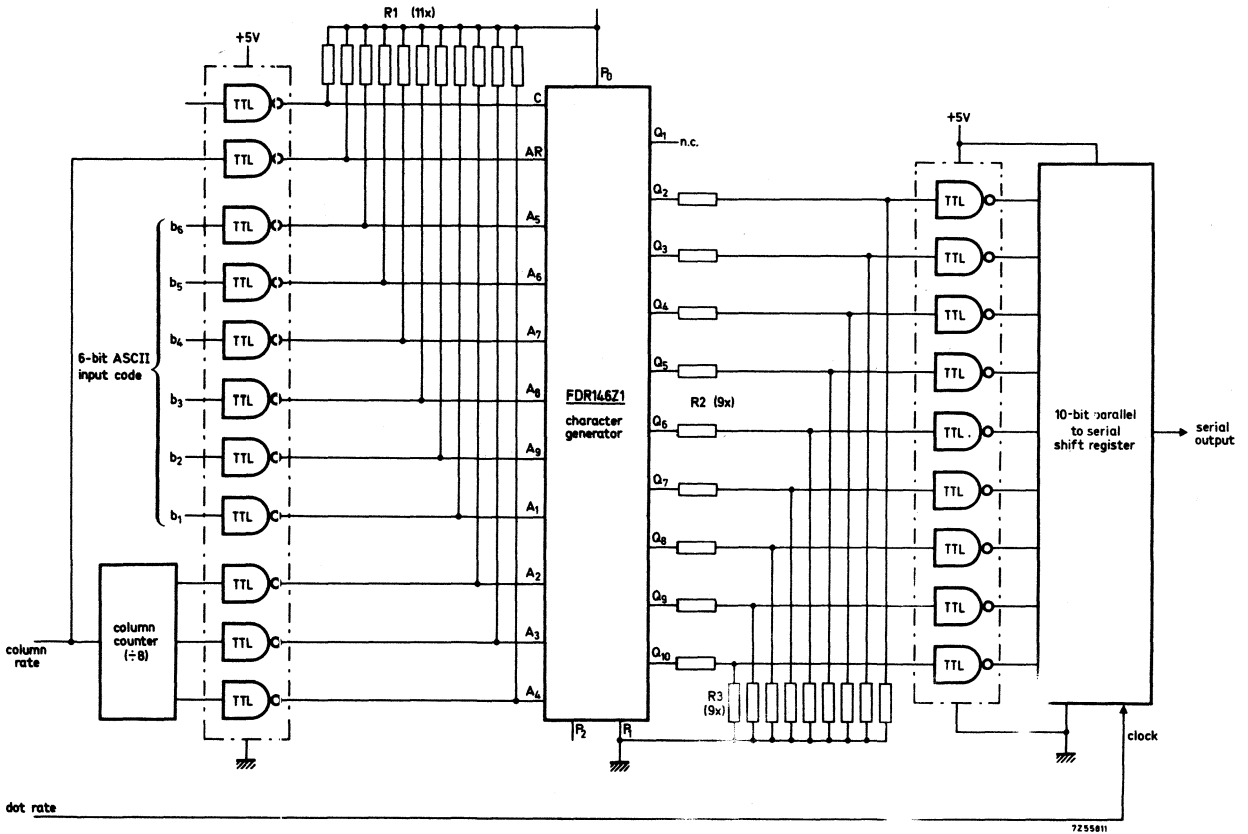
Vertical column scanning (see circuit on page 6)

At a given ROM input address (an ASCII code plus the column code) nine parallel bits are detected, representing on column of a character. Depending upon the application, the entire column may be displayed at once, or as in the case of Z axis modulation of a single beam, it is necessary to convert the nine parallel bits to a single train of serial bits.
The "two resistor" interface is only one of several interface techniques that may be employed (see also FDR146Z data sheet).

Low speed horizontal row scanning (see circuit on page 7)

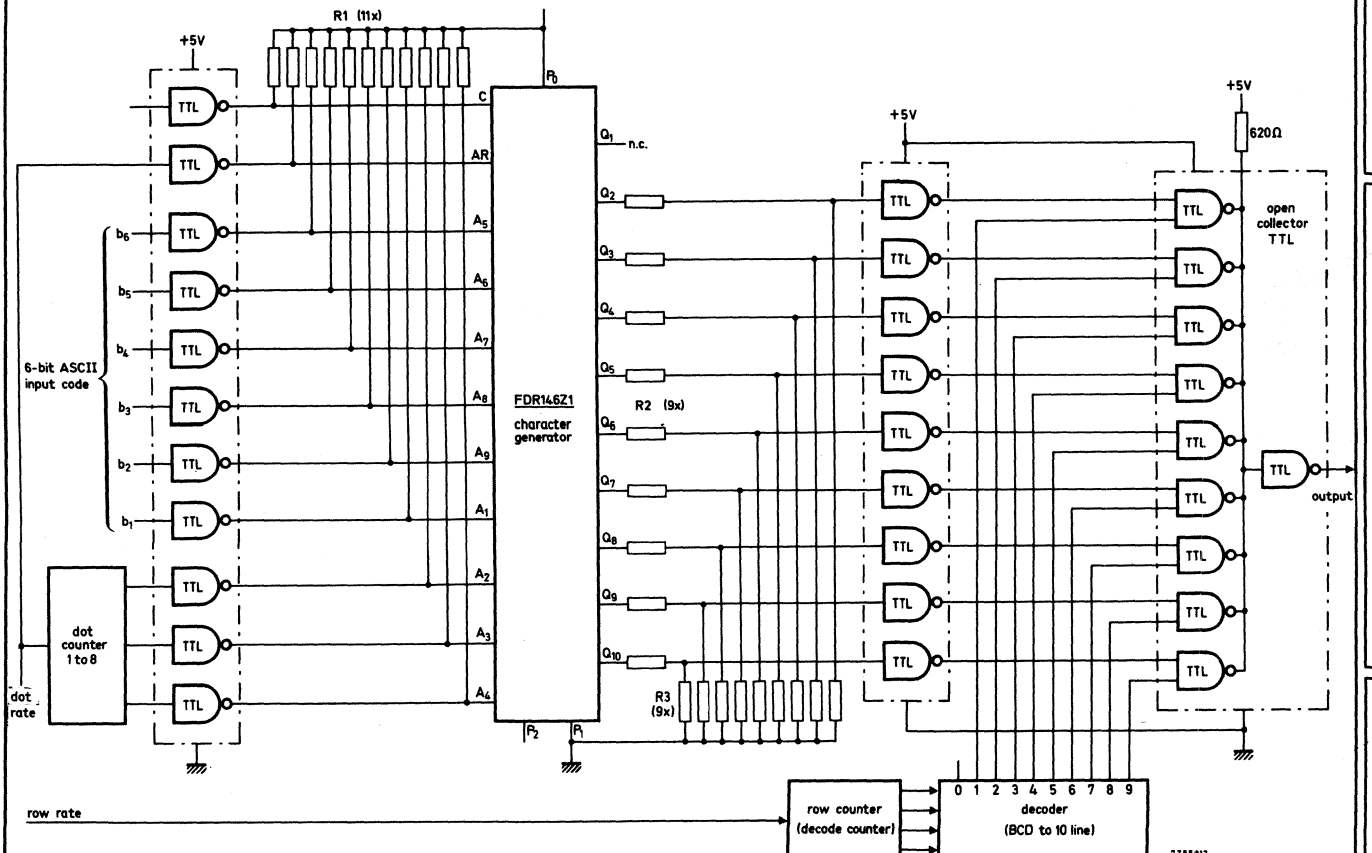
For applications such as electronic printing in line increments this technique will rotate a pre-programmed vertical scan character font to one with a horizontal scan orientation. Essentially, the roles of the dot rate and the row rate have been interchanged. Again, the "two resistor" interface is only one of several interface techniques that may be employed.
For any given ROM address, only one bit is detected and is in the row determined by the state of the counter. To generate one complete row of information, the row counter holds while the dot counter scans the full row. This scan is repeated for each of the ten rows to generate a complete character. The scan time for one row is increased by the time required to address eight dot rows. Thus, for a device with a 700 ns cycle time, it would require 5.6 µs to complete the row of that character, which is the upper limit for this technique. The outputs of the gates are wired-OR, to provide one line out and to eliminate the parallel-to-serial shift register.

APPLICATION INFORMATION (continued)



Vertical column scanni (see page 5)

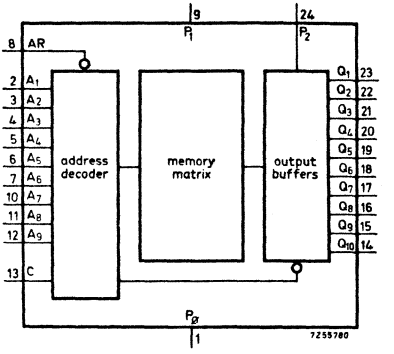
APPLICATION INFORMATION (continued)

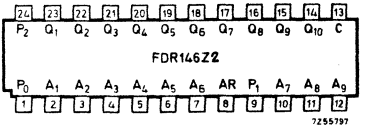


Low speed horizontal ro scanning (see also page 5)

The FD family is a series of complex monolithic integrated circuits utilizing MOS P-channel enchancement mode technology.

STATIC CHARACTER GENERATOR
UPPER AND LOWER CASE
(5 × 7 dot matrix; row scan system)





P_0 and metal lid on bottom of the package are connected.

QUICK REFERENCE DATA			
Read access time	t_{ac}	max. 725	ns
Supply voltage	V_{P1}	−24 to −28	V
Power dissipation	P_{tot}	typ. 300	mW
D.C. noise margin	M_H, M_L	> 1	V
Operating ambient temperature	T_{amb}	−55 to +85	°C

PACKAGE OUTLINE 24 lead metal ceramic dual in line (See General Section).

GENERAL DESCRIPTION

The FDR146Z2 is a pre-programmed version of the FDR146Z and intended for use as character generator in 5 x 7 dot matrix displays, where the full 7-bit ASCII character set is required.
128 characters are stored in the FDR146Z2, viz. the upper and lower case characters and a pictorial representation of the control codes.
The character generator is organized for row scan, i.e. when a 7-bit ASCII code and a 3-bit row code is applied, the five bits belonging to one horizontal row of the character font appear at the outputs.
Access times of 725 ns or better are achievable by utilizing the appropriate output configuration.

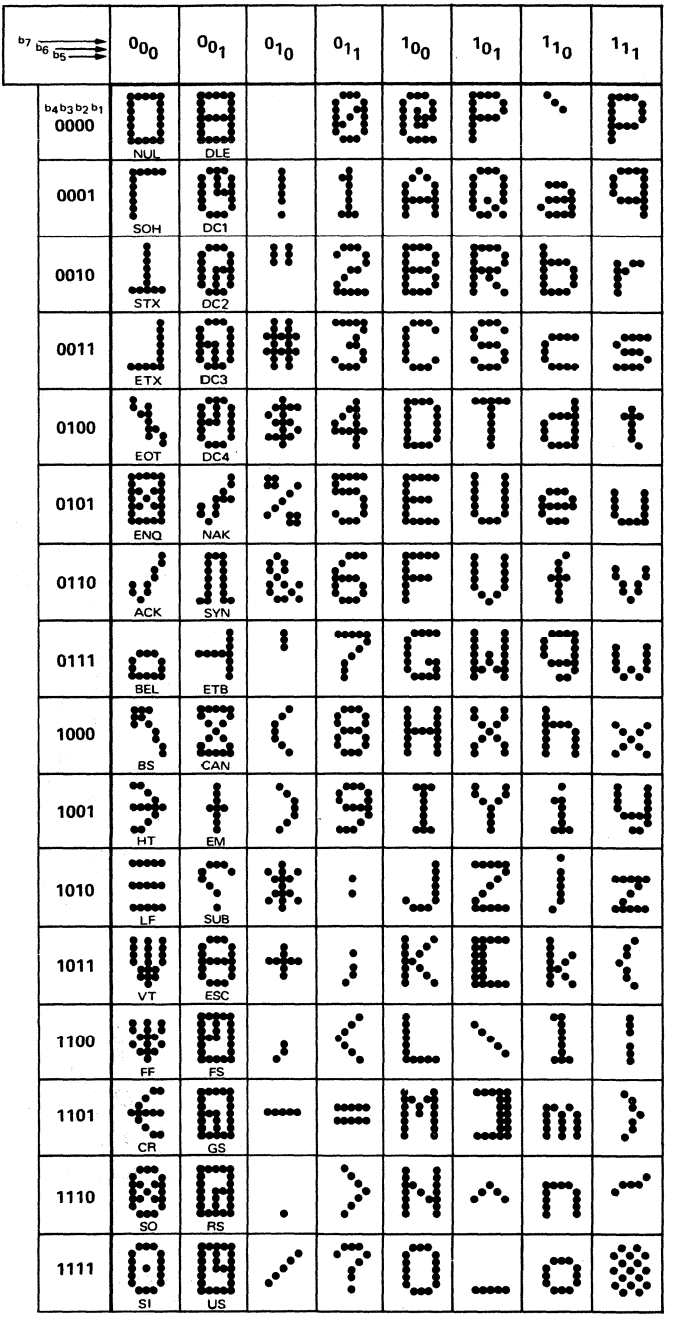
RATINGS

CHARACTERISTICS

OUTPUT BUFFER DESCRIPTION

For this information see data sheets of FDR146Z

CHARACTER FONT AND INPUT CODE



APPLICATION INFORMATION

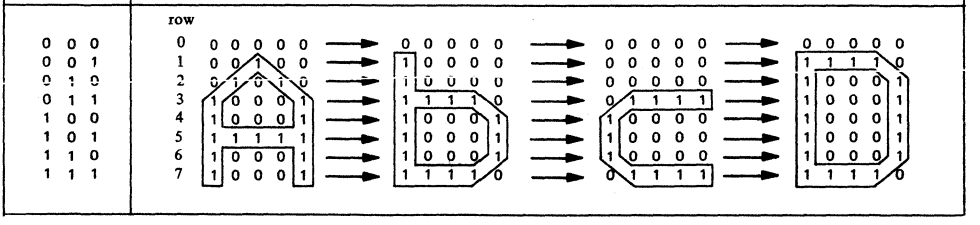
To use the FDR146Z2 as a character generator the ASCII code of the character to be displayed should be applied to the inputs A_4 to A_9 with the following correspondence:

ASCII bit	address input
b_1	A_4
b_2	A_5
b_3	A_6
b_4	A_7
b_5	A_8
b_6	A_9

Negative logic is assumed for the inputs (HIGH = 0; LOW = 1).

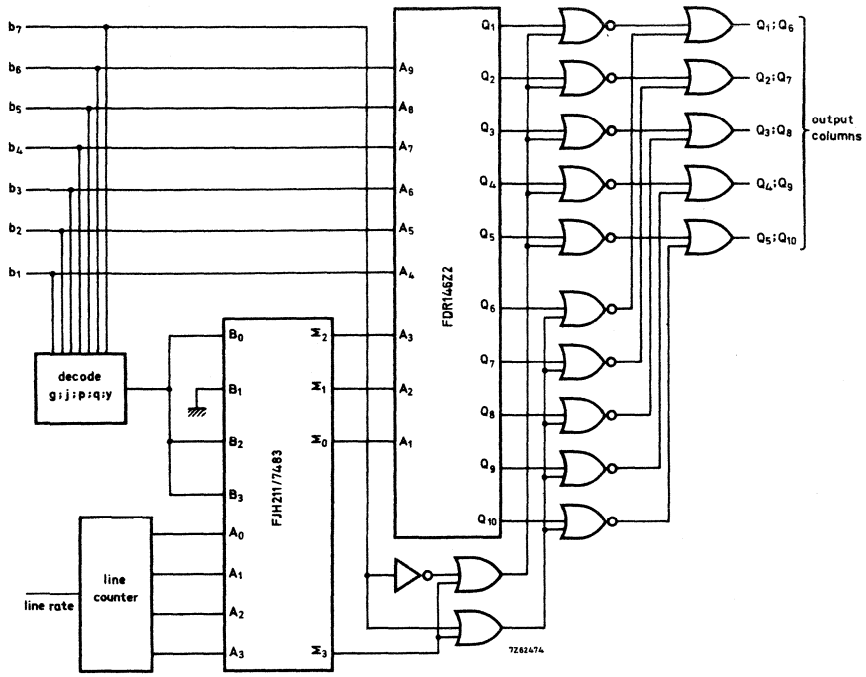
ASCII bit b_7 must be used to select between the outputs Q_1 to Q_5 or Q_6 to Q_{10} (See example on page 5).
The row select code should be applied to the inputs A_1 to A_3 (A_1 being the least significant bit).
The characters are stored in rows 1 to 7, row 0 contains blanks (see example below).
The figure on page 5 shows the block diagram of a character generator system incorporating a "descender" circuit, with which the lower case g, j, p, q and y can be lowered two rows. For this purpose an adder circuit is inserted between the row counter and the READ ONLY MEMORIES.
When a lower case g, j, p, q or y is detected a binary 2 is subtracted from the row number (actually the binary number 14 is added), which causes the character to be displayed two rows lower.
The output $\Sigma 3$ of the adder is used to blank all outputs in order to avoid a repeated display of the character during rows 9 and 10 in the "normal" position, or during rows 0 and 1 in the "descended" position.

ROM ORGANIZATION



In this example, with the row select input address fixed, the ASCII character addresses are sequentially altered to produce one line of four different characters, left to right. After 8 sequential binary row select iterations, using the same character address sequence, the complete ROW of characters is formed, including a SPACE line.

APPLICATION INFORMATION (continued)



b_7 = logic LOW, selects Q_6 to Q_{10}

block diagram of 128ASCII symbol character generator

Note:

With a separate additional input on the counter, one could also utilize any of the characters as subscripts.

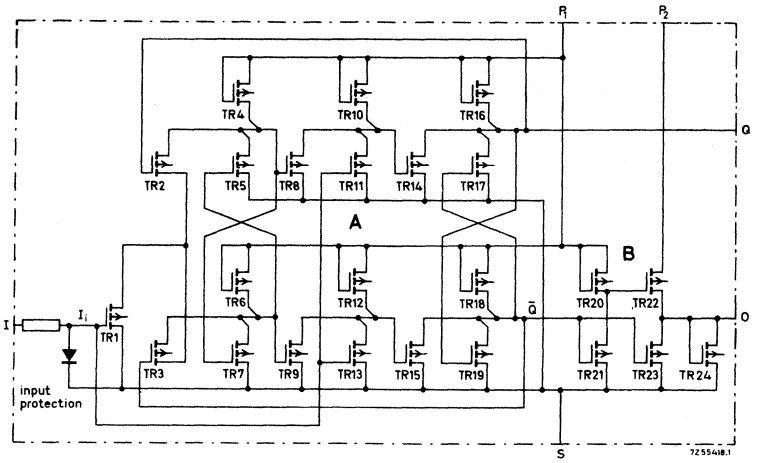
MOS FREQUENCY DIVIDER

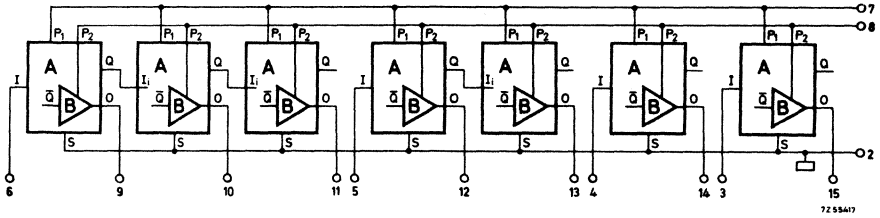
The SAJ100 is a monolithic integrated circuit in MOS-technique, consisting of 7 binary frequency dividers separated into 3, 2, 1 and 1, each section having its own trigger input. The trigger input of each section is protected by a diode and all outputs are protected by a thick oxide MOS to prevent gate breakdown. As the flip-flops comprising each section are of the master-slave type, the circuit can accept any input waveform, making the device particularly suitable for use in electronic organs. The output impedance is low (R_L = 1 kΩ) and there is excellent separation between adjacent stages.

QUICK REFERENCE DATA					
Supply voltage	$-V_{7-2} = -V_{P1}$		nom.	25	V
Supply voltage for output stage	$-V_{8-2} = -V_{P2}$		nom.	8.5	V
Operating ambient temperature		T_{amb}	nom.	25	°C
Input voltage levels		$-V_{IL}$	≥	6.5	V
		$-V_{IH}$	≤	2	V
Output voltage levels		$-V_{OL}$	≥	7.5	V
		$-V_{OH}$	≤	0.1	V
Output impedance		$\|Z_O\|$	typ.	1.0	kΩ
Total power dissipation every output loaded with R_L = 10 kΩ		P_{tot}	typ.	80	mW

PACKAGE OUTLINE: 16 lead dual in-line (See page 7)

CIRCUIT DIAGRAM





RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages

Pin No. 3; 4; 5; 6; 7; 8; voltage with respect to pin No. 2 (substrate)		−30 to +0.3	V
All other pins to substrate (pin No. 2)		max. + 0.3	V [1]

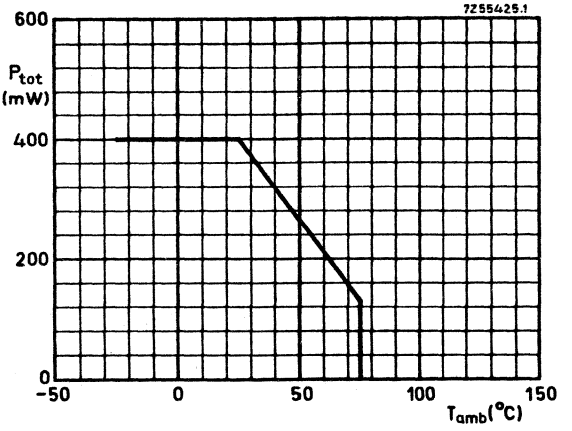
Temperatures

Storage temperature	T_{stg}	−55 to + 125	°C
Operating ambient temperature	T_{amb}	−25 to + 75	°C

[1] To keep the p-n junctions from being forward biased, the voltage at each lead must not be allowed to become more than 0.3 V positive with respect to the substrate.

RATINGS (continued)

Total power dissipation P_{tot} max. 400 mW



Note:

So long as the maximum temperature is not exceeded, the device will not be damaged by occasioned short-circuiting of any output.
Currents are plotted in Figs. 4 and 5 on page 6.

CHARACTERISTICS

Supply voltages

divider stages	$-V_{7-2} = -V_{P1}$	20 to 30 V [1]	
		typ. 25 V [1]	
buffer stages	$-V_{8-2} = -V_{P2}$	7.0 to 30 V [1]	
		typ. 8.5 V [1]	

[1] If the divider stages are externally coupled through (output voltage V_O of one stage used to trigger the next stage) satisfactory operation can not be guaranteed at the extreme condition: $-V_{P1}$ = 30 V, $-V_{P2}$ = 7.0 V (at load resistance R_L = 10 kΩ)

CHARACTERISTICS at $-V_{P1}$=25 V; $-V_{P2}$=8.5 V; T_{amb} = 25 °C unless otherwise specified (see Fig. 1 on page 5)

Input voltage levels (see also Fig.2)					
	$-V_{IL}$	≥	6.5	V	
	$-V_{IH}$	≤	2	V	
Buffer output voltage levels (see also Fig.3)					
LOW	$-V_{OL}$	≥	7.5	V	1)
HIGH	$-V_{OH}$	≤	0.1	V	1)
Output signal rise time (see also Fig.3)	t_{Or}	typ.	6	μs	2)
Output signal fall time (see also Fig.3)	t_{Of}	typ.	0.5	μs	2)
Input leakage current					
$-V_I$ = 25 V	$-I_I$	typ.	10	nA	
$-V_I$ = 30 V	$-I_I$	≤	10	μA	
Total power dissipation	P_{tot}	typ.	80	mW	3)
Total supply currents	$-I_7$	typ.	3	mA	4)
	$-I_8$	≤	5.6	mA	5)
Frequency range					
Input I driven by sine wave	f_I	10 Hz to 100		kHz	
Output impedance (see also Fig.6)	$\lvert Z_O \rvert = \frac{dV_O}{dI_O}$	typ.	1.0	kΩ	

1) See also Figs. 4 and 5 on page 6.

2) Measured as a function of the input V_I of Fig.2 with the rise time adjusted to 100 μs; the output pulse is shown in Fig.3.
If the input is driven by a signal with a fall time (t_{If}) lower than 5 μs, an output signal with a rise time (t_{Ir}) of nominal 0.5 μs is obtained.

3) Power dissipation when all flip-flops and buffer stages are operating at maximum dissipation (extreme condition). In organ practice the average power dissipation is less because the master oscillators cause the flip-flops to switch continuously.

4) Measured under conditions of maximum current to the dividers.

5) All buffer stages in the LOW state, R_L = 10 kΩ.

CHARACTERISTICS (continued)

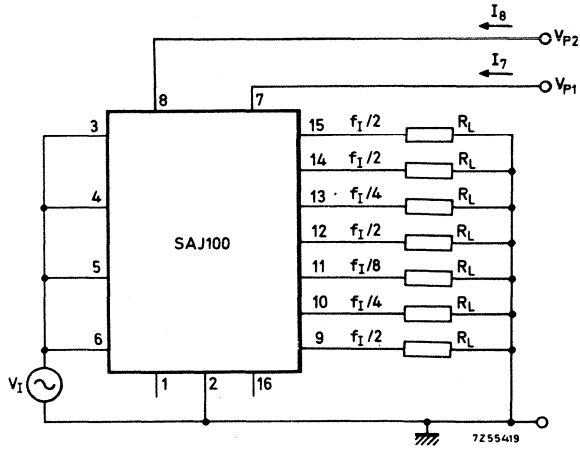


Fig.1. Test circuit

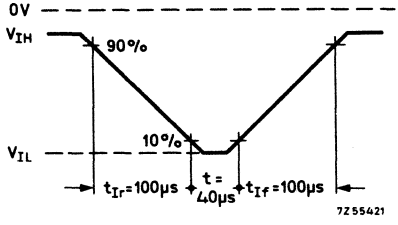


Fig.2. Input voltage V_I

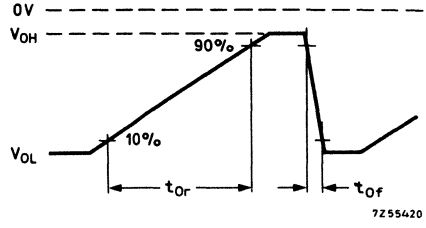


Fig.3. Output voltage at pins 9; 10; 11; 12; 13; 14; 15

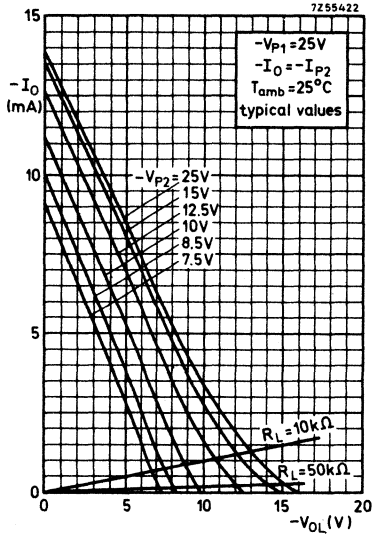


Fig. 4. Output characteristic

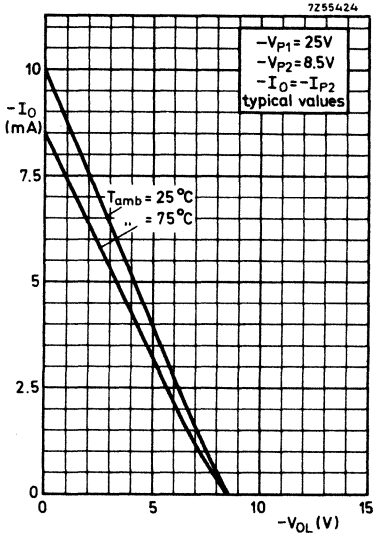


Fig. 5. Output characteristic

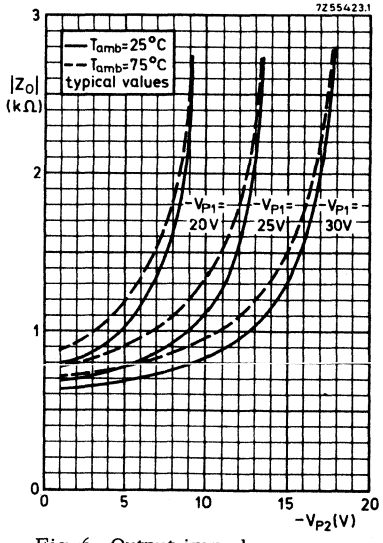
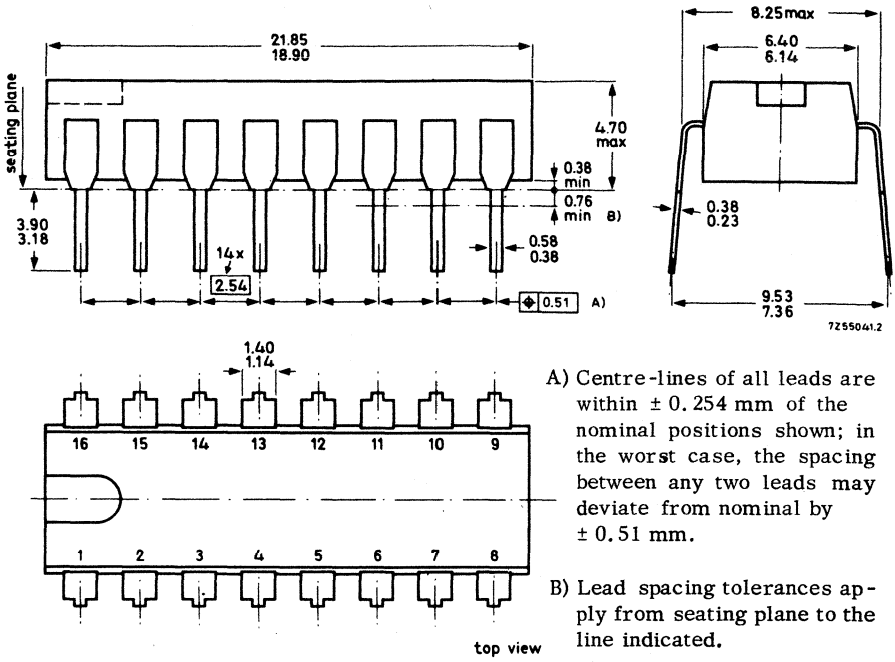


Fig. 6. Output impedance versus supply voltages

16 LEAD PLASTIC DUAL IN-LINE (type A)

Dimensions in mm



A) Centre-lines of all leads are within ± 0.254 mm of the nominal positions shown; in the worst case, the spacing between any two leads may deviate from nominal by ± 0.51 mm.

B) Lead spacing tolerances apply from seating plane to the line indicated.

SOLDERING

1. By hand

   Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

   260 °C is the maximum allowable temperature of the solder; it must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
   The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the allowable limit.

3. Repairing soldered joints

   The same precautions and limits apply as in (1) above.

INDEX OF TYPE NUMBERS

The inclusion of a type number in this publication does not necessarily imply its availability.

DTL = FC family
MOS = FD family
TTL = FJ family

CML = GH family
DTL/HNIL = FZ family
TTL = FJ/GJ family

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